



# Intel® 875P MCH/ E7210 MCH and Intel® 6300ESB ICH Chipset Platform

## Design Guide

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*August 2005*

For use with the Intel® Pentium® 4 Processor and Intel® Pentium® 4  
Processor with Hyper-Threading Technology†



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## Revision History

Date	Revision	Description
August 2005	002	Updated sections 9.15, 10, 13.3.4.7.1, and 16.7. Also included general updates.
February 2004	001	Initial release of this document.

# Introduction

# 1

This design guide documents Intel's design recommendations for systems based on the Intel® Pentium® 4 Processor and Intel® Pentium® 4 Processor with Hyper-Threading Technology<sup>†</sup> and the Intel® 875P Memory Controller Hub (MCH)/Intel® E7210 MCH/Intel® 6300ESB I/O Controller Hub (ICH) chipset. In addition to providing motherboard design recommendations such as layout and routing guidelines, this document will also address other system design issues such as power delivery.

Carefully follow the design information, board schematics, debug recommendations, and system checklists provided in this document. These design guidelines have been developed to ensure maximum flexibility for board designers while reducing the risk of board related issues.

Note that the guidelines recommended in this document are based on experience and preliminary simulation work done at Intel while developing the Pentium 4 / Pentium 4 with HT Technology and 875P MCH/E7210 MCH/6300ESB ICH chipset-based systems. This work is ongoing, and the recommendations are subject to change.

Board designers may use the associated Intel schematics as a reference. While the schematics cover a specific design implementation, the core schematics will remain the same for most 875P MCH/6300ESB ICH chipset-based platforms. The schematic set provides a reference schematic for each 875P MCH/6300ESB ICH chipset component as well as common motherboard options. Additional flexibility is possible through other permutations of these options and components.

**Note:** Unless otherwise specified, the term MCH in this document refers to the 875P MCH or the E7210 MCH.

## 1.1 Reference Documentation

The following documents are referenced throughout this design guide. Documents indicated as available on FDBL may require the assistance of an Intel field representative.

**Table 1. Reference Documentation (Sheet 1 of 3)**

Document	Document Number/Source
6300ESB I/O Controller Datasheet	<a href="http://www.intel.com/design/intarch/datashts/300641.htm">http://www.intel.com/design/intarch/datashts/300641.htm</a>
6300ESB I/O Controller Hub (ICH) Specification Update	<a href="http://www.intel.com/design/intarch/specupdt/300884.htm">http://www.intel.com/design/intarch/specupdt/300884.htm</a>
82540EM Gigabit Ethernet Controller Datasheet	<a href="http://www.intel.com/design/network/datashts/82540em_ds.htm">http://www.intel.com/design/network/datashts/82540em_ds.htm</a>
82547GI / 82547EI Gigabit Ethernet Controller Networking Silicon Datasheet	<a href="http://www.intel.com/design/network/datashts/82547gi_ei_ds.htm">http://www.intel.com/design/network/datashts/82547gi_ei_ds.htm</a>
82551QM/82540EM Interchangeable LOM Design Guide Application Note	<a href="http://www.intel.com/design/network/applnotts/ap432.htm">http://www.intel.com/design/network/applnotts/ap432.htm</a>
82551QM Fast Ethernet Multifunction PCI/ CardBus Controller Datasheet	<a href="http://www.intel.com/design/network/datashts/82551qm_ds.htm">http://www.intel.com/design/network/datashts/82551qm_ds.htm</a>

Table 1. Reference Documentation (Sheet 2 of 3)

Document	Document Number/Source
82562ET LAN on Motherboard Design Guide Application Note, AP-414	<a href="http://www.intel.com/design/network/applnnts/82562et_ap414.htm">http://www.intel.com/design/network/applnnts/82562et_ap414.htm</a>
82562ET/EM Platform LAN Connect (PLC) Printed Circuit Board (PCB) Design Application Note	Please contact your Intel Field Representative and request document AP-412.
82562EZ(EX)/82540EM Dual Footprint LOM Design Guide Application Note (AP-434)	<a href="http://www.intel.com/design/network/applnnts/ap434.htm">http://www.intel.com/design/network/applnnts/ap434.htm</a>
875P Chipset: Intel® 82875P Memory Controller Hub (MCH) Datasheet	<a href="http://www.intel.com/design/chipsets/datashts/252525.htm">http://www.intel.com/design/chipsets/datashts/252525.htm</a>
875P/E7210/6300ESB Chipset Platform Design Guide	<a href="http://www.intel.com/design/intarch/designngd/300907.htm">http://www.intel.com/design/intarch/designngd/300907.htm</a>
875P Memory Controller Hub (MCH) External Design Specification Addendum	Please contact your Intel Field Representative.
AGP Interface Specification	Please contact your Intel Field Representative.
AGP Design Guide	Please contact your Intel Field Representative.
Alert Standard Format Z(ASF) Specification	<a href="http://www.dmtf.org/standards/standard_alert.php">http://www.dmtf.org/standards/standard_alert.php</a>
AT Attachment with Packet Interface - 6 (ATA/ATAPI-6)	<a href="http://webstore.ansi.org/ansidocstore/default.asp">http://webstore.ansi.org/ansidocstore/default.asp</a>
Audio Codec '97 Specification	<a href="http://www.intel.com/labs/media/audio/index.htm">http://www.intel.com/labs/media/audio/index.htm</a>
CK409 Clock Synthesizer Design Guidelines	Please contact your Intel Field Representative.
CK409 Clock Synthesizer/Driver Specification	Please contact your Intel Field Representative.
Communication and Network Riser Specification	Please contact your Intel Field Representative.
Communication and Network Riser Reference Design Application Note AP-418	Please contact your Intel Field Representative and request document AP-418.
Desktop System Air Duct Design Suggestions	Please contact your Intel Field Representative.
E7210 Memory Controller Hub (MCH) Datasheet	<a href="http://www.intel.com/design/chipsets/e7210/300798.htm">http://www.intel.com/design/chipsets/e7210/300798.htm</a>
E7210 MCH External Design Specification Addendum	Please contact your Intel Field Representative.
Flash BIOS Specification	Please contact your Intel Field Representative.
Front Panel I/O Connectivity Design Guide	<a href="http://www.formfactors.org/developer/specs/A2928604-005.pdf">http://www.formfactors.org/developer/specs/A2928604-005.pdf</a>
FWH Specification	Please contact your Intel Field Representative.
GPE Routing for Windows* - General Purpose Event Register Wiring	<a href="http://www.microsoft.com/whdc/system/pnppwr/powermgmt/GPE_routing.msp">http://www.microsoft.com/whdc/system/pnppwr/powermgmt/GPE_routing.msp</a>
ICH Family Real Time Clock (RTC) Accuracy and Considerations under Test Conditions Application Note	<a href="http://www.intel.com/design/chipsets/applnnts/292276.htm">http://www.intel.com/design/chipsets/applnnts/292276.htm</a>
ITP700 Debug Port Design Guide	<a href="http://developer.intel.com/design/Pentium4/documentation.htm">http://developer.intel.com/design/Pentium4/documentation.htm</a>
Pentium 4 Processor 90 nm Process Datasheet	<a href="http://developer.intel.com/design/Pentium4/documentation.htm">http://developer.intel.com/design/Pentium4/documentation.htm</a>
Pentium 4 Processor on 90 nm Process Thermal and Mechanical Design Guide	<a href="http://developer.intel.com/design/Pentium4/documentation.htm">http://developer.intel.com/design/Pentium4/documentation.htm</a>



Table 1. Reference Documentation (Sheet 3 of 3)

Document	Document Number/Source
<i>Pentium® 4 Processor Supporting Hyper-Threading Technology Datasheet</i>	<a href="http://developer.intel.com/design/Pentium4/documentation.htm">http://developer.intel.com/design/Pentium4/documentation.htm</a>
<i>Pentium 4 Processor with 512 KB L2 Cache on 0.13 Micron Process Datasheet</i>	<a href="http://developer.intel.com/design/Pentium4/documentation.htm">http://developer.intel.com/design/Pentium4/documentation.htm</a>
<i>Pentium® 4 Processor with 512-KB L2 Cache on 0.13 Micron Process Thermal Design Guidelines</i>	<a href="http://www.intel.com/design/pentium4/guides/252161.htm">http://www.intel.com/design/pentium4/guides/252161.htm</a>
<i>Pentium 4 Processor with HT Technology I/O Buffer Models</i>	Please contact your Intel Field Representative.
<i>Low Pin Count Interface Specification</i>	<a href="http://www.intel.com/design/chipsets/industry/lpc.htm">http://www.intel.com/design/chipsets/industry/lpc.htm</a>
<i>PCI-X Specification</i>	<a href="http://www.pcisig.com/specifications">http://www.pcisig.com/specifications</a>
<i>PNG OEM 82562ET Datasheet</i>	Please contact your Intel Field Representative and request document 58327 (available on FDBL).
<i>PNG OEM 82562EM Datasheet</i>	Please contact your Intel Field Representative and request document 59104 (available on FDBL).
<i>PNG OEM 82562EX/EZ Datasheet</i>	Please contact your Intel Field Representative and request document 10522.
<i>Serial ATA Specification</i>	<a href="http://www.serialata.org/specifications.asp">http://www.serialata.org/specifications.asp</a>
<i>System Management Bus Specification</i>	<a href="http://www.smbus.org/specs/index.html">http://www.smbus.org/specs/index.html</a>
<i>Universal Serial Bus Specification</i>	<a href="http://www.intel.com/technology/usb/spec.htm">http://www.intel.com/technology/usb/spec.htm</a>
<i>Voltage Regulator-Down (VRD) 10.0 Power Delivery for Desktop Socket 478 Design Guide</i>	<a href="http://developer.intel.com/design/Pentium4/documentation.htm">http://developer.intel.com/design/Pentium4/documentation.htm</a>

## 1.2 Conventions and Terminology

This section defines conventions and terminology that are used throughout the design guide.

<b>Aggressor</b>	A network that transmits a coupled signal to another network.
<b>AGTL+</b>	The front-side bus uses a bus technology called AGTL+, or Assisted Gunning Transceiver Logic. AGTL+ buffers are open-drain, and require pull-up resistors to provide the high logic level and termination. AGTL+ output buffers differ from GTL+ buffers by the addition of an active pMOS pull-up transistor to assist the pull-up resistors during the first clock of a low-to-high voltage transition.
<b>Asynchronous GTL+</b>	The processor does not utilize CMOS voltage levels on any signals that connect to the processor. As a result, legacy input signals such as A20M#, IGNNE#, INIT#, LINT0/INTR, LINT1/NMI, PWRGOOD, SMI#, SLP#, and STPCLK# utilize GTL+ input buffers. Legacy output signals (FERR# and IERR#) and non-AGTL+ signals (THERMTRIP# and PROCHOT#) also utilize GTL+ output buffers. All of these signals follow the same DC requirements as AGTL+ signals; however the outputs are not actively driven high (during a logical 0 to 1 transition) by the processor (the major difference between GTL+ and AGTL+). These signals do not have setup or hold time specifications in relation to BCLK[1:0], and are therefore referred to as asynchronous GTL+ signals.

However, all of the asynchronous GTL+ signals are required to be asserted for at least two BCLKs in order for the processor to recognize them.

**Bus Agent**

A component or group of components that, when combined, represent a single load on the AGTL+ bus.

**Crosstalk**

The reception on a victim network of a signal imposed by aggressor network(s) through inductive and capacitive coupling between the networks.

- Backward Crosstalk— Coupling that creates a signal in a victim network that travels in the opposite direction as the aggressor's signal.
- Forward Crosstalk— Coupling that creates a signal in a victim network that travels in the same direction as the aggressor's signal.
- Even Mode Crosstalk— Coupling from a signal or multiple aggressors when all the aggressors switch in the same direction that the victim is switching.
- Odd Mode Crosstalk— Coupling from a signal or multiple aggressors when all the aggressors switch in the opposite direction that the victim is switching.

**Flight Time**

Flight time is a term in the timing equation that includes the signal propagation delay, any effects the system has on the TCO of the driver, plus any adjustments to the signal at the receiver needed to ensure the setup time of the receiver. More precisely, flight time is defined as:

- The time difference between a signal at the input pin of a receiving agent crossing the switching voltage (adjusted to meet the receiver manufacturer's conditions required for AC timing specifications; i.e., ringback, etc.) and the output pin of the driving agent crossing the switching voltage when the driver is driving a test load used to specify the driver's AC timings.
- Maximum and Minimum Flight Time— Flight time variations are caused by many different parameters. The more obvious causes include variation of the board dielectric constant, changes in load condition, crosstalk, power noise, variation in termination resistance, and differences in I/O buffer performance as a function of temperature, voltage, and manufacturing process. Some less obvious causes include effects of simultaneous switching output (SSO) and packaging effects.
- Maximum flight time is the largest acceptable flight time a network will experience under all conditions.
- Minimum flight time is the smallest acceptable flight time a network will experience under all conditions.

**ISI**

Inter-symbol interference is the effect of a previous signal (or transition) on the interconnect delay. For example, when a signal is transmitted down a line and the reflections due to the transition have not completely dissipated, the following data transition launched onto the bus is affected. ISI is dependent upon frequency, time delay of the line, and the reflection coefficient at the driver and receiver. ISI may impact both timing and signal integrity.

<b>Network</b>	The network is the trace of a printed circuit board (PCB) that completes an electrical connection between two or more components.
<b>Overshoot</b>	The maximum voltage observed for a signal at the device pad, measured with respect to VCC.
<b>Pad</b>	The electrical contact point of a semiconductor die to the package substrate. A pad is only observable in simulations.
<b>Pin</b>	The contact point of a component package to the traces on a substrate, such as the motherboard. Signal quality and timings may be measured at the pin.
<b>Power-Good</b>	“Power-Good,” “PWRGOOD,” or “CPUPWRGOOD” (an active high signal) indicates that all of the system power supplies and clocks are stable. PWRGOOD should go active a predetermined time after system voltages are stable and should go inactive as soon as any of these voltages fail their specifications.
<b>Ringback</b>	The voltage to which a signal changes after reaching its maximum absolute value. Ringback may be caused by reflections, driver oscillations, or other transmission line phenomena.
<b>System Bus</b>	The microprocessor bus of the processor.
<b>Setup Window</b>	The time between the beginning of Setup to Clock (TSU_MIN) and the arrival of a valid clock edge. This window may be different for each type of bus agent in the system.
<b>SSO</b>	Simultaneous switching output (SSO) effects are differences in electrical timing parameters and degradation in signal quality caused by multiple signal outputs simultaneously switching voltage levels in the opposite direction from a single signal or in the same direction. These are called odd mode and even mode switching, respectively. This simultaneous switching of multiple outputs creates higher current swings that may cause additional propagation delay (“push-out”) or a decrease in propagation delay (“pull-in”). These SSO effects may impact the setup and/or hold times and are not always taken into account by simulations. System timing budgets should include margin for SSO effects.
<b>Stub</b>	The branch from the bus trunk terminating at the pad of an agent.
<b>Trunk</b>	The main connection, excluding interconnect branches, from one end agent pad to the other end agent pad.
<b>Undershoot</b>	The minimum voltage extending below VSS observed for a signal at the device pad.
<b>VCC (CPU core)</b>	VCC (CPU core) is the core power for the processor. The system bus is terminated to VCC (CPU core).
<b>Victim</b>	A network that receives a coupled crosstalk signal from another network.
<b>VRD 10.0</b>	The Voltage Regulator Module (a down on the board solution) specification for the Pentium 4 processor with HT. It is a DC-DC converter module that supplies the required voltage and current to a single processor.

Table 2 defines the acronyms, conventions, and terms that are used throughout the design guide.

**Table 2. Conventions and Terminology**

Acronym/Convention/ Term	Definition
AC	Audio Codec
ASF	Alert Standard Format
AMC	Audio/Modem Codec.
Anti-Etch	Any plane-split, void or cutout in a VCC or GND plane
CMC	Common Mode Choke
CNR	Communications and Networking Riser
EMI	Electro Magnetic Interference
ESD	Electrostatic Discharge
FS	Full-speed. Refers to USB.
HS	High-speed. Refers to USB.
ICH	I/O Controller Hub
LOM	LAN on Motherboard
LPC	Low Pin Count
LS	Low-speed. Refers to USB.
MC	Modem Codec
PCM	Pulse Code Modulation
PLC	Platform LAN Connect
RTC	Real Time Clock
SATA	Serial ATA
SMBus	System Management Bus. A two-wire interface through which various system components may communicate.
SPD	Serial Presence Detect
STR	Suspend To RAM
TCO	Total Cost of Ownership
TDM	Time Division Multiplexed
TDR	Time Domain Reflectometry
µBGA	Micro Ball Grid Array
USB	Universal Serial Bus

# System Overview

# 2

The 875P MCH/E7210 MCH/6300ESB ICH contains the following main components:

- Either the 875P Memory Controller Hub (MCH) or the E7210 MCH
- The 6300ESB I/O Controller Hub (ICH)

These components are interconnected through an Intel proprietary interface called the Hub Interface.

## 2.1 Intel® 875P MCH and Intel® E7210 MCH System Features

The 875P MCH and the E7210 MCH are designed for use with a single UP-capable processor in the 478 pin package. The role of the 875P MCH and E7210 MCH is to arbitrate the flow of information between the five system interfaces: front side bus (FSB), system memory, accelerated graphics port (AGP) (875P MCH only), hub interface, and CSA interface.

### 2.1.1 System Memory Interface

The 875P MCH and E7210 MCH integrates a system memory DDR controller with two 64-bit wide interfaces.

#### System Memory Interface

- Supports two 64-bit wide DDR data channels
- Available bandwidth up to 3.2 GBytes/s (DDR-400) for single-channel mode and 6.4 GBytes/s (DDR-400) in dual-channel mode
- Supports 128 MB, 256 MB, 512 MB DDR technologies
- Supports only x8, x16, DDR devices with four banks
- Registered DIMMs not supported
- Supports opportunistic refresh
- Up to 16 simultaneously open pages (four per row, four rows maximum)
- SPD (serial presence detect) scheme for DIMM detection support
- Suspend-to-RAM support using CKE
- Supports configurations defined in the JEDEC DDR1 DIMM specification only

#### Single-Channel DDR Configuration

- Supports 2.0 GBytes maximum system memory
- Supports up to two DDR DIMMs, single-sided and/or double-sided

- Supports DDR-266/333/400 unbuffered ECC and non-ECC DDR DIMMs
- Does not support registered DIMMs
- Does not support mixed-mode/uneven double-sided DDR DIMMs (not validated)

### **Dual-Channel DDR Configuration - Lockstep**

- Supports 4.0 GBytes maximum system memory
- Supports up to four DDR DIMMs, single-sided and/or double-sided
- DIMMs must be populated in identical pairs for Dual-Channel operation
- Supports 16 simultaneous open pages (four per row)
- Supports DDR-266/333/400 unbuffered ECC and non-ECC DDR DIMMs

## **2.1.2 Supported Frequencies**

The following configurations are supported by the 875P MCH and E7210 MCH:

- 800 MHz FSB, 400 MHz memory interface
- 800 MHz FSB, 333 MHz memory interface
- 533 MHz FSB, 333 MHz memory interface
- 400 MHz FSB, 266 MHz memory interface

## **2.1.3 Hub Interface**

The Hub Interface connects the 875P MCH or E7210 MCH to the 6300ESB ICH. The 875P MCH or E7210 MCH supports only HI 1.5, which utilizes HI 1.0 protocol with HI 2.0 electricals. The hub interface runs at 266 MT/s (with 66 MHz base clock) and utilizes 1.5 V signaling. Accesses between the hub interface and AGP are limited to hub interface-originated memory writes to AGP.

## **2.1.4 Communications Streaming Architecture (CSA) Interface**

The CSA interface connects the 875P MCH or E7210 MCH with the 82547GI GbE controller. The CSA interface runs at 266 MT/s (with 66 MHz base clock) and utilizes 1.5 V signaling.

## **2.1.5 AGP Interface (875P MCH Only)**

The 875P MCH has support for an AGP 8X mode slot. This slot meets the requirements of the AGP 3.0 specification including 0.8 V and 1.5 V AGP electricals. The following features are supported by the 875P MCH:

- AGP 8X fast writes
- PIPE# or SBA[7:0] AGP address mechanisms
- 32-deep AGP request queue
- High priority accesses

## 2.2 Intel® 6300ESB ICH System Features

The 6300ESB ICH is designed for a variety of processors/memory controller hubs and contains enhancements to the Intel® ICH4 and Intel® ICH5 controller hubs.

The ACPI-compliant 6300ESB ICH may support the Full-on, Stop-grant, Suspend-to-RAM, Suspend-to-Disk, and Soft-Off power management states.

The 6300ESB ICH component provides the data buffering and interface arbitration required to ensure that system interfaces operate efficiently and provide the bandwidth necessary to enable the system to obtain peak performance.

The 6300ESB ICH system provides the I/O subsystem with access to the rest of the system. Additionally, it integrates many I/O functions. The 6300ESB ICH integrates:

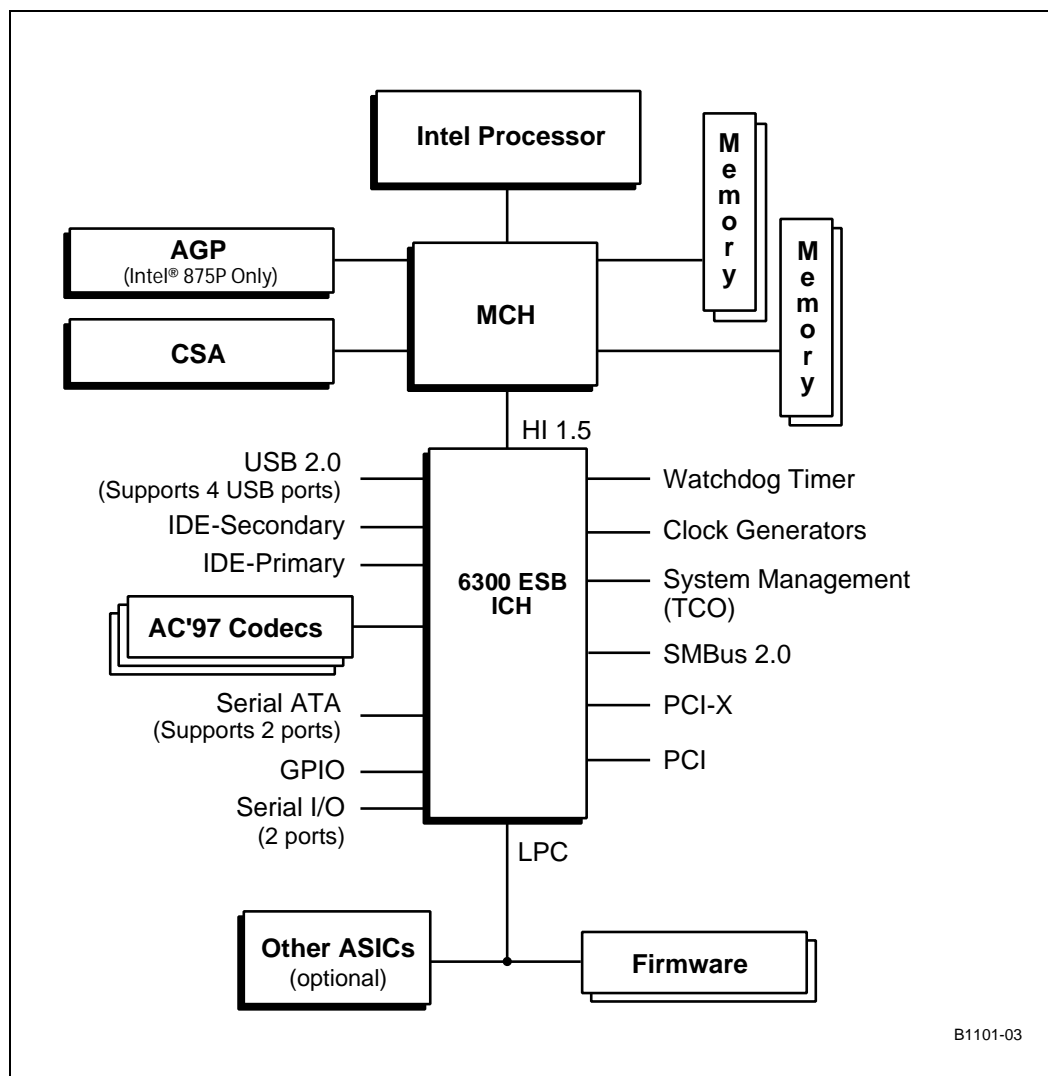
- The upstream hub interface for access to the MCH
- Two port Serial ATA controller
- Two channel Ultra ATA/100 Bus Master IDE controller
- One EHCI USB 2.0 host controller and two UHCI USB 1.1 host controllers (expanded capabilities for four ports)
- I/O APIC
- SMBus 2.0 controller
- FWH interface
- LPC interface
- AC '97 2.2 interface
- PCI-X 1.0 interface
- PCI 2.2 interface
- Two serial I/O ports
- Two-stage watchdog timer

The 6300ESB ICH also contains the arbitration and buffering necessary to ensure efficient utilization of these interfaces.

## 2.2.1 System Configurations

Figure 1 shows typical platform configurations using the 6300ESB ICH component.

Figure 1. Intel® 6300ESB ICH Uni-Processor System Block Diagram



## 2.2.2 Serial ATA

The 6300ESB ICH contains two integrated Serial ATA (SATA) host controllers capable of independent DMA operation on two ports. The SATA controllers are completely software transparent with the IDE interface, while providing a lower pin count and higher performance. The 6300ESB ICH SATA interface supports data transfer rates up to 150 MBytes/s.



### 2.2.3 USB 2.0 Support

The 6300ESB ICH contains two UHCI Host Controllers and one EHCI Host Controller. Each UHCI Host Controller includes a root hub with two separate USB ports each, for a total of four legacy USB ports. The EHCI Host Controller includes a root hub that supports up to four USB 2.0 ports. The 6300ESB ICH supports a maximum of four USB ports at any given time. The connection to either a UHCI or the EHCI is dynamic and dependent on the USB device capability meaning that all ports support HS/FS/LS.

### 2.2.4 PCI-X

The 6300ESB ICH supports a 64-bit, 66 MHz PCI-X\* interface. The PCI-X bus is capable of supporting four masters and has support for 64 bit addressing using DAC protocol. The PCI-X bus supports PCI Rev. 2.2 specification at 33 MHz and at PCI 64/66 MHz there is support for two masters. The PCI-X 66 MHz bus can support up to 480 MByte/s peer-to-peer transfers.

### 2.2.5 Watchdog Timer

The 6300ESB ICH contains a watchdog timer that provides unassisted reboot upon system hang and postmortem analysis. It also supports two modes: free-running or WDT. In free-running mode it acts as a one-stage timer that toggles the output pin when the loaded 20-bit counter reaches zero. In WDT mode it performs as a two-stage timer: the first stage generates an SMI when it reaches zero and after counting down. The second stage asserts the output pin which may be tied to the system reset logic.

### 2.2.6 Serial I/O

The 6300ESB ICH supports two Serial I/O ports. The Serial I/O ports have programmable baud rate generators, modem control functions, and configurable I/O address and IRQ. The Serial I/O ports are also capable of being disabled when an external SIO is used.

### 2.2.7 Manageability and Other Enhancements

The 6300ESB ICH platform integrates several functions designed to manage the system and lower the total cost of ownership (TCO) of the system. These system management functions are designed to report errors, diagnose the system, and recover from system lockups without the aid of an external microcontroller.

#### 2.2.7.1 SMBus 2.0

The 6300ESB ICH integrates an SMBus 2.0 controller. The SMBus provides an interface to manage peripherals such as serial presence detection (SPD) on RAM, thermal sensors, CNR cards, PCI cards, etc. The slave interface allows an external microcontroller to access system resources.

#### 2.2.7.2 Interrupt Controller

The interrupt capabilities of the 6300ESB ICH platform maintain the support for up to eight PCI interrupt pins and PCI 2.3 Message-Based Interrupts. In addition, the 6300ESB ICH supports Processor System Bus interrupt delivery.

### 2.2.7.3 Intel Compatible Flash BIOS

The 6300ESB ICH platform supports the Intel Compatible Flash BIOS Memory size up to 8 MBytes for increased system flexibility.

## 2.3 AC '97 Six-Channel Support

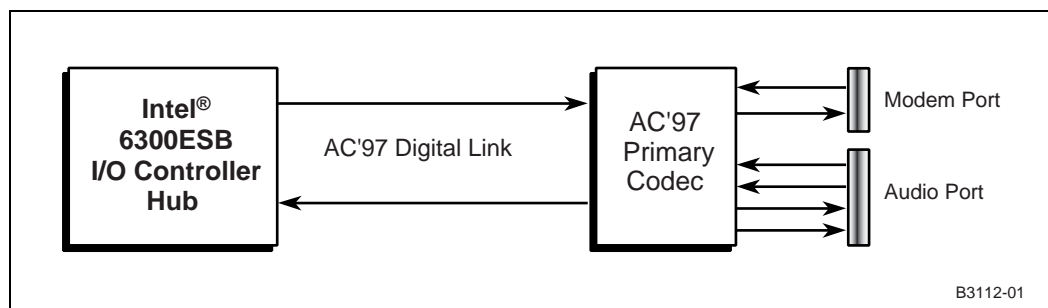
The Audio Codec '97 (AC '97) specification defines a digital interface that may be used to attach an audio codec (AC), a modem codec (MC), or an audio/modem codec (AMC) in various configurations. The AC '97 specification defines the interface between the system logic and the audio or modem codec, known as the AC '97 Digital Link.

The 6300ESB ICH's AC '97 (with the appropriate codecs) improves overall platform integration by incorporating the AC '97 digital link. By using an audio codec, the AC '97 digital link allows for cost-effective, high-quality, integrated audio on the 6300ESB ICH. In addition, an AC '97 soft modem may be implemented with the use of a modem codec. Several system options exist when implementing AC '97. The 6300ESB ICH integrated digital link allows several external codecs to be connected to the platform. The system designer may provide audio with an audio codec, a modem with a modem codec, or an integrated audio/modem codec (see [Figure 2](#)). The digital link is expanded to support three audio codecs or a combination of two audio codecs and a modem codec (see [Figure 3](#) and [Figure 4](#)).

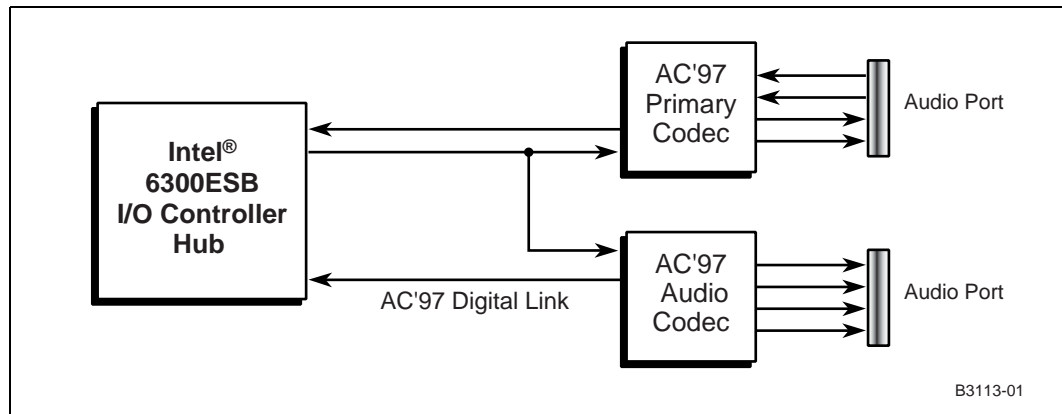
The digital link in the 6300ESB ICH is AC '97 Rev. 2.2 compliant, supporting up to three codecs with independent PCI functions for audio and modem. Microphone input and left and right audio channels are supported for a high quality two-speaker audio solution. Wake-on-ring from suspend is also supported with an appropriate modem codec.

The 6300ESB ICH expands audio capability with support for up to six channels of PCM audio output (full AC3 decode). Six-channel audio consists of Front Left, Front Right, Back Left, Back Right, Center, and Sub Woofer for a complete surround sound effect. 6300ESB ICH has expanded support for three audio codecs on the AC '97 digital link.

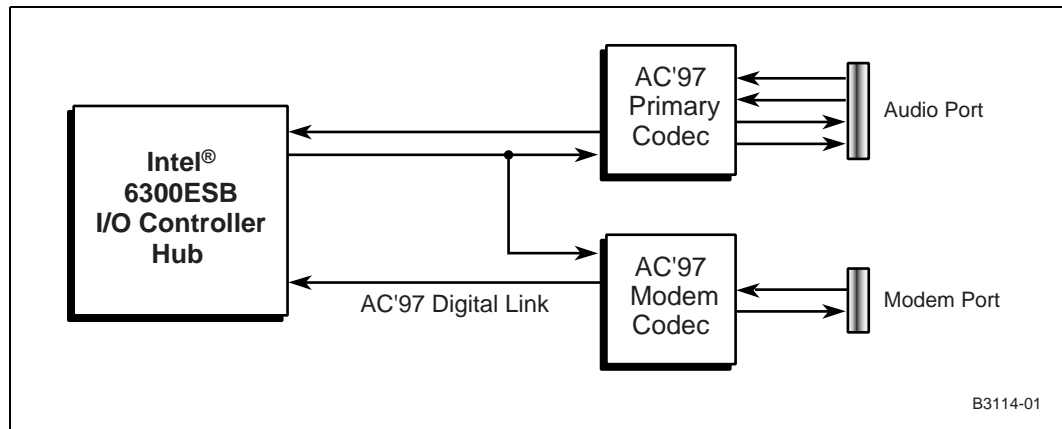
**Figure 2. AC'97 with Audio/Modem Codec**



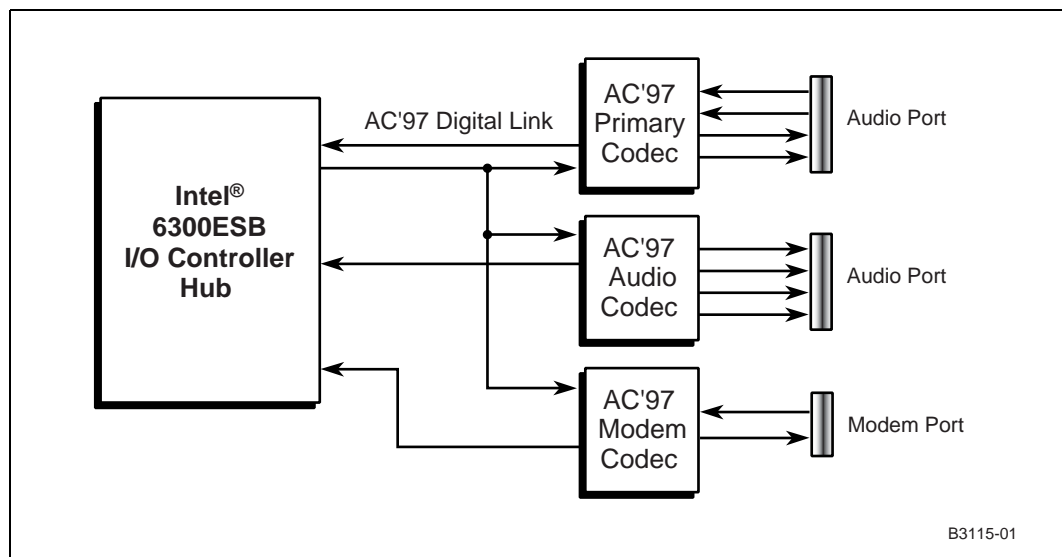
**Figure 3. AC'97 with Audio Codecs (Four Channel Secondary)**



**Figure 4. AC '97 with Audio and Modem Codec**



**Figure 5. AC'97 with Two Audio and a Modem Codec (Four Channel Secondary)**



## 2.4 Bandwidth Summary

Table 3 and Table 4 provide a summary of the bandwidth requirements for the 875P MCH/ E7210 MCH and 6300ESB ICH chipset platform.

**Table 3. Intel® 875P MCH and Intel® E7210 MCH System Bandwidth Summary**

Interface	Clock Speed (MHz)	Samples per Clock	Data Width (Bytes)	Bandwidth
System Bus	100/133/200	4	8	6.4 GBytes/s at 200 MHz
DDR-SDRAM	133/166/200	2	8	3.2 GBytes/s per channel 6.4 GBytes/s total at 200 MHz
AGP (875P MCH only)	66	8	4	2.1 Gbytes/s
CSA	66	4	1	266 MBytes/s

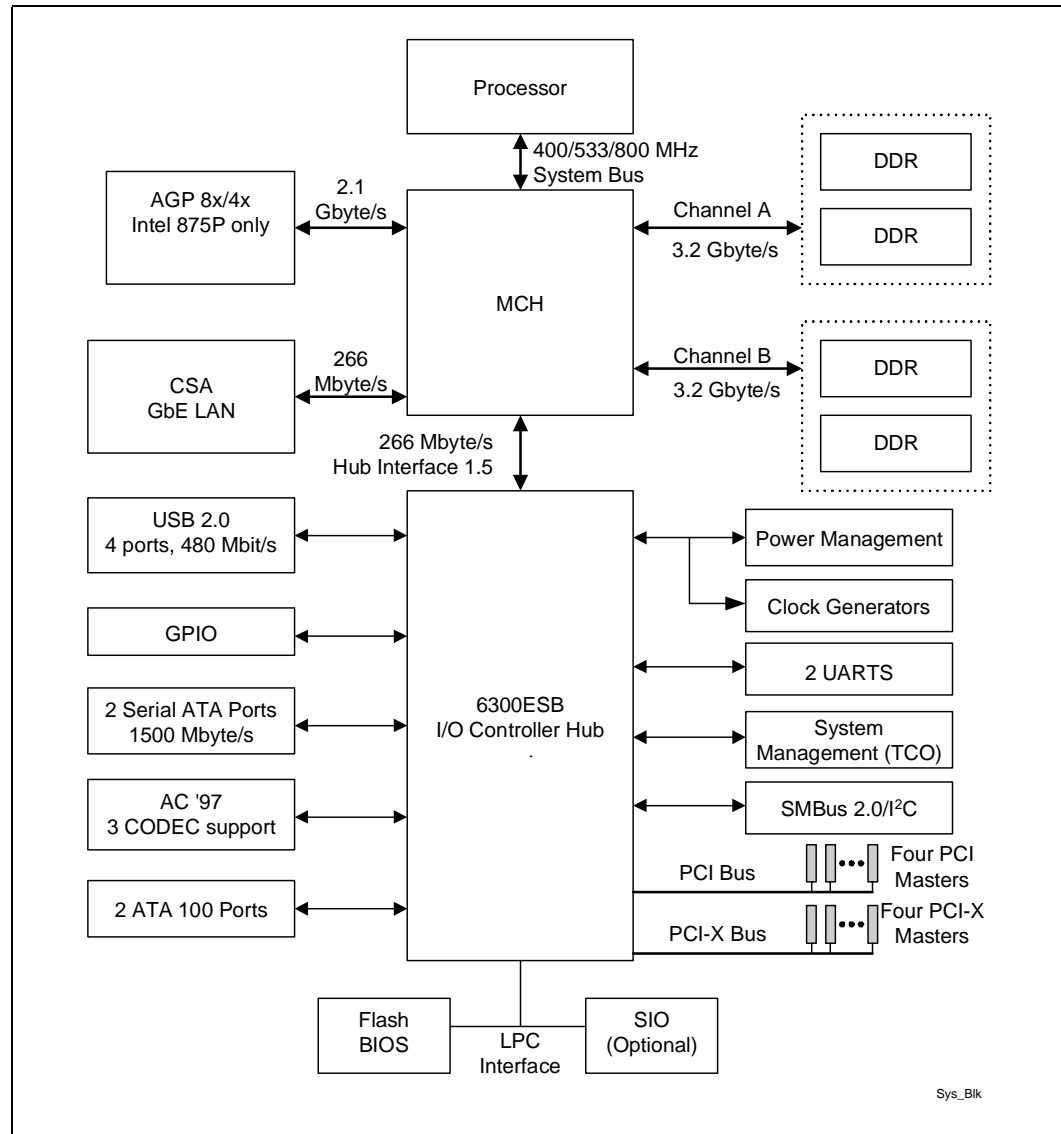
**Table 4. Intel® 6300ESB ICH System Bandwidth Summary**

Interface	Clock Speed (MHz)	Samples Per Clock	Data Rate (Mega-samples/s)	Data Width (Bits)	Bandwidth (Mbytes/s)
Hub Interface	66	4	266	8	266
PCI 2.3	33	1	33	32	133
IDE	Up to 44.444 Write Up to 50 Read	1	44.444 (Write) 50 (Read)	16	88.9 (Write) 100 (Read)
SATA	750	2	1500	1	150
AC '97	12.288	1	12.288	1	1.536
PCI-X	66	1	66	64	480
LPC	33	1	33	4	16.5
USB 2.0 High-speed	Up to 240 (embedded in data)	Up to 2	480	1	60
SMBus	10–16 kHz	1	10	1	1.25 Kbyte/s

## 2.5 System Configurations

Figure 6 illustrates a typical 875P MCH/E7210 MCH/6300ESB ICH based system configuration.

**Figure 6. Typical Intel® 875P MCH/Intel® E7210 MCH/Intel® 6300ESB ICH Chipset Based System Configuration**



# Platform Stack-Up and Placement Overview

## 3

In this section, an example of a 875P MCH/6300ESB ICH chipset platform component placement and stack-up is presented for a desktop system in an ATX board form factor with dual-channel, DDR-266/333/400 SDRAM memory capabilities.

### 3.1 General Design Considerations

This section documents motherboard layout and routing guidelines for E7210 MCH/6300ESB ICH platforms. This section does not discuss the functional aspects of any bus, or the layout guidelines for an add-in device.

If the guidelines listed in this document are not followed, it is very important that thorough signal integrity and timing simulations are completed for each design. Even when the guidelines are followed, critical signals are recommended to be simulated to ensure proper signal integrity and flight time. Any deviation from the guidelines should be simulated.

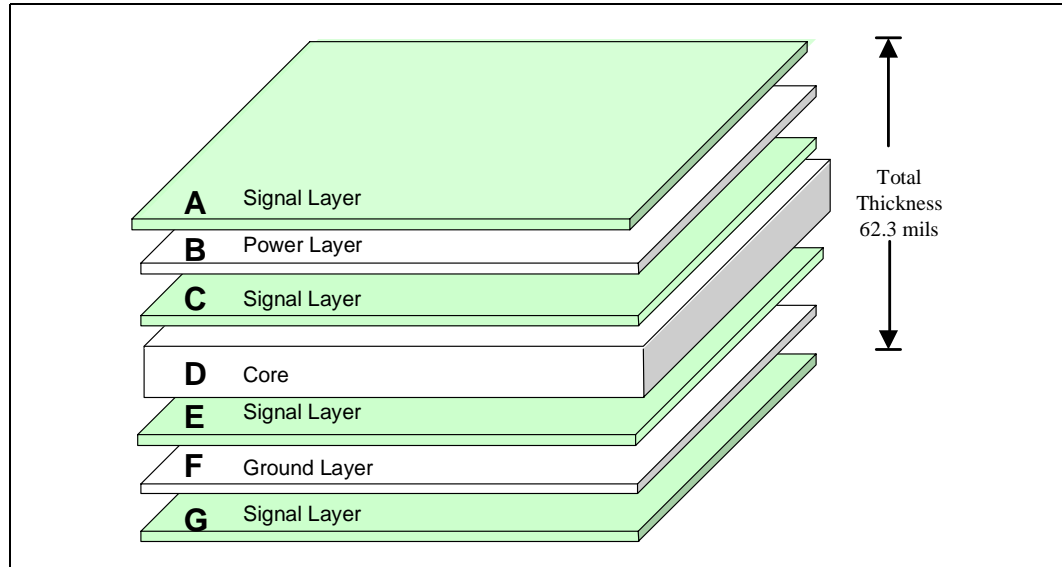
The trace impedance typically noted (i.e.,  $60 \Omega \pm 15\%$ ) is the “nominal” trace impedance for a 5 mil wide trace. That is, the impedance of the trace when not subjected to the fields created by changing current in neighboring traces. When calculating flight times, it is important to consider the minimum and maximum impedance of a trace based on the switching of neighboring traces. Using wider spaces between the traces may minimize this trace-to-trace coupling. In addition, these wider spaces reduce settling time.

Coupling between two traces is a function of the coupled length, the distance separating the traces, the signal edge rate, and the degree of mutual capacitance and inductance. In order to minimize the effects of trace-to-trace coupling, the routing guidelines documented in this section should be followed.

Additionally, these routing guidelines are created using a printed circuit board (PCB) stack-up as illustrated in [Figure 7](#).

### 3.2 Board Stack-Up

The E7210 MCH/6300ESB ICH platform requires a board stack-up yielding a target board impedance of  $60 \Omega \pm 15\%$ . Recommendations in this design guide are based on the following six layer board stack-up. The stack-up numbers may vary; it is important to stay within the specified tolerances.

**Figure 7. Six Layer PCB Stack-Up Example**


Description	Nominal Value	Tolerance	Comments
Board Impedance $Z_0$	60 $\Omega$	$\pm 15\%$	With nominal 5 mil trace width
Soldermask Er	4.0	$\pm 0.5$	@ 100 MHz
Soldermask Thickness	1.0 mil	$\pm 0.5$ mils	From top of trace
Trace Width	5.0 mils	$\pm 0.5$ mils	Standard trace

Layer	Description	Nominal Value	Tolerance	Prepreg Dielectric (Er) at 100 MHz	Comments
A	Signal Layer	0.7 mils	(See Note 2)		0.5 oz. Cu (See Note 1)
	Prepreg	4.4 mils	$\pm 0.6$ mils	$3.78 \pm 0.3$	
B	Power Layer	1.4 mils	$\pm 0.2$ mils		1 oz. unplated Cu
	Core	5.3 mils	$\pm 0.5$ mils	$3.9 \pm 0.3$	
C	Signal Layer	1.4 mils	$\pm 0.2$ mils		1 oz. unplated Cu
D	Core/Prepreg	31.6 mils	$\pm 3.0$ mils	$3.9 \pm 0.3$	
E	Signal Layer	1.4 mils	$\pm 0.2$ mils		1 oz. unplated Cu
	Core	5.3 mils	$\pm 0.5$ mils	$3.9 \pm 0.3$	
F	Ground Layer	1.4 mils	$\pm 0.2$ mils		1 oz. unplated Cu
	Prepreg	4.4 mils	$\pm 0.6$ mils	$3.78 \pm 0.3$	
G	Signal Layer	0.7 mils	(See Note 2)		0.5 oz. Cu (See Note 1)

**NOTES:**

1. Thickness before plating
2. Final Plating Thickness varies 1.3 mils - 1.42 mils (need 1.85 mils total)

### 3.2.1 PCB Technology Considerations

Intel has found that the following recommendation aids in the design of an E7210 MCH/6300ESB ICH-based platform. Simulations and the reference platform are based on the following technology, and it is recommended that designers adhere to these guidelines.

**Table 5. PCB Technologies Stack-Up**

Number of Layers	
Stack-up	6 Layer
Cu. Thickness	0.5 oz. outer (plated); 1 oz. Inner
Final Board Thickness	62.3 mils ( $\pm$ 5 mils)
Material	Fiberglass made of FR4
Signal and Power Via Stack	
Via Pad	25 mils
Via Anti-Pad	40 mils
Via Finished Hole	14 mils

### 3.2.2 Component Motherboard Layout (Pads and Vias)

Intel currently recommends non-solder mask defined pads (metal defined pads) with “dog-bone” connecting vias for its chipsets. When compared to solder mask defined pads, non-solder mask defined pads offer improved solder-joint reliability.

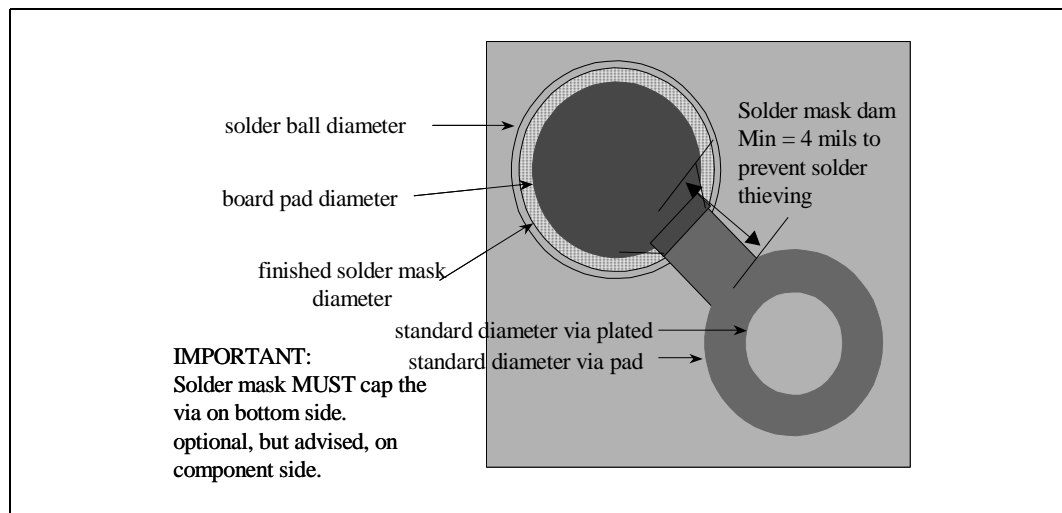
The solder mask opening and the registration accuracy of that opening relative to the pad is critical to ensure good solder joints and minimize shorting. If the opening is too large, misregistration may uncover a nearby trace increasing the possibility of a short occurring. Regardless of opening size, misregistration may cause solder mask material to cover part or the entire pad, yielding a joint with a poor cross-section (reliability) or a complete open.

Tips:

- Inconsistent solder mask coverage between the via and pad may lead to top and bottom side tenting in order to avoid accidentally wicking the solder ball into the via-hole, creating an open or unreliable joint. Tenting both sides may trap moisture in the via during reflow, causing severe solder mask damage as it vents. One solution is to ensure that the raw printed circuit boards are dry; an alternative is to allow for a small topside vent-hole (pin-hole) in the tenting.
- A reliability consideration to take into account when choosing a pad size: The pad size also affects the joint height; a smaller pad forces a taller joint. There are industry claims that a taller joint increases the mechanical flexibility of the joint and thus may improve power cycle and temperature cycle joint life.
- Solder mask must cap the vias on the bottom side of the board to minimize heat transfer to the solder.



**Figure 8. Via-Pad Layout— Metal-Defined Pads**



**Table 6. Via-Pad Layout— Metal-Defined Pads**

Component	Solder Ball Pitch	Solder Ball Diameter	Board Pad Diameter	Finished Solder Mask Diameter
CPU	1.27 mm	30 mils	20 mils	22 - 26 mils
MCH	1.00 mm	24 mils	18 mils	20 - 24 mils
ICH	1.27 mm	30 mils	20 - 24 mils	24 - 27mils

**Figure 9. Via-Pad Layout— Solder Mask-Defined Pads**

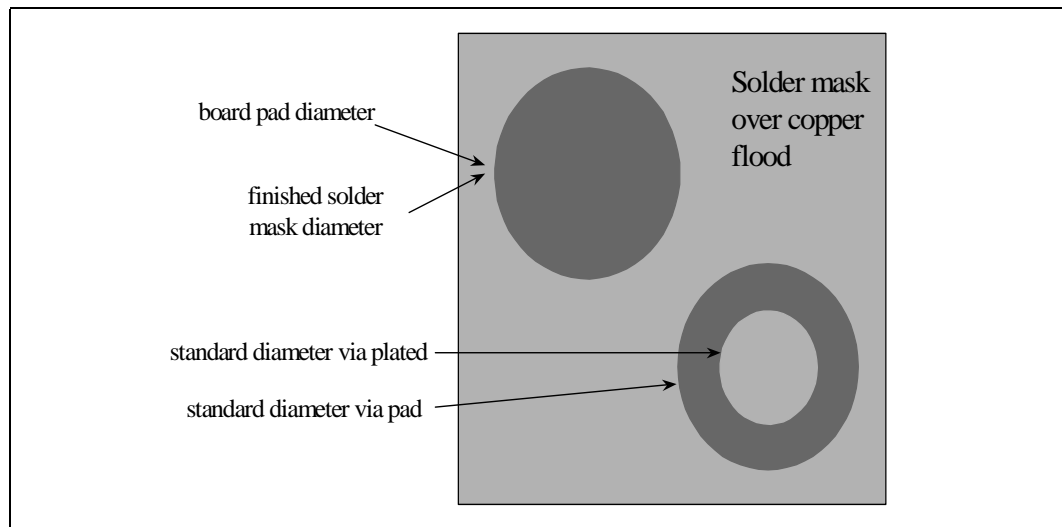


Table 7. Via-Pad Layout— Solder Mask-Defined Pads

Component	Solder Ball Pitch	Solder Ball Diameter	Board Pad Diameter	Finished Solder Mask Diameter
CPU	1.27 mm	30 mils	22 - 26 mils	22 - 26 mils
MCH	1.00 mm	24 mils	18 mils	18 mils
ICH	1.27 mm	30 mils	20 - 24 mils	20 - 24 mils

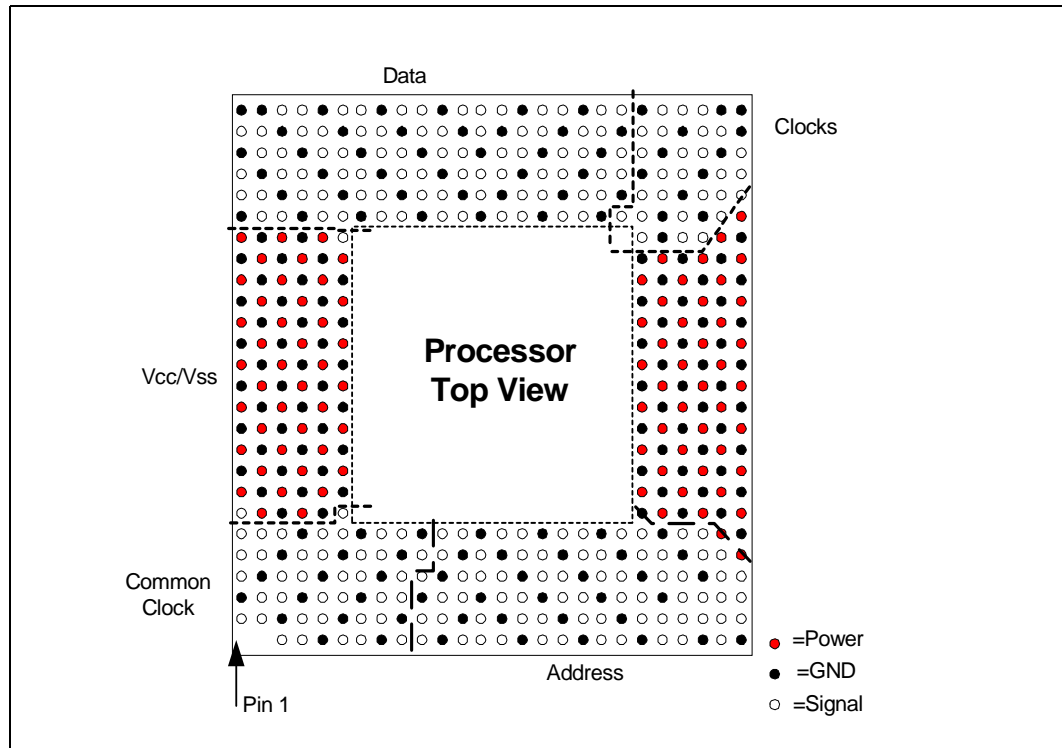
### 3.2.3 Component Quadrant Layout

The preliminary quadrant layouts shown are approximations. The quadrant layout figures do not show the exact component ball count; only general quadrant information is presented and is intended for reference while using this document. Only the exact pin or ball assignment should be used to conduct routing analysis. Reference the following documents for pin or ball assignment information.

- *Intel Pentium 4 Processor with 512 KByte L2 Cache on 0.13 Micron Process Datasheet*
- *Intel Pentium 4 Processor on 90 nm Process Datasheet*
- *Intel 875P Memory Controller Hub (MCH) Datasheet*
- *Intel E7210 Memory Controller Hub (MCH) Datasheet*
- *Intel 6300ESB I/O Controller Hub (ICH) Datasheet*

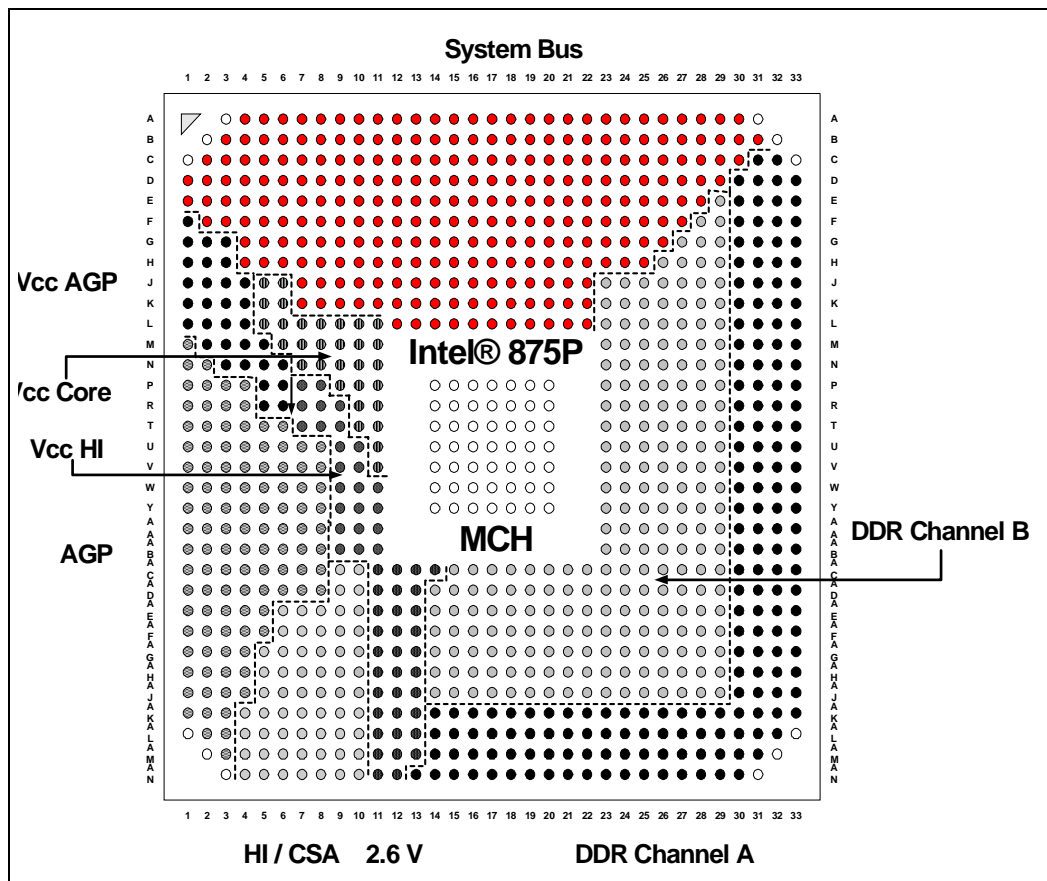
### 3.2.4 Pentium® 4 Processor with HT Technology† Component Quadrant Layout

Figure 10. Intel® Pentium® 4 Processor with HT Technology Component Quadrant Layout (Top View)



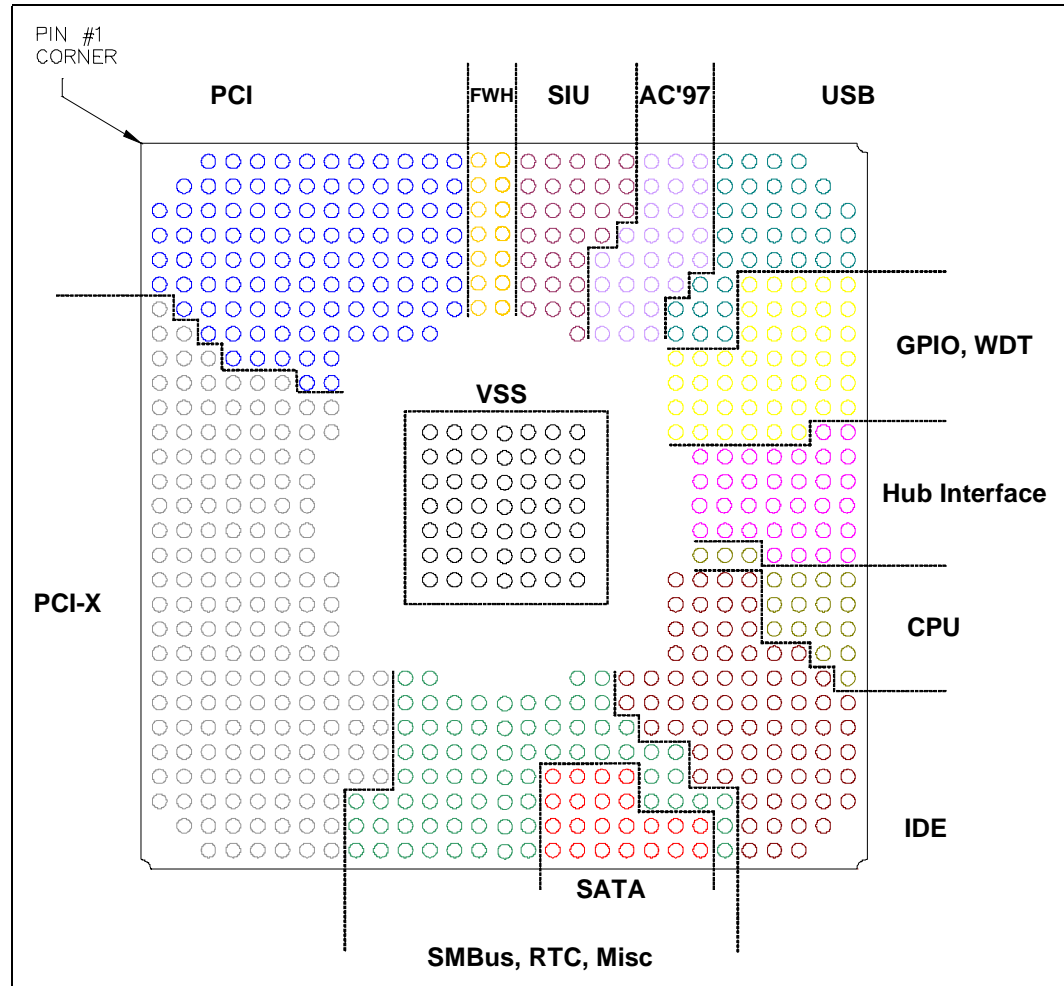
### 3.2.5 Intel® 875P MCH Component Quadrant Layout

Figure 11. Intel® 875P MCH Component Quadrant Layout (Top View)



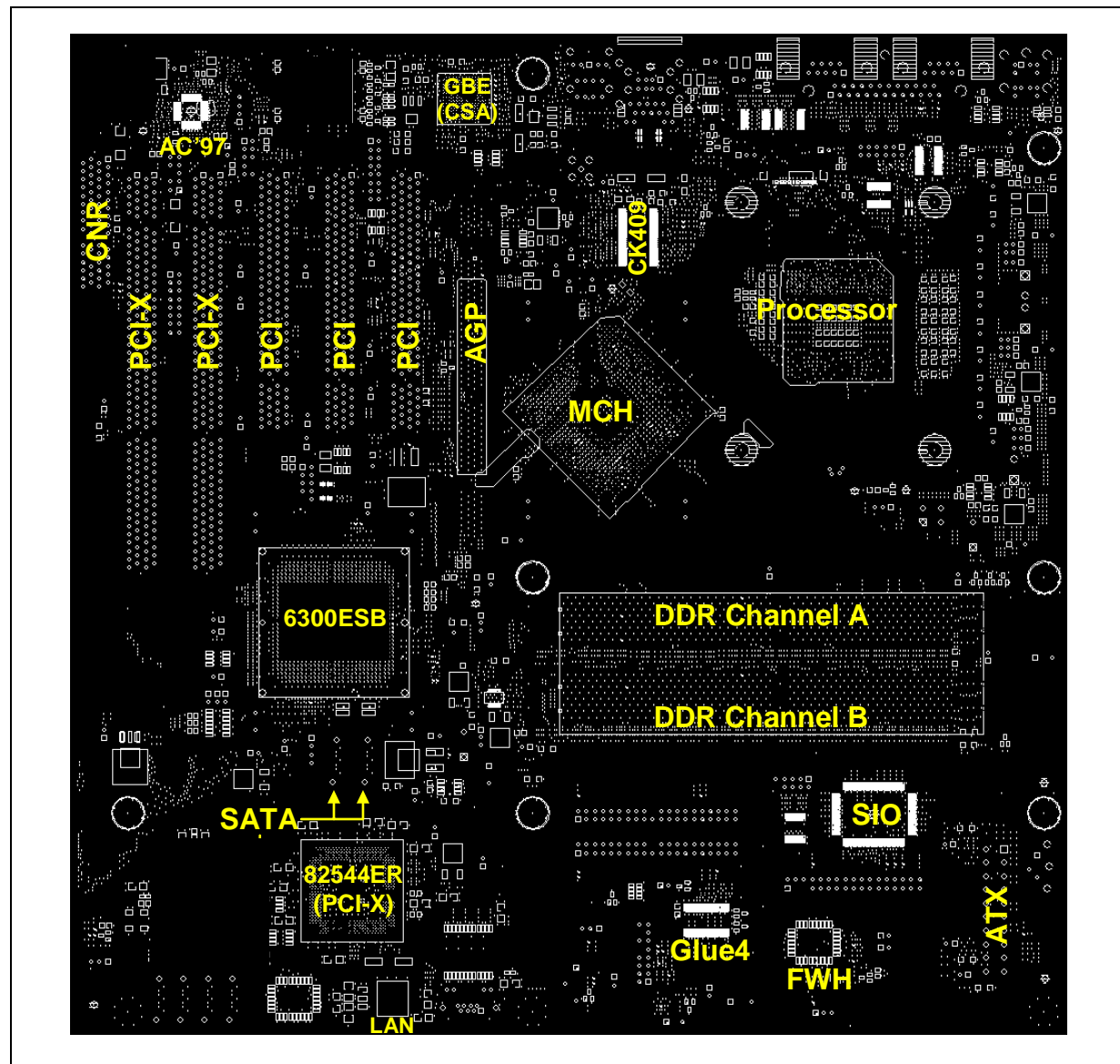
### 3.2.6 Intel® 6300ESB ICH Component Quadrant Layout

Figure 12. Intel® 6300ESB ICH Quadrant Layout (Top View)



### 3.3 Platform Component Placement

Figure 13. Intel® 6300ESB ICH Component Placement Example Using a 4-DIMM ATX Board



# Platform Clock Routing Guidelines 4

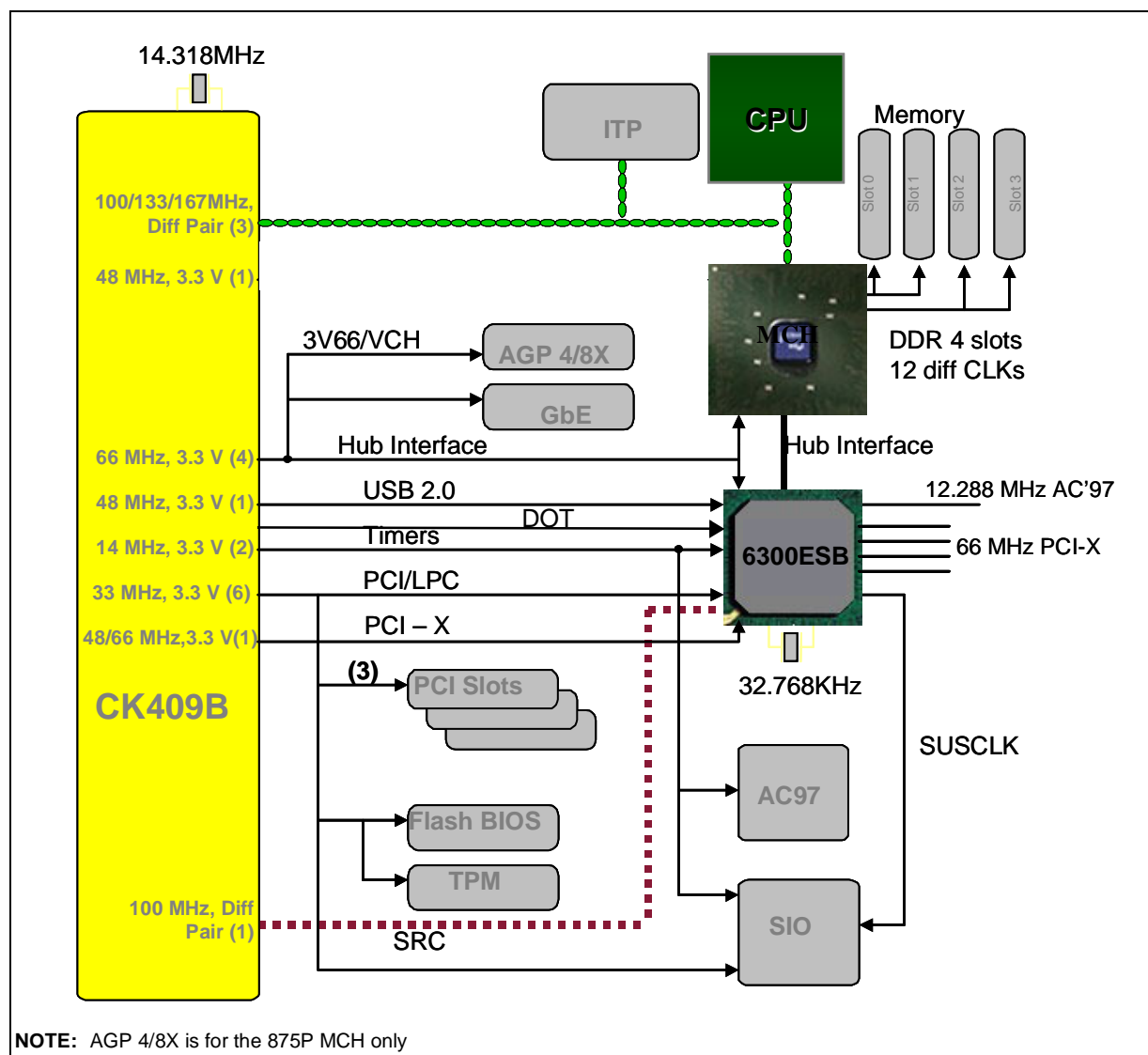
To minimize jitter, improve routing, and reduce cost, 875P MCH/E7210 MCH/6300ESB ICH chipset-based systems should use a single-chip clock solution, the CK409. In this configuration, the CK409 provides three 133/200 MHz selectable differential outputs pairs for all of the host bus agents, one 100 MHz differential output pair for serial ATA, two 48 MHz clocks, five 66 MHz clocks, ten 33 MHz clocks, and two 14 MHz clocks. [Figure 14](#) shows the implementation of the clocks for a typical E7210 MCH/6300ESB ICH platform.

For more information on CK409 compliance, refer to the *CK409 Clock Synthesizer/Driver Specification*.

**Table 8. Intel® E7210 MCH Clock Group**

Clock Name	Frequency (MHz)	Receiver
Host_CLK	100/133/200	Processor, Debug Port and MCH
CLK66	66	MCH, 6300ESB ICH, 82547GI GbE controller and AGP connector
CLK33_ICH	33	6300ESB ICH
CLK14	14.318	6300ESB ICH, and SIO
CLK33	33	PCI Connectors, SIO, and Flash BIOS
DOTCLK	48	ICH
SRC	100	6300ESB ICH— Serial ATA
USBCLK	48	6300ESB ICH

**Figure 14. Preliminary 875P MCH/E7210 MCH/6300ESB ICH Chipset-Based System Clocking Diagram**



## 4.1 Clock Groups

### 4.1.1 HOST\_CLK Clock Group

#### 4.1.1.1 HOST\_CLK Clock Topology

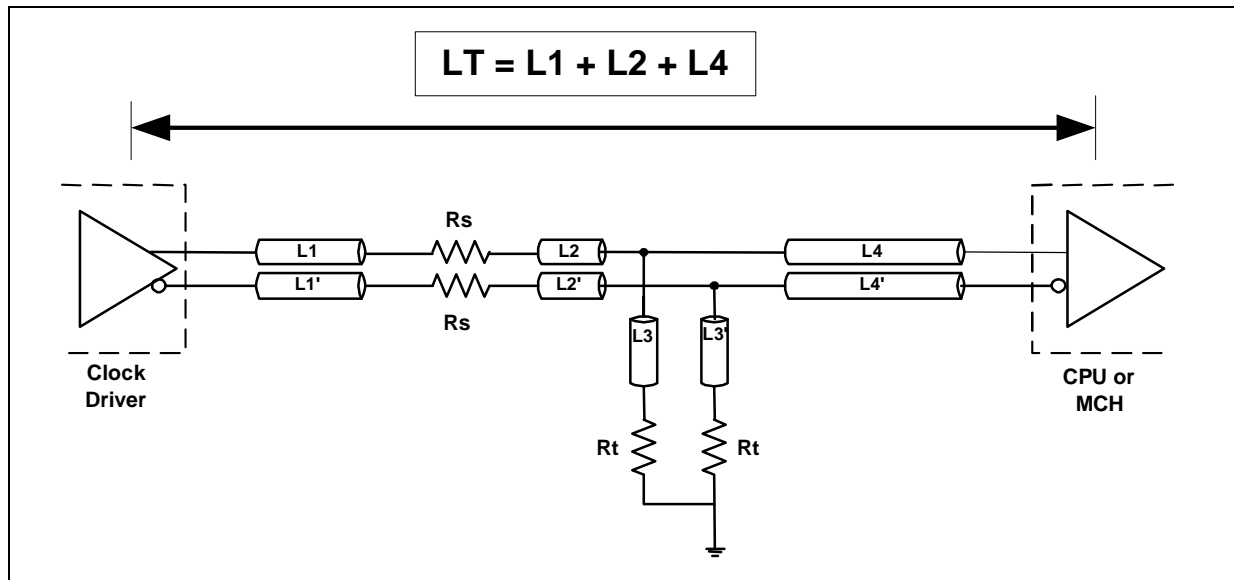
The clock synthesizer provides three sets of 100/133/200 MHz differential clock outputs. The differential clocks are driven to the processor, the E7210 MCH/6300ESB ICH chipset, and the processor's debug ports as shown in [Figure 14](#).



The clock driver differential bus output structure is a “Current Mode Current Steering” output which develops a clock signal by alternately steering a programmable constant current to the external termination resistors “Rt.”

The recommended termination for the differential bus clock is a “Shunt Source Termination.” Refer to [Figure 15](#) for an illustration of this terminology scheme. Parallel Rt resistors perform a dual function, converting the current output of the clock driver to a voltage and matching the driver output impedance to the transmission line. The series resistors “Rs” provide isolation from the clock driver’s output parasitics, which would otherwise appear in parallel with the termination resistor Rt.

**Figure 15. Source Shunt Termination**



The value of Rt should be selected to match the characteristic impedance of the motherboard, and Rs should be 33 Ω. Simulations have shown that Rs values above 33 Ω provide no benefit to signal integrity but only degrade the edge rate.

**Note:** The IREF pin (pin # 41) is connected to ground through a 475 Ω ± 1% resistor – making the IREF 2.32 mA.

For more information on CK409 compliance, refer to the *CK409 Clock Synthesizer/Driver Specification*.

The CK409 allows for different host clock frequencies. The FS\_A and FS\_B pins on the CK409 control the output host clock frequencies. See [Table 9](#) for different CK409 host clock frequency configurations.

**Table 9. Host Clock Frequency Select on CK409**

FS_A	FS_B	Host Clock Frequency
0	0	100 MHz
1	0	133 MHz
0	1	200 MHz

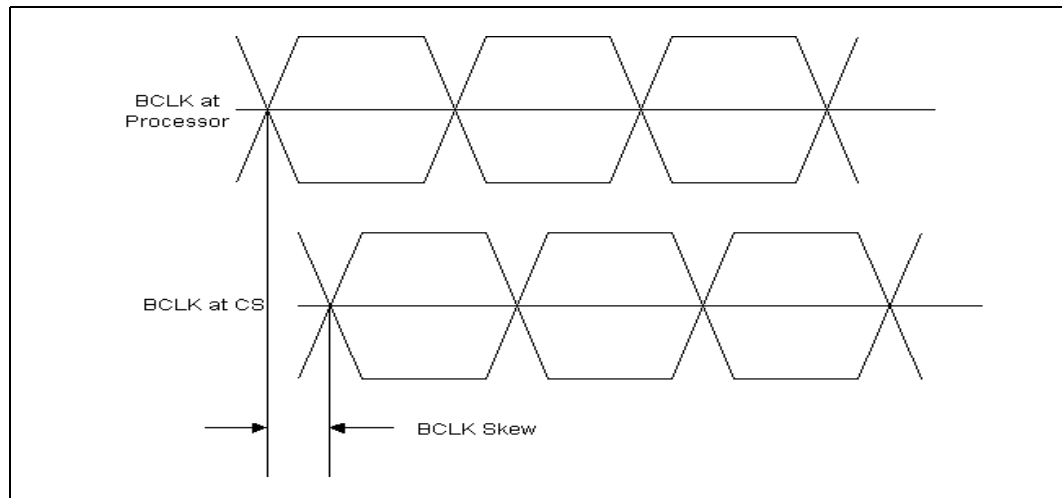
Table 10. HOST\_CLK[1:0]# Routing Guidelines

Layout Guideline	Value	Illustration	Notes
HOST_CLK Skew between Agents	300 ps total budget: 150 ps for clock driver 150 ps for interconnect	Figure 15 and Figure 16	1, 2, 3, 4
Trace Width	5 mils	Figure 17	6
Differential Pair Spacing	11 mils	Figure 10	5, 7
Spacing to Other Traces	25 mils	Figure 17	
Serpentine Spacing	Maintain a minimum 25 mils. Keep parallel serpentine sections as short as possible. Minimize 90-degree bends. Make 45-degree bends if possible.		
Motherboard Impedance – Differential	100 $\Omega$ typical		7
Processor Routing Length – L1, L1': Clock Driver to Rs	0.5 inch max	Figure 15	9
Processor Routing Length – L2, L2': Rs to Rs-Rt Node	0 – 0.2 inch	Figure 15	9
Processor Routing Length – L3, L3': Rs-Rt Node to Rt	0 – 0.2 inch	Figure 15	9
Processor Routing Length – L4, L4': Rs-Rt Node to Load	2 – 15 inches	Figure 15	
MCH Routing Length – L1, L1': Clock Driver to Rs	0.5 inch max	Figure 15	9
MCH Routing Length – L2, L2': Rs to Rs-Rt Node	0 – 0.2 inch	Figure 15	9
MCH Routing Length – L3, L3': Rs-Rt Node to Rt	0 – 0.2 inch	Figure 15	9
MCH Routing Length – L4, L4': Rs-Rt Node to Load	2 – 15 inch	Figure 15	
Processor to MCH Length Matching (LT)	Host clocks to <u>processor</u> should be 150 mils <u>longer</u>	Figure 15	8
HOST_CLK0 – HOST_CLK1 Length Matching	$\pm 10$ mils		
Rs Series Termination Value	33 $\Omega \pm 5\%$	Figure 15	
Rt Shunt Termination Value	49.9 $\Omega \pm 5\%$ (for 50 $\Omega$ odd mode MB impedance)	Figure 15	

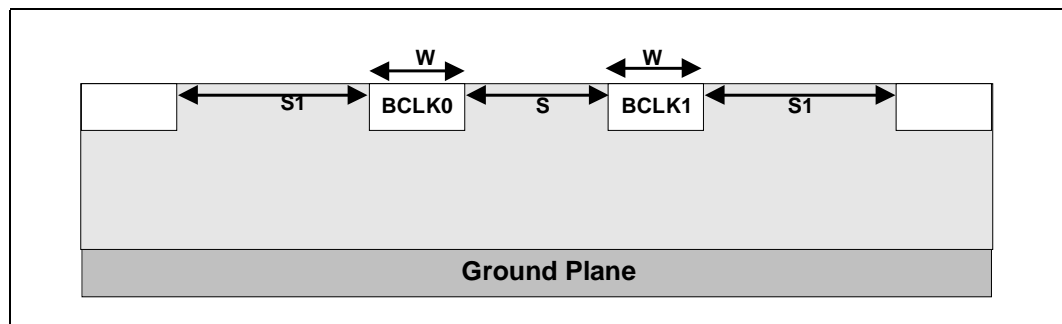
**NOTES:**

1. The skew budget includes clock driver output pair to output pair jitter (differential jitter) and skew, clock skew due to interconnect process variation, and static skew due to layout differences between clocks to all bus agents.
2. This number does not include clock driver common mode (cycle to cycle) jitter or spread spectrum clocking.
3. The interconnect portion of the total budget for this specification assumes clock pairs are routed on multiple routing layers and routed no longer than the maximum recommended lengths.
4. Skew measured at the load between any two-bus agents. Measured at the crossing point.
5. Clock traces are routed in a differential configuration. Maintain the minimum recommended spacing between the two traces of the pair. Uniform spacing should be maintained along the entire length of the trace. Do not exceed the maximum trace spacing, as this will degrade the noise rejection of the network.
6. Set line width to meet correct motherboard impedance. The line width value provided here is a recommendation to meet the proper trace impedance based on the recommended stack up.
7. The differential impedance of each clock pair is approximately  $2 \cdot Z_{\text{single-ended}} \cdot (1 - 2 \cdot K_b)$  where  $K_b$  is the backwards cross-talk coefficient. For the recommended trace spacing,  $K_b$  is very small, and the effective differential impedance is approximately equal to 2 times the single-ended impedance of each half of the pair.
8. The host clocks to the processor must be 150 mils longer than the host clocks to the MCH.
9. Minimize L1, L2 and L3 lengths. Long lengths on L2 and L3 degrade effectiveness of source termination and contribute to ringback.

**Figure 16. Clock Skew As Measured from Agent to Agent**



**Figure 17. Trace Spacing for HOST\_CLK Clocks**



#### 4.1.1.2 BCLK General Routing Guidelines

- When routing the 133/200 MHz selectable differential clocks, do not split up the two halves of a differential clock pair between layers, and route to all agents on the same physical routing layer referenced to ground.
- If a layer transition is required, make sure to do simulations to determine the skew induced by the vias used to transition between routing layers is compensated in the traces to other agents.
- Also, if a layer transition is required, then both clock traces must transition layers so that differential routing is maintained.

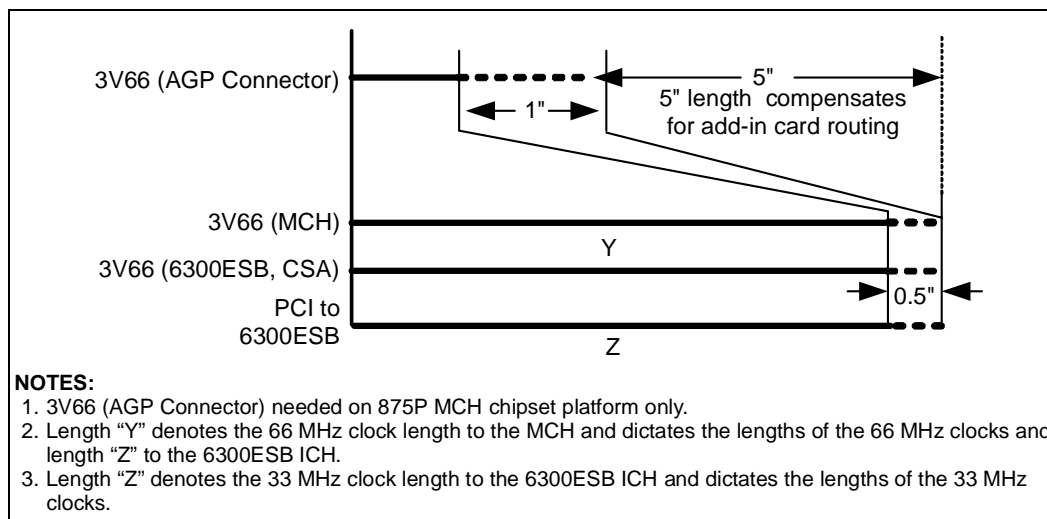
## 4.2 CLK66 and CL33 Clock Groups

### 4.2.1 Length Matching

When routing the 33 MHz and 66 MHz clock group signals, it is important to understand the length matching relationships between all of these signals. Trace length matching is required in each group to help minimize skew and ensure good signal integrity.

### 4.2.1.1 CLK\_66 and 6300ESB ICH CLK\_33 Length Matching

Figure 18. 66 MHz/33 MHz Clock Relationships



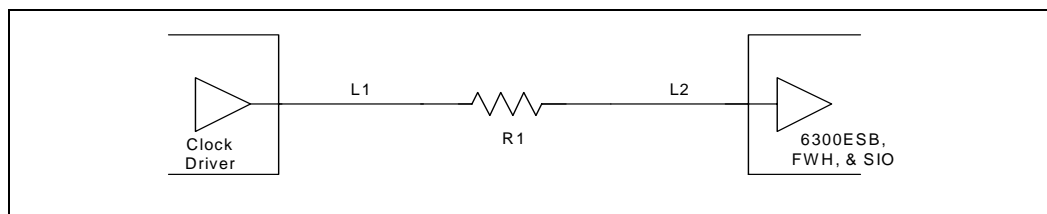
If Y is the length of the 66 MHz clock length to the MCH, then the 66 MHz clocks to CSA, AGP, and 6300ESB ICH, as well as the 33 MHz clock to the 6300ESB ICH (length "Z"), should be length matched to  $Y \pm 0.5$  inches. These lengths are strictly dependent on their clock matching relationships to the MCH. AGP add-in card routing (including connector) reduces motherboard trace length by 5 inches, thus maximum routable mismatch to the AGP connector is  $Y - 5 \pm 0.5$  inches. In addition, designers are allowed up to an additional inch of routing flexibility to meet AGP timing specifications.

Thus, if Y is 9 inches, then CLK\_66 to CSA can be anywhere between 8.5 to 9.5 inches, while CLK\_66 to AGP is routed between 3.5 to 4.5 inches. This minimum length may decrease an additional inch to 2.5 inches based on simulation results.

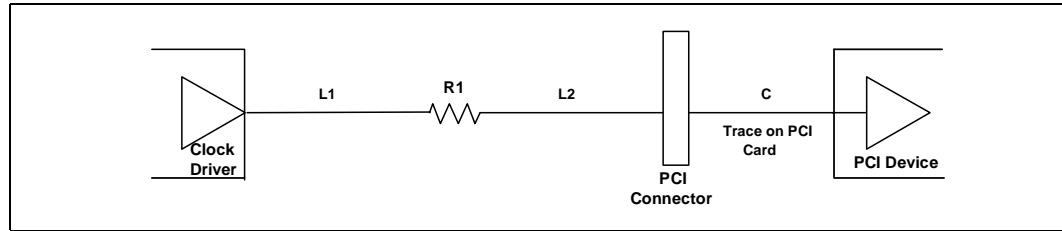
### 4.2.2 TCLK33 Clock Group

For the CLK33 clock group, the driver is the clock synthesizer 33 MHz clock output buffer, and the receiver is the 33 MHz clock input buffer at the various down devices and the PCI slots.

Figure 19. Topology for CLK33 to Down Devices



**Figure 20. Topology for CLK33 to PCI Slot**



**Table 11. CLK33 Routing Guidelines to the 6300ESB ICH, Flash BIOS, SIO, and PCI Slots**

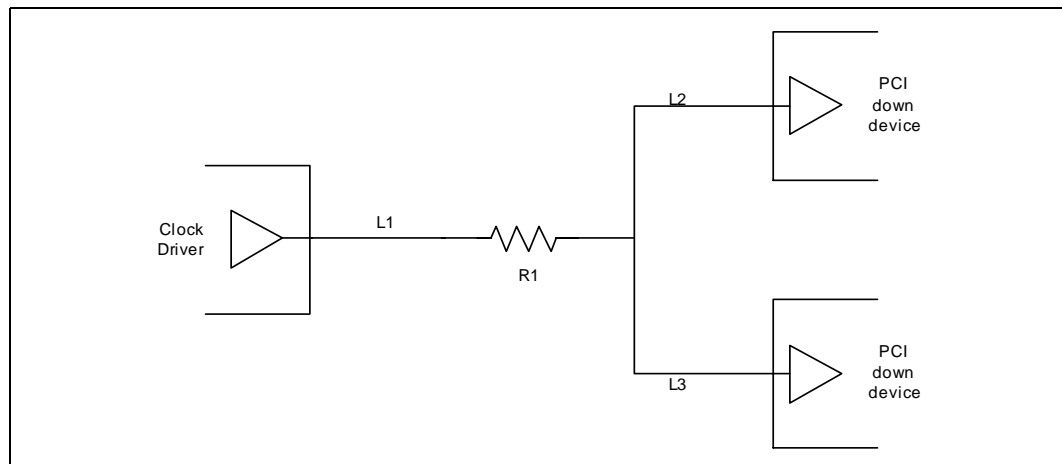
Parameter	Routing Guidelines	Notes
Clock Group	CLK33	
Topology	Point-to-Point	
Reference Plane	Ground referenced (contiguous over entire length)	
Characteristic Trace Impedance ( $Z_0$ )	$60 \Omega \pm 15\%$	
Trace Width	5 mils	
Trace Spacing	10 mils	
6300ESB ICH, Flash BIOS, SIO, PCI slots Trace Length – L1	0 inch to 0.5 inch	
6300ESB ICH – L2	Z; 2 inches to 20 inches	†
Flash BIOS, SIO Trace Length – L2	Z + (0 inch to 10 inches); max length is 20 inches	†
PCI slots Trace Length – L2	Z + (0 inch to 6 inches); max length is 20 inches	†
Resistor	$R1 = 33 \Omega \pm 5\%$	

† Refer to Figure 18 for length of “Z.”

### 4.2.2.1 Sharing 33 MHz Clocks

In some cases the motherboard designer may have a need to share one PCI 33 MHz clock between two PCI down devices. In this case the driver is the clock synthesizer 33 MHz clock output buffer, and the receivers are the 33 MHz clock input buffers of two separate PCI down devices.

**Figure 21. Topology for Sharing CLK33 between Two PCI Down Devices**



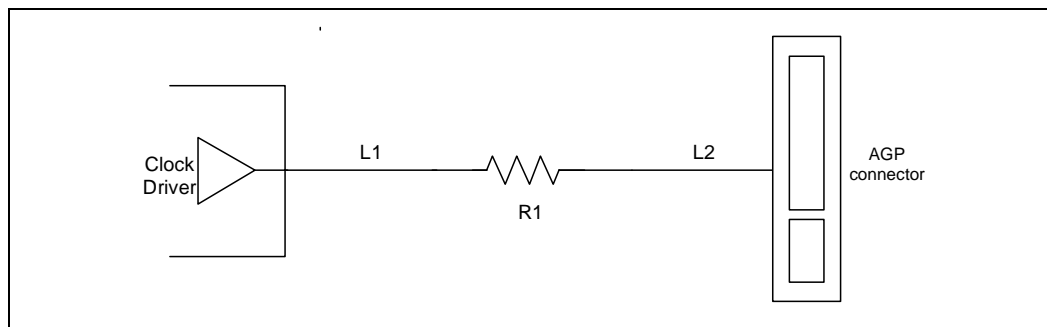
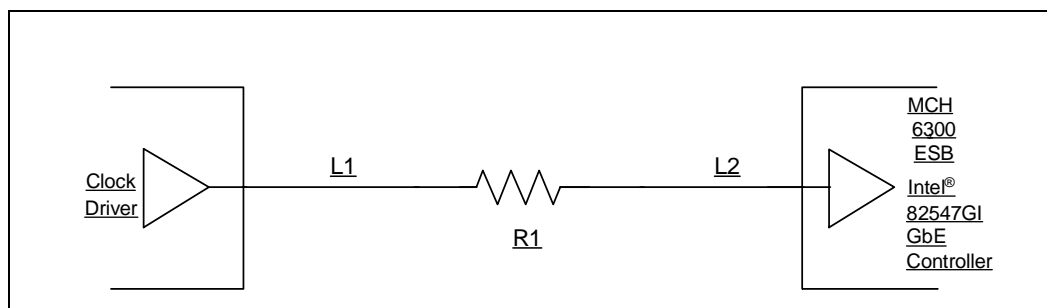
**Table 12. CLK33 Routing Guidelines for Sharing CLK33 Between Two PCI Down Devices**

Parameters	Routing Guidelines
Clock Group	CLK33
Topology	"T"
Reference Plane	Ground referenced (contiguous over entire length)
Characteristic Trace Impedance ( $Z_0$ )	$60 \Omega \pm 15\%$
Trace Width	5 mils
Trace spacing	10 mils
Resistor	$33 \Omega \pm 5\%$
PCI down devices– L1	0 inch to 0.5 inch; max length is 20 inches
PCI down devices – L2 and L3	$Z + (0 \text{ inch to } 7 \text{ inches})$ ; max length is 20 inches. L2 and L3 should be length matched to within 250 mils.

**NOTE:** Length "Z" is the distance from the 33 MHz clock driver to the 6300ESB ICH, 33 MHz input buffer. "Z" may be between 2 and 20 inches long.

### 4.2.3 CLK66 Clock Group

In the CLK66 clock group, the driver is the clock synthesizer 66 MHz clock output buffer, and the receiver is the 66 MHz clock input buffer at the MCH, 6300ESB ICH, the AGP connector, and the 82547GI GbE controller.

**Figure 22. Topology for CLK66 to AGP Connector (Intel® 875P MCH only)****Figure 23. Topology for CLK66 to MCH, ICH, and Intel® 82547GI GbE Controller**

**Table 13. CLK66 Routing Guidelines for CLK66 to MCH, ICH, Intel® 82647GI GbE Controller, and AGP Connector**

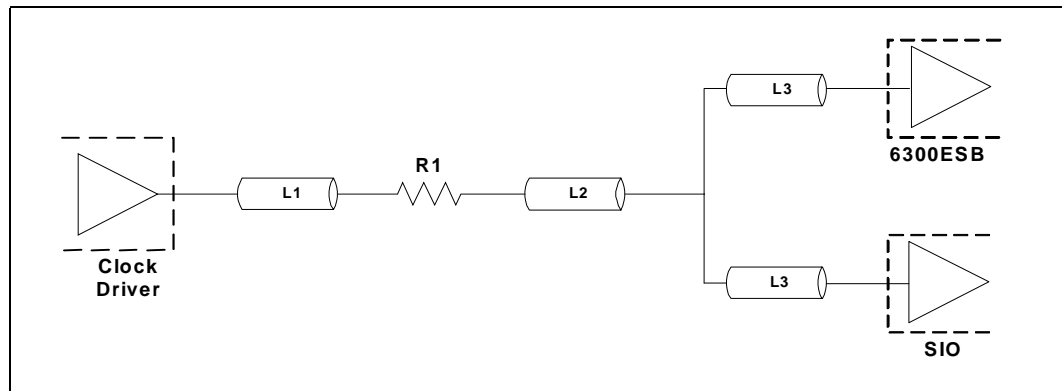
Parameters	Routing Guidelines	Notes
Clock Group	CLK66	
Topology	Point-to-point	
Reference Plane	Ground referenced (contiguous over entire length)	
Characteristic Trace Impedance ( $Z_0$ )	$60 \Omega \pm 15\%$	
Trace Width	5 mils	
Trace spacing	10 mils	
Resistor	$33 \Omega \pm 1\%$	
AGP connector, MCH, 6300ESB ICH, CSA Trace Length – L1	0 inch to 0.5 inch	
Clock Driver to MCH, 6300ESB ICH, and GbE Trace Length – L2	Z - (0.5 inch to 0 inch); max length is 20 inches	†
Clock Driver to AGP connector Trace Length – L2	Z - (6 inches to 5 inches); max length is 20 inches	†

† Length “Z” is the distance from the 33 MHz clock driver to the 6300ESB ICH 33 MHz input buffer. Refer to Figure 18. “Z” may be two inches to 20 inches long.

## 4.2.4 CLK14 Clock Group

The driver in the CLK14 clock group is the clock synthesizer 14.318 MHz clock output buffer, and the receiver is the 14.318 MHz clock input buffer at the 6300ESB ICH and SIO.

**Figure 24. Topology for CLK14**



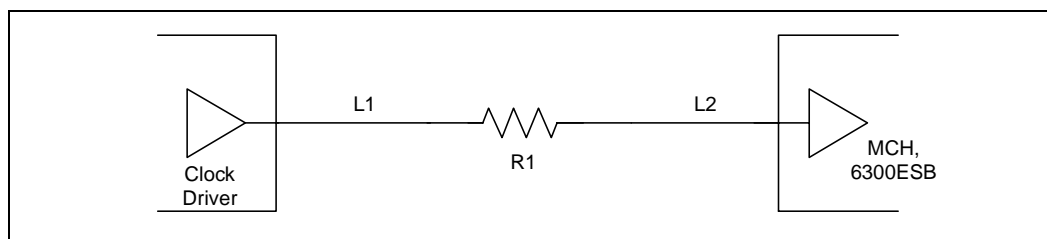
**Table 14. CLK14 Routing Guidelines**

Parameter	Routing Guidelines
Clock Group	CLK14
Topology	Balanced T topology
Reference Plane	Ground referenced (contiguous over entire length)
Characteristic Trace Impedance ( $Z_0$ )	$60 \Omega \pm 15\%$
Trace Width	5 mils
Trace Spacing	10 mils
Trace Length – L1	0 inch to 0.5 inch
Trace Length – L2	0 inch to 12 inches
Trace Length – L3	0 inch to 6 inches
CLK14 total length (L1+L2+L3)	(L1+L2+L3) to 6300ESB ICH must be within 500 mils of (L1+L2+L3) to SIO
Resistor	$33 \Omega \pm 5\%$
Skew Requirements	None

### 4.2.5 USB/DOTCLK Clock Group

For the USBCLK clock group, the driver is the clock synthesizer USB clock output buffer, and the receiver is the USB clock input buffer at the 6300ESB ICH. For the DOTCLK clock group, the driver is the clock synthesizer DOTCLK clock output buffer, and the receiver is the UART clock input buffer at the 6300ESB ICH.

**Note:** This clock is asynchronous to any other clock on the board.

**Figure 25. Topology for USB/DOTCLK**



**Table 15. USB/DOTCLK Routing Guidelines**

Parameter	Routing Guideline
Clock Group	USB/DOTCLK
Topology	Point-to-Point
Reference Plane	Ground referenced (contiguous over entire length)
Characteristic Trace Impedance ( $Z_0$ )	$60\ \Omega \pm 15\%$
Trace Width	5 mils
Trace Spacing	20 mils
Trace Length – L1	0 inch to 0.5 inch
Trace Length – L2	2 inches to 20 inches
Resistor	$R1 = 22\ \Omega \pm 1\%$
Skew Requirements	None – DOTCLK and USBCLK are asynchronous to any other clock on the board
Maximum via Count	2

## 4.2.6 SRC Clock Group

### 4.2.6.1 SRC Clock Topology

The clock synthesizer provides one set of 100 MHz differential clock outputs. The differential clocks are driven to the 6300ESB ICH for Serial ATA as shown in [Figure 14](#).

The clock driver differential bus output structure is a “Current Mode Current Steering” output which develops a clock signal by alternately steering a programmable constant current to the external termination resistors “Rt.”

The recommended termination for the differential bus clock is a “Shunt Source Termination.” Refer to [Figure 26](#) for an illustration of this terminology scheme. Parallel Rt resistors perform a dual function, converting the current output of the clock driver to a voltage and matching the driver output impedance to the transmission line. The series resistors “Rs” provide isolation from the clock driver’s output parasitics, which would otherwise appear in parallel with the termination resistor Rt.

The value of Rt should be  $49\ \Omega$ , and Rs should be  $33\ \Omega$ . Simulations have shown that Rs values above  $33\ \Omega$  provide no benefit to signal integrity but only degrade the edge rate.

Figure 26. Source Shunt Termination

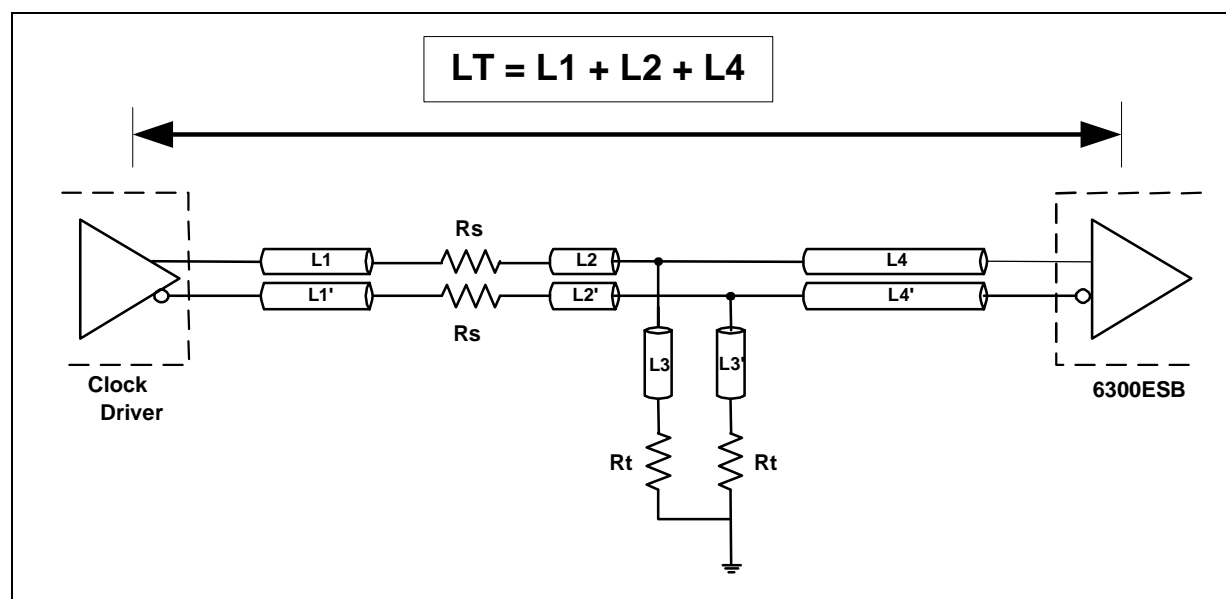


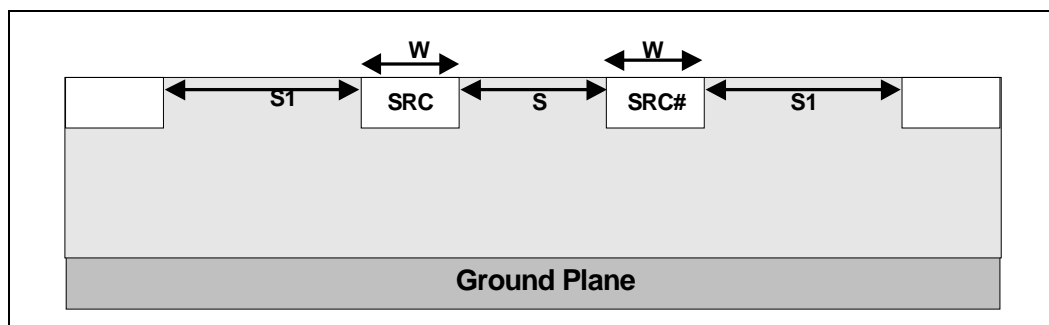
Table 16. SCR/SCR# Routing Guidelines

Layout Guideline	Value	Illustration	Notes
Trace Width	5 mil	Figure 27	
Differential Pair Spacing	11 mils	Figure 27	1, 2, 3
Spacing to Other Traces	25 mils	Figure 27	
Serpentine Spacing	Maintain a minimum 25 mils. Keep parallel serpentine sections as short as possible. Minimize 90 degree bends. Make 45 degree bends, if possible.		
Motherboard Impedance – Differential	100 $\Omega$ typical		4
Routing Length – L1, L1': Clock Driver to Rs	0.5 inch max	Figure 26	6, 7
Routing Length – L2, L2': Rs to Rs-Rt Node	0 – 0.2 inch	Figure 26	6, 7
Routing Length – L3, L3': Rs-Rt Node to Rt	0 – 0.2 inch	Figure 26	6, 7
Routing Length – L4, L4': Rs-Rt Node to Load	2 – 15 inches	Figure 26	
SCR – SCR# Length Matching	$\pm 10$ mils		
Rs Series Termination Value	33 $\Omega \pm 5\%$	Figure 26	
Rt Shunt Termination Value	49.9 $\Omega \pm 1\%$ (for 50 $\Omega$ odd mode MB impedance)	Figure 26	5

**NOTES:**

- Edge-to-edge spacing between the two traces of any differential pair. Uniform spacing should be maintained along the entire length of the trace.
- Clock traces are routed in a differential configuration. Maintain the minimum recommended spacing between the two traces of the pair. Do not exceed the maximum trace spacing, as this will degrade the noise rejection of the network.
- Set line width to meet correct motherboard impedance. The line width value provided here is a recommendation to meet the proper trace impedance based on the recommended stack up.
- The differential impedance of each clock pair is approximately  $2 \cdot Z_{\text{single-ended}} \cdot (1 - 2 \cdot K_b)$ , where  $K_b$  is the backwards cross-talk coefficient. For the recommended trace spacing,  $K_b$  is very small, and the effective differential impedance is approximately equal to twice the single-ended impedance of each half of the pair.
- Rt shunt termination value should match the motherboard impedance.
- Minimize L1, L2 and L3 lengths. Long lengths on L2 and L3 degrade effectiveness of source termination and contribute to ringback.
- The goal of constraining all bus clocks to one physical routing layer is to minimize the impact on skew due to variations in  $E_r$  and the impedance variations due to physical tolerances of circuit board material.

Figure 27. Trace Spacing for SRC Clocks



#### 4.2.6.2 SRC General Routing Guidelines

- When routing the 100 MHz differential clocks, do not split up the two halves of a differential clock pair between layers, and route to all agents on the same physical routing layer referenced to ground.
- If a layer transition is required, make sure skew induced by the vias used to transition between routing layers is compensated in the traces to other agents.
- Do not place vias between adjacent complementary clock traces, and avoid differential vias. Vias placed in one half of a differential pair must be matched by a via in the other half. Differential vias may be placed within length L1, between clock driver and Rs, if needed to shorten length L1.

### 4.3 Clock Driver Decoupling

- For **all** power connection to planes, decoupling capacitors, and vias, the **maximum** trace width allowable and shortest possible lengths should be used to ensure lowest possible inductance.
- The VSS pins should not be connected directly to the VSS side of the capacitors. They should be connected to the ground flood under the part which is viaed to the ground plane in order to avoid VDD glitches propagating out, getting coupled through the decoupling capacitors to the VSS pins. This method has been shown to provide the best clock performance.
- The ground flood should be viaed through the ground plane with no less than 12-16 vias under the part. It should be well connected.
- For all power connections, heavy duty and/or dual vias should be used.
- It is imperative that the standard signal vias and small traces not be used for connecting decoupling capacitors and ground floods to the power or ground planes.

#### 4.3.1 CK409 Power Plane Filtering

##### 4.3.1.1 VDD Plane Filtering

The VDD decoupling requirements for a CK409 compliant clock synthesizer are as follows:

- One 300  $\Omega$  (100 MHz) ferrite bead is recommended for the VDD plane.

- 10  $\mu$ F of bulk decoupling capacitance in a 1206 package placed close to the VDD generation circuitry is recommended for the VDD plane. Two 4.7  $\mu$ F capacitors may also be used in place of the 10  $\mu$ F capacitor.
- Seven 0.1  $\mu$ F high-frequency decoupling capacitors in the 0603 packages should be placed as close as possible to each VDD pin.

#### 4.3.1.2 VDDA Plane Filtering

The VDDA decoupling requirements for a CK-409 compliant clock synthesizer are as follows:

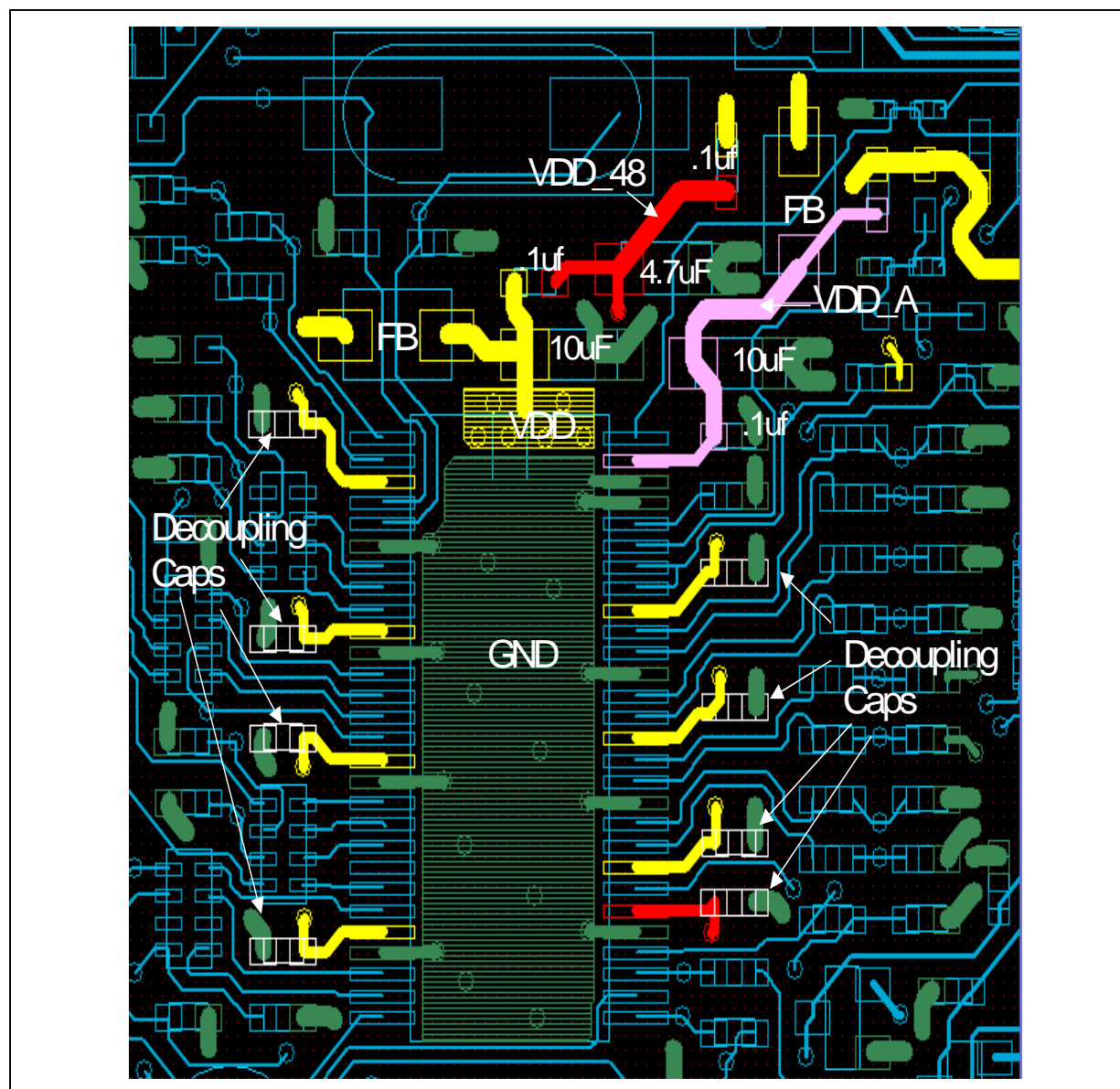
- One 300  $\Omega$  (100 MHz) ferrite bead is recommended for the VDDA plane.
- 10  $\mu$ F of bulk decoupling capacitance in a 1206 package placed close to the VDDA generation circuitry is recommended for the VDDA plane. Two 4.7  $\mu$ F capacitors may also be used in place of the 10  $\mu$ F capacitor.
- One 0.1  $\mu$ F high-frequency decoupling capacitor in the 0603 package should be placed as close as possible to each VDDA pin.

#### 4.3.1.3 VDD\_48 Plane Filtering

The VDD\_48 decoupling requirements for a CK-409 compliant clock synthesizer are as follows:

- One 5  $\Omega$  series resistor is recommended for the VDD\_48 plane.
- One 4.7  $\mu$ F of bulk decoupling capacitance in a 1206 package placed close to the VDD\_48 generation circuitry is recommended for the VDD\_48 plane.
- One 0.1  $\mu$ F high-frequency decoupling capacitor in the 0603 package should be placed as close as possible to each VDD\_48 pin.

Figure 28. Decoupling Capacitor Placement and Connectivity



## 4.4 EMI Constraints

Clocks are a significant contributor to EMI. The following recommendations may aid in EMI reduction:

- Maintain uniform spacing between the two halves of differential clocks.
- Route clocks on physical layer adjacent to the VSS reference plane only.

# Front Side Bus (FSB)

# 5

## 5.1 General Topologies and Layout Guidelines

**Caution:** All signals in this section are assumed to be routed microstrip. If you choose to route on inner layers, you must perform thorough signal integrity and timing simulations on each design.

This section covers the FSB source synchronous (data, address, and associated strobes) and common clock signal routing for platforms based on the Pentium 4 processor/Pentium 4 Processor with HT Technology<sup>†</sup> and the 875P MCH/E7210 MCH/6300ESB ICH chipset. Table 17 lists the signals and their corresponding signal types.

**Table 17. System Bus Signal Groups (Sheet 1 of 2)**

Signal Group	Type	Signals <sup>1</sup>														
AGTL+ Common Clock Input	Synchronous to BCLK[1:0]	BPRI#, DEFER#, RESET# <sup>3, 5</sup> , RS[2:0]#, RSP#, TRDY#														
AGTL+ Common Clock I/O	Synchronous to BCLK[1:0]	AP[1:0]#, ADS#, BINIT#, BNR#, BPM[5:0]# <sup>3, 5</sup> , BR0# <sup>3</sup> , DBSY#, DP[3:0]#, DRDY#, HIT#, HITM#, LOCK#, MCERR#														
AGTL+ Source Synchronous I/O	Synchronous to associated strobe	<table><tr><th>Signals</th><th>Associated Strobe</th></tr><tr><td>REQ[4:0]#, A[16:3]#<sup>4</sup></td><td>ADSTB0#</td></tr><tr><td>A[35:17]#<sup>4</sup></td><td>ADSTB1#</td></tr><tr><td>D[15:0]#, DBI0#</td><td>DSTBP0#, DSTBN0#</td></tr><tr><td>D[31:16]#, DBI1#</td><td>DSTBP1#, DSTBN1#</td></tr><tr><td>D[47:32]#, DBI2#</td><td>DSTBP2#, DSTBN2#</td></tr><tr><td>D[63:48]#, DBI3#</td><td>DSTBP3#, DSTBN3#</td></tr></table>	Signals	Associated Strobe	REQ[4:0]#, A[16:3]# <sup>4</sup>	ADSTB0#	A[35:17]# <sup>4</sup>	ADSTB1#	D[15:0]#, DBI0#	DSTBP0#, DSTBN0#	D[31:16]#, DBI1#	DSTBP1#, DSTBN1#	D[47:32]#, DBI2#	DSTBP2#, DSTBN2#	D[63:48]#, DBI3#	DSTBP3#, DSTBN3#
Signals	Associated Strobe															
REQ[4:0]#, A[16:3]# <sup>4</sup>	ADSTB0#															
A[35:17]# <sup>4</sup>	ADSTB1#															
D[15:0]#, DBI0#	DSTBP0#, DSTBN0#															
D[31:16]#, DBI1#	DSTBP1#, DSTBN1#															
D[47:32]#, DBI2#	DSTBP2#, DSTBN2#															
D[63:48]#, DBI3#	DSTBP3#, DSTBN3#															
AGTL+ Strobes	Synchronous to BCLK[1:0]	ADSTB[1:0]#, DSTBP[3:0]#, DSTBN[3:0]#														
Asynchronous GTL+ Input <sup>3</sup>		A20M#, IGNNE#, INIT#, LINT0/INTR, LINT1/NMI, SMI#, SLP#, STPCLK#														
Asynchronous GTL+ Output <sup>3</sup>		FERR#, IERR#, THERMTRIP# <sup>5</sup>														
Asynchronous GTL+ Input/Output		PROCHOT#														
TAP Input <sup>3</sup>	Synchronous to TCK	TCK, TDI, TMS, TRST#														

**NOTES:**

1. Refer to the *Intel 875P Memory Controller Hub (MCH) Datasheet* and the *Intel E7210 Memory Controller Hub (MCH) Datasheet* for signal descriptions.
2. In processor systems where there is no debug port implemented on the system board, these signals are used to support a debug port interposer. In systems with the debug port implemented on the system board, these signals are no connects.
3. These signal groups are not terminated by the processor. Refer to the *Intel Pentium 4 Processor with HT Technology Debug Port Design Guide*, and Section 5.1.6 for termination requirements and further details.
4. The value of these pins during the active-to-inactive edge of RESET# defines the processor configuration options. For details refer to the *Intel Pentium 4 Processor with HT Technology Electrical, Mechanical, and Thermal Specifications*.
5. These signals do not have R<sub>L</sub> termination on die.

Table 17. System Bus Signal Groups (Sheet 2 of 2)

Signal Group	Type	Signals <sup>1</sup>
TAP Output <sup>3</sup>	Synchronous to TCK	TDO <sup>5</sup>
System Bus Clock	Clock	BCLK[1:0], ITP_CLK[1:0] <sup>2</sup>
Power/Other		VCC, VCCA, VCCIOPLL, VID[5:0], V <sub>SS</sub> , VSSA, GTLREF[3:0], COMP[1:0], RESERVED, TESTHI[12:0], THERMDA, THERMDC, VCC_SENSE, VSS_SENSE, VCCVID, VCCVIDLB, BSEL[1:0], SKTOCC#, DBR# <sup>2</sup> , VIDPWRGD, BOOTSELECT, OPTIMIZED/COMPAT# <sup>3</sup> , PWRGOOD <sup>3, 5</sup>

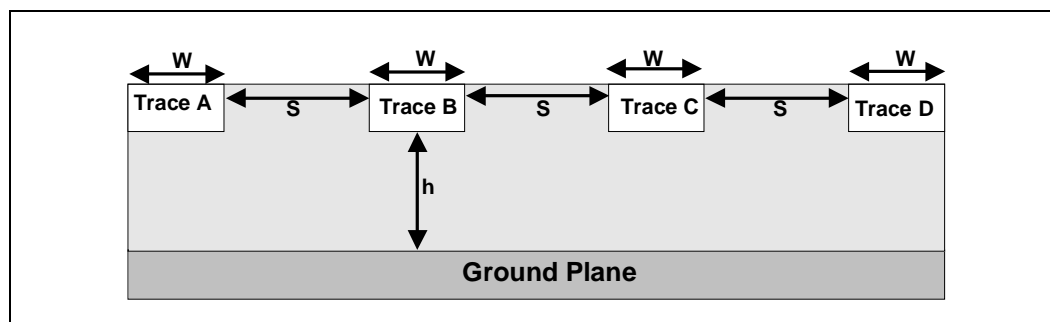
**NOTES:**

1. Refer to the *Intel 875P Memory Controller Hub (MCH) Datasheet* and the *Intel E7210 Memory Controller Hub (MCH) Datasheet* for signal descriptions.
2. In processor systems where there is no debug port implemented on the system board, these signals are used to support a debug port interposer. In systems with the debug port implemented on the system board, these signals are no connects.
3. These signal groups are not terminated by the processor. Refer to the *Intel Pentium 4 Processor with HT Technology Debug Port Design Guide*, and [Section 5.1.6](#) for termination requirements and further details.
4. The value of these pins during the active-to-inactive edge of RESET# defines the processor configuration options. For details refer to the *Intel Pentium 4 Processor with HT Technology Electrical, Mechanical, and Thermal Specifications*.
5. These signals do not have R<sub>L</sub> termination on die.

### 5.1.1 Trace Spacing Rules

The spacing rules are based upon board stack-up and dielectric thickness, not on trace width. A 3:1 spacing rule corresponding to the air gap (distance S) between traces must be three times the distance from the trace to the ground plane (distance h). For instance, if the dielectric thickness was 4.1 mils, and the trace space guidelines calls for 3:1 spacing, the air gap between traces must be 12.3 mils.

Figure 29. Spacing Diagram



### 5.1.2 Signal Groups

This section covers the AGTL+ system bus 1X, 2X, and 4X signals as well as their associated strobe pairs.

Table 18. 1X, 2X, and 4X Signal Groups

1X	2X Group	4X Group
BPRI#, DEFER#, RS[2:0]#, TRDY#, ADS#, BNR#, DBSY, DRDY#, HIT#, HITM#, LOCK#	A[31:3]#, REQ[4:0]#, ADSTB[1:0]#	D[63:0]#, DSTBP[3:0]#, DSTBN[3:0]#, DBI[3:0]#



**Table 19. Address and Data, and Associated Strobe Pairs**

Data/Address Group	Associated Strobes
D[63:48]#, DBI3#	DSTBP3#, DSTBN3#
D[47:32]#, DBI2#	DSTBP2#, DSTBN2#
D[31:16]#, DBI1#	DSTBP1#, DSTBN1#
D[15:0]#, DBI0#	DSTBP0#, DSTBN0#
A[31:17]#	ASTB1#
A[16:3]#, REQ[4:0]#	ASTB0#

### 5.1.3 Motherboard Layout Rules for AGTL+ Signals

The following topologies and layout guidelines are preliminary and are subject to change. These guidelines are derived from simulations with the processor and 875P MCH and the E7210 MCH package models. All lengths are pin to pin lengths, but length matching must be pad to pad.

#### 5.1.3.1 4X Routing Guidelines

**Table 20. 4X Routing Guidelines**

Signal Name	Spacing	Length	Referencing	Topology	Impedance	Matching	Notes
D[63:0]#	3:1	2.5" to 6"	VSS	1	60 $\Omega \pm 15\%$	$\pm 25$ mils	2, 3, 4, 5
DSTBP[3:0]#	4:1	2.5" to 6"	VSS	1	60 $\Omega \pm 15\%$	$\pm 25$ mils	1, 2, 3, 4
DSTBN[3:0]#	4:1	2.5" to 6"	VSS	1	60 $\Omega \pm 15\%$	$\pm 25$ mils	1, 2, 3, 4
DBI[3:0]#	3:1	2.5" to 6"	VSS	1	60 $\Omega \pm 15\%$	$\pm 25$ mils	2, 3, 5

**NOTES:**

1. DSTBP[3:0]# and DSTBN[3:0]# must **not** be routed adjacent to each other and must have 4:1 spacing.
2. All signal groups within the 4X data group must be routed on the same layer.
3. Length matching must include motherboard compensation for MCH and CPU package trace lengths.
4. Strobe length matching:  $\text{Length\_DSTBPx} = \text{Length\_DSTBNx} \pm 25$  mils.
5. Data to strobe length matching:  $\text{Length\_data} = (\text{Length\_DSTBPx} + \text{Length\_DSTBNx})/2 \pm 25$ .

#### 5.1.3.2 2X Routing Guidelines

**Note:** To ensure clean breakout and routing from the MCH to CPU for the signal groups in [Table 21](#), these signals are allowed to transition layers and route for up to 750 mils maximum length, at which point the signal must transition back to the original layer or connect to the MCH or CPU pin.

Table 21. 2X Routing Guidelines

Signal Name	Spacing	Length	Referencing	Topology	Impedance	Matching	Notes
A[31:3]#	3:1	3" to 10"	VSS	1	60 $\Omega \pm 15\%$	$\pm 100$ mils	2, 3
ADSTB[1:0]#	4:1	3" to 10"	VSS	1	60 $\Omega \pm 15\%$	N/A	1, 2, 3
REQ[4:0]#	3:1	3" to 10"	VSS	1	60 $\Omega \pm 15\%$	$\pm 100$ mils	2, 3

**NOTES:**

1. ADSTB[1:0]# must be routed 4:1.
2. Length matching must include motherboard compensation for package trace lengths.
3. Address to strobe length matching: Length\_address = Length\_ADSTB  $\pm 100$ .

## 5.1.3.3 1X Routing Guidelines

Table 22. 1X Routing Guidelines

Signal Name	Spacing	Length	Referencing	Topology	Impedance	Notes
BPRI#	3:1	3" to 8"	VSS	1	60 $\Omega \pm 15\%$	1, 2
DEFER#	3:1	3" to 8"	VSS	1	60 $\Omega \pm 15\%$	1, 2
RS[2:0]#	3:1	3" to 8"	VSS	1	60 $\Omega \pm 15\%$	1, 2
TRDY#	3:1	3" to 8"	VSS	1	60 $\Omega \pm 15\%$	1, 2
ADS#	3:1	3" to 8"	VSS	1	60 $\Omega \pm 15\%$	1, 2
BNR#	3:1	3" to 8"	VSS	1	60 $\Omega \pm 15\%$	1, 2
DBSY#	3:1	3" to 8"	VSS	1	60 $\Omega \pm 15\%$	1, 2
DRDY#	3:1	3" to 8"	VSS	1	60 $\Omega \pm 15\%$	1, 2
HIT#	3:1	3" to 8"	VSS	1	60 $\Omega \pm 15\%$	1, 2
HITM#	3:1	3" to 8"	VSS	1	60 $\Omega \pm 15\%$	1, 2
LOCK#	3:1	3" to 8"	VSS	1	60 $\Omega \pm 15\%$	1, 2

**NOTES:**

1. 3:1 spacing is the minimum requirement; 4:1 spacing is preferred, if achievable.
2. For routes 7 inches to 8 inches, 4:1 spacing is required.

## 5.1.3.4 Ground Referencing and Reference Plane Splits

It is strongly recommended that AGTL+ signals be routed on a signal layer which is next to the ground layer (referenced to ground). It is important to provide effective signal return paths with low inductance. The best routing is directly adjacent to a solid ground plane with no splits or cuts.

Splits in reference planes disrupt signal return paths and increase overshoot, undershoot, and ring-back due to significantly increased inductance. This is very hard to predict and suppress, thus, such plane splits under AGTL+ signals should be avoided.

## 5.1.4 Motherboard Layout Rules for Async AGTL+ Signals

For all Asynchronous AGTL+ signals, routing may be done on any layer or combination of layers. [Table 23](#) provides insight for routing these signals, but [Section 5.1.6](#) further details the routing topologies and layout requirements.

**Table 23. Routing Guidelines for Asynchronous AGTL+ Signals**

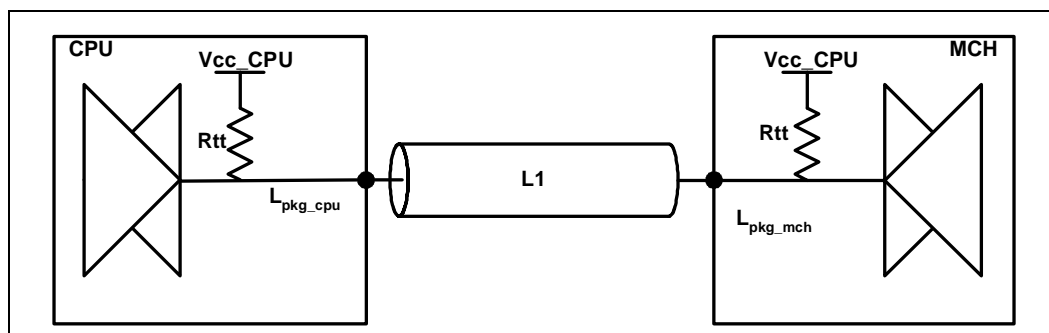
Signal	Impedance	Spacing	Trace Width	Topology
THERMTRIP#	60 $\Omega \pm 15\%$	7 mils	5 mils	2
FERR#	60 $\Omega \pm 15\%$	7 mils	5 mils	2
A20M#	60 $\Omega \pm 15\%$	7 mils	5 mils	3
IGNNE#	60 $\Omega \pm 15\%$	7 mils	5 mils	3
SMI#	60 $\Omega \pm 15\%$	7 mils	5 mils	3
SLP#	60 $\Omega \pm 15\%$	7 mils	5 mils	3
STPCLK#	60 $\Omega \pm 15\%$	7 mils	5 mils	3
LINT[1:0]	60 $\Omega \pm 15\%$	7 mils	5 mils	3
IERR#	60 $\Omega \pm 15\%$	7 mils	5 mils	4
BR0#	60 $\Omega \pm 15\%$	13 mils	5 mils	5
RESET#	60 $\Omega \pm 15\%$	13 mils	5 mils	5
INIT#	60 $\Omega \pm 15\%$	7 mils	5 mils	6
PWRGOOD	60 $\Omega \pm 15\%$	13 mils	5 mils	7
PROCHOT#	60 $\Omega \pm 15\%$	7 mils	5 mils	8
TESTHI	60 $\Omega \pm 15\%$	7 mils	5 mils	9
COMP[1:0]	60 $\Omega \pm 15\%$	13 mils	5 mils	10
BOOTSELECT	60 $\Omega \pm 15\%$	7 mils	5 mils	11
RESERVED	NA	NA	NA	12
OPTIMIZED/COMPAT#	NA	NA	NA	13
RSP#	NA	NA	NA	13

## 5.1.5 AGTL+ Layout Topologies

### 5.1.5.1 Topology 1

Topology 1 requires that the signals be routed directly from the CPU to the chipset. Both the CPU and the chipset have on-die termination (ODT), which removes the need for termination resistors on the motherboard. Thus, the signal is dual-end terminated. The allowable break-in and breakout region for AGTL+ signals is 500 mils at 5 mil traces with 5 mil separation. Figure 30 illustrates the recommended topology.

Figure 30. Topology 1



## 5.1.6 Non-AGTL+ Topologies

### 5.1.6.1 Topology 2: THERMTRIP# and FERR#

These signals adhere to the following routing and layout recommendations. Figure 31 illustrates the recommended topology. If THERMTRIP# is routed to external logic, voltage translation may be required to avoid excessive voltage levels at the processor and to meet input thresholds for the external logic.

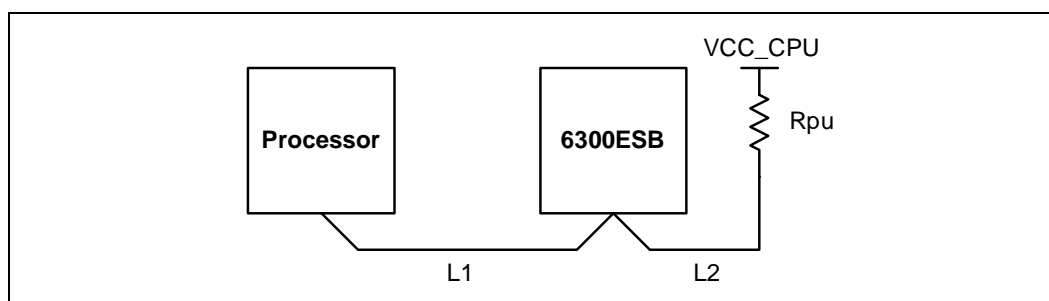
Table 24. Layout Recommendations for FERR# and THERMTRIP#

Trace $Z_0$	Trace Spacing	L1	L2	Rpu
60 $\Omega \pm 15\%$	7 mils	1 inch to 12 inches	3 inches maximum	62 $\Omega \pm 5\%$

**NOTES:**

1. THERMTRIP# may be routed next to FERR# with 5 mil spacing for up to 17 inches.
2. THERMTRIP# or FERR# cannot be routed next to any other signal for more than 8 inches at 7 mil spacing.

Figure 31. Routing Illustration for FERR# and THERMTRIP#



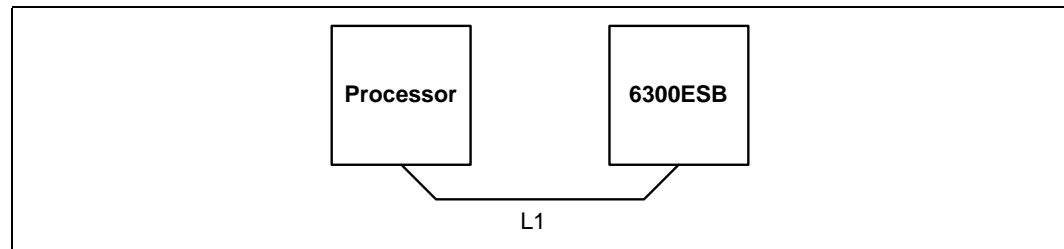
### 5.1.6.2 Topology 3: A20M#, IGNNE#, SMI#, SLP#, STPCLK#, and LINT[1:0]

These signals adhere to the following routing and layout recommendations. Figure 32 illustrates the recommended topology.

**Table 25. Layout Recommendations for Miscellaneous Signals**

Trace $Z_0$	Trace Spacing	L1
$60\ \Omega \pm 15\%$	7 mils	17 inches maximum

**Figure 32. Routing Illustration for A20M#, IGNNE#, SMI#, SLP#, STPCLK#, and LINT[1:0]**



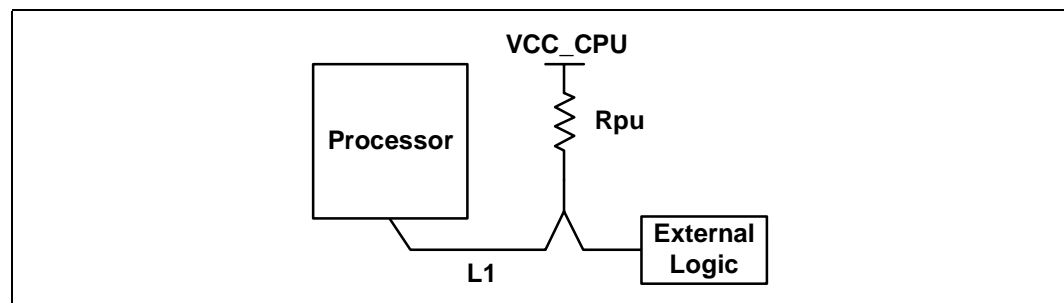
### 5.1.6.3 Topology 4: IERR#

The IERR# signal does not have on-die termination and must be terminated if it is used. If the signal is not used then it may be left as a no connect. Figure 33 illustrates the recommended topology if the pin is used.

**Table 26. Layout Recommendations for IERR#**

Trace $Z_0$	Trace Spacing	L1	Rpu
$60\ \Omega \pm 15\%$	7 mils	1 inch maximum	$62\ \Omega \pm 5\%$

**Figure 33. Routing Illustration for IERR#**



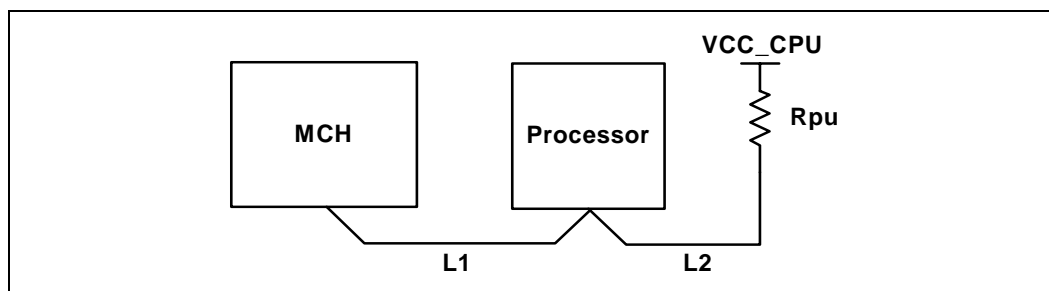
### 5.1.6.4 Topology 5: RESET# and BR0#

Since the processor does not have on-die termination on the RESET# or BR0# signals, it is necessary to terminate them using discrete components on the system board. Connect the signals between the 875P MCH and the processor as shown in Figure 34.

**Table 27. Layout Recommendations for RESET# and BR0#**

Pin Name	Trace $Z_0$	Trace Spacing	L1	L2	Rpu
RESET#	$60\ \Omega \pm 15\%$	13 mils	2" to 10"	1" to 2"	$62\ \Omega \pm 5\%$
BR0#	$60\ \Omega \pm 15\%$	13 mils	2" to 10"	1" to 2"	$200\ \Omega \pm 5\%$

**NOTE:** BR0# may be routed with 7 mil spacing for up to 8 inches.

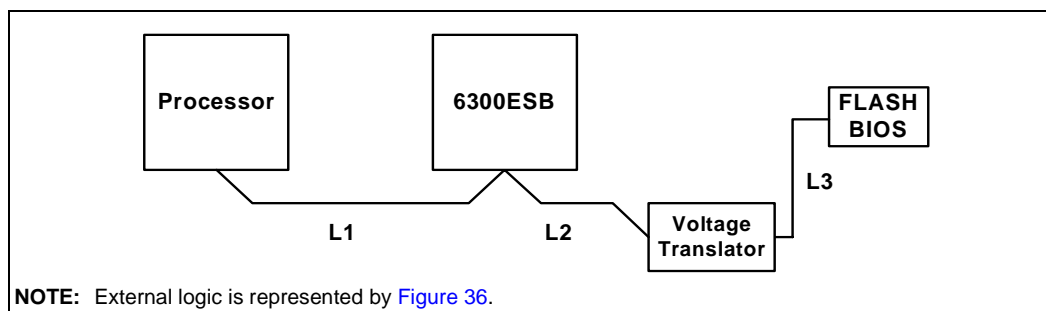
**Figure 34. Routing Illustration for RESET# and BR0#**

### 5.1.6.5 Topology 6: INIT#

The INIT# signal adheres to the following routing and layout recommendations. [Figure 35](#) illustrates the recommended topology.

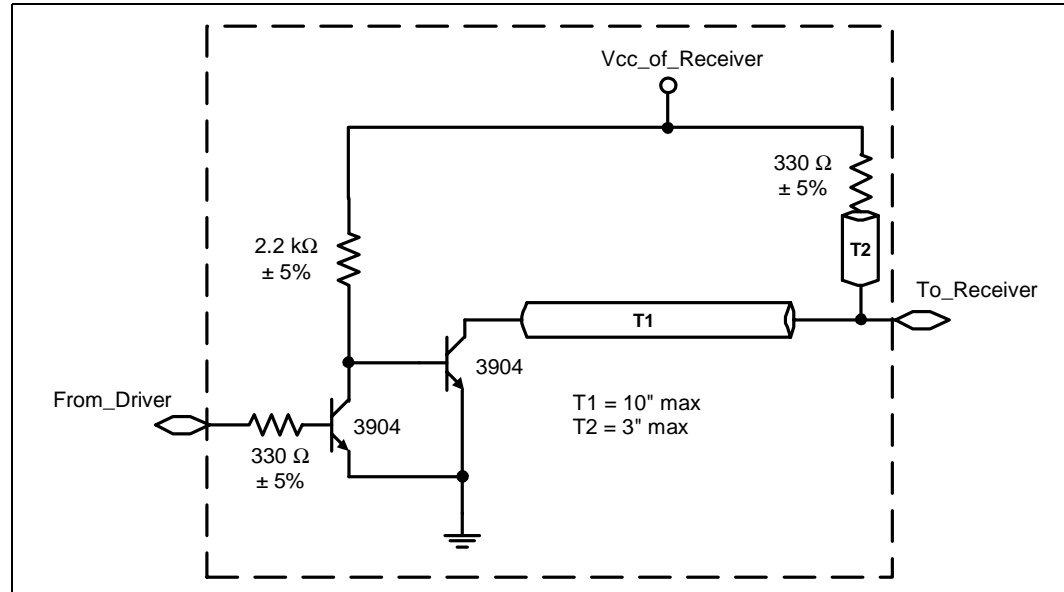
**Table 28. Layout Recommendations For INIT#**

Trace $Z_0$	Trace Spacing	L1	L2	L3
$60\ \Omega \pm 15\%$	7 mils	17" maximum	2" maximum	10" maximum

**Figure 35. INIT# Topology**

Level shifting is required for the INIT# signals to the flash BIOS in order to meet the input logic levels of the flash BIOS. Figure 36, below, illustrates one method of implementing this.

**Figure 36. Voltage Translation of INIT#**



#### 5.1.6.6 Topology 7: PWRGOOD

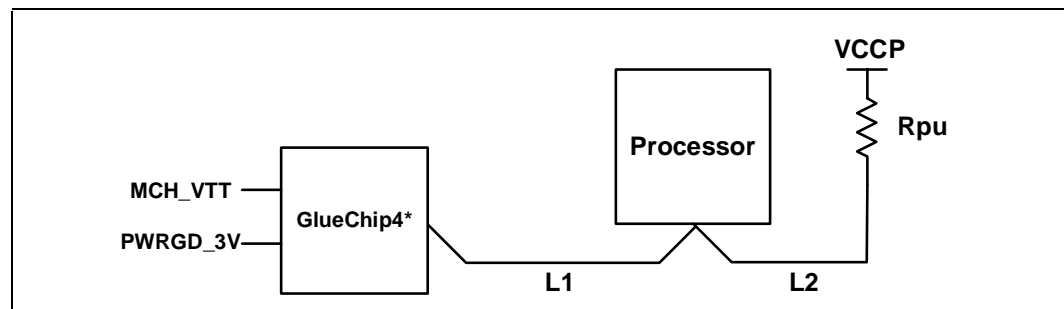
The PWRGOOD signal must be asserted to the CPU after the CPU voltage regulator, MCH and 6300ESB ICH power supplies have stabilized. The following is the solution used on the customer reference board using an ATX\* power supply and a Glue Chip 4\* device. The MCH\_VTT and PWRGD\_3V signals are ANDed together using the NAND gate and inverter on the Glue Chip 4 device to create the CPU PWRGOOD signal.

Figure 37 illustrates the recommended topology.

**Table 29. Layout Recommendations for PWRGOOD**

Trace $Z_0$	Trace Spacing	L1	L2	Rpu
$60\ \Omega \pm 15\%$	13 mils	1" to 12"	3" maximum	$300\ \Omega \pm 5\%$

**Figure 37. Routing Illustration for PWRGOOD**



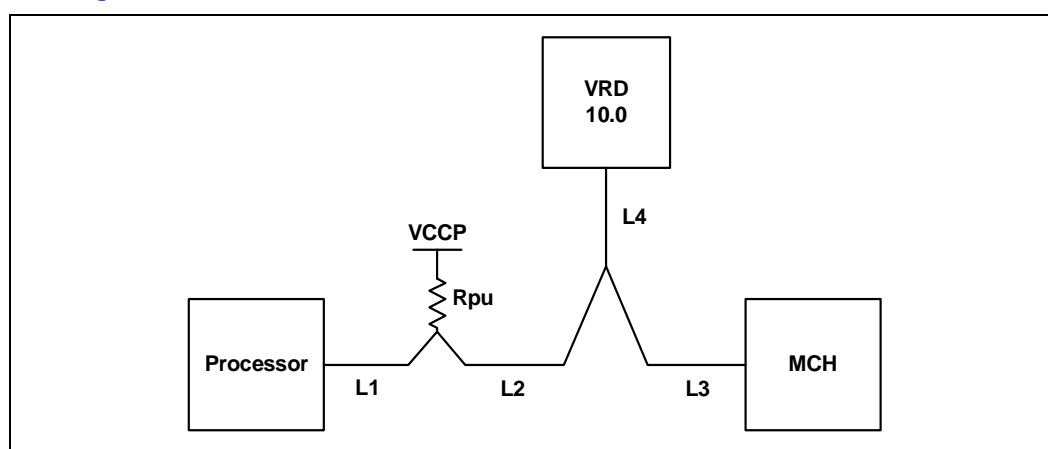
### 5.1.6.7 Topology 8: PROCHOT#

PROCHOT# adheres to the following routing and layout recommendations. Figure 38 illustrates the recommended topology. If PROCHOT# is routed to external logic, voltage translation may be required to avoid excessive voltage levels at the processor and to meet input thresholds for external logic.

**Table 30. Layout Recommendations for PROCHOT#**

Trace $Z_0$	Trace Spacing	L1	L2	L3	L4	Rpu
$60\ \Omega \pm 15\%$	7 mils	0.75" maximum	10" maximum	10" maximum	0.5" maximum	$120\ \Omega - 140\ \Omega \pm 5\%$

**Figure 38. Routing Illustration for PROCHOT#**



### 5.1.6.8 Topology 9: TESTHI Signals

The TESTHI pins adhere to the following routing and layout recommendations. The following figure illustrates the recommended topology. The TESTHI pins may use individual pull-up resistors or be grouped together as detailed below. A matched resistor, Rpu, should be used for each group.

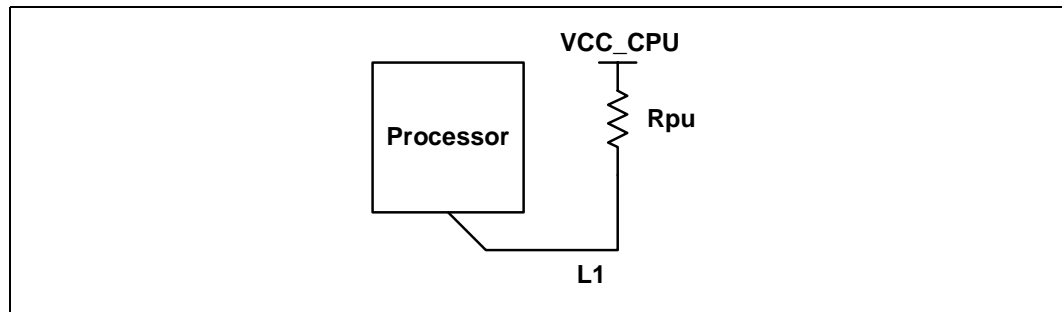
1. TESTHI[1:0]
2. TESTHI[7:2]
3. TESTHI8 - Cannot be grouped with any other TESTHI signal
4. TESTHI9 - Cannot be grouped with any other TESTHI signal
5. TESTHI10 - Cannot be grouped with any other TESTHI signal
6. TESTHI11 - Cannot be grouped with any other TESTHI signal
7. TESTHI12 - Cannot be grouped with any other TESTHI signal

**Table 31. Layout Recommendations for TESTHI Signals**

Trace $Z_0$	Trace Spacing	L1	Rpu
$60\ \Omega \pm 15\%$	7 mils	1" maximum	$62\ \Omega \pm 5\%$



**Figure 39. Routing Illustration for TESTHI Signals**



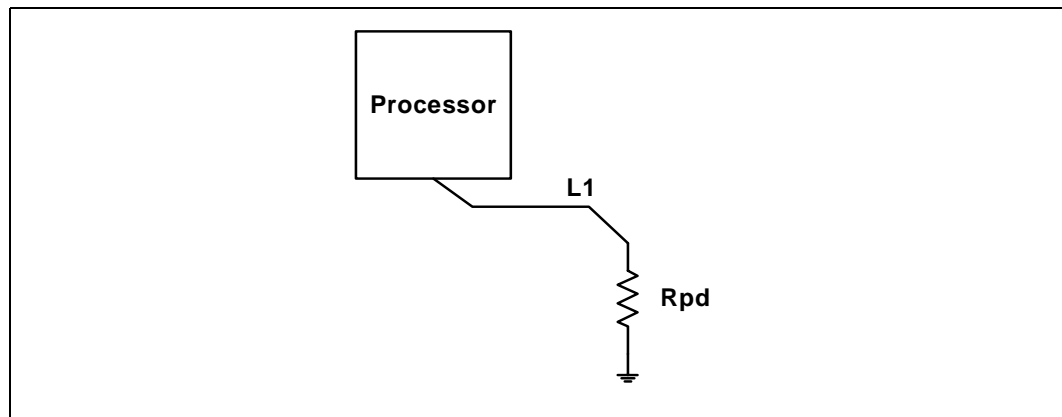
### 5.1.6.9 Topology 10: COMP[1:0]

The COMP[1:0] signals adhere to the following routing and layout recommendations. [Figure 40](#) illustrates the recommended topology.

**Table 32. Layout Recommendations for COMP[1:0]**

Trace $Z_0$	Trace Spacing	L1	Rpd
$60\ \Omega \pm 15\%$	13 mils	1.5" maximum	$61.9\ \Omega \pm 1\%$

**Figure 40. Routing Illustration for COMP[1:0]**



### 5.1.6.10 Topology 11: BOOTSELECT

Loadlines for the Pentium 4 processor and Pentium 4 processor with HT Technology require a different slope. Therefore, the VRD must switch feedback networks depending on which processor is installed. The BOOTSELECT signal is used by the VRD to detect whether a Pentium 4 processor with HT Technology or a Pentium 4 processor is inserted into the CPU socket and switches the feedback network. [Figure 41](#) shows a diagram of the switching while [Figure 42](#) shows an example switching circuit.

Refer to the appropriate processor electrical, mechanical, and thermal specifications for each processor.

Figure 41. VRD Feedback Switching Diagram

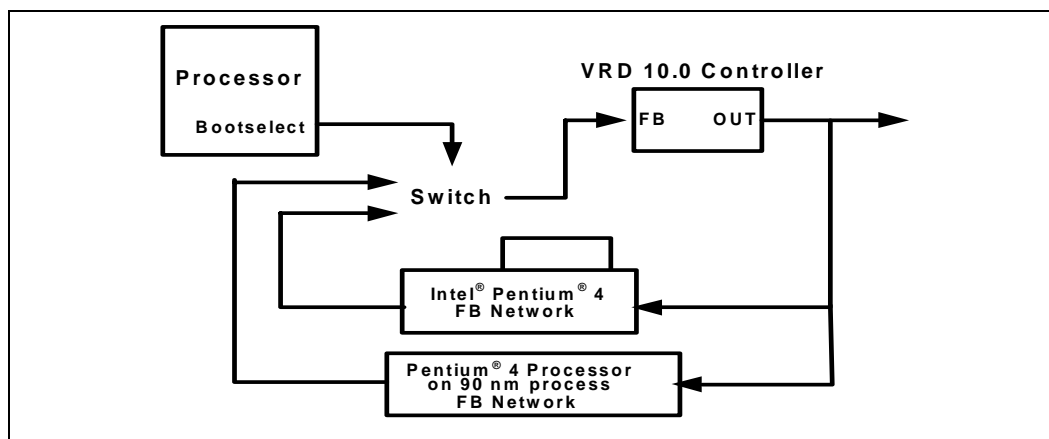
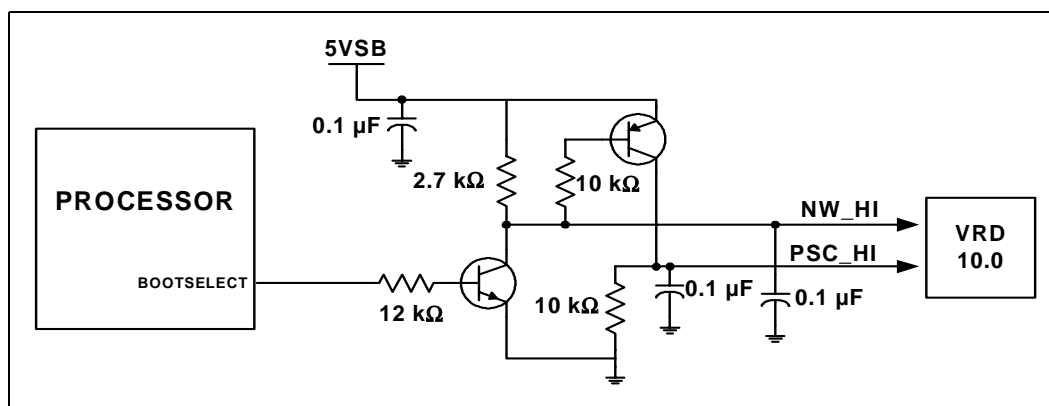


Figure 42. Routing Illustration for BOOTSELECT



#### 5.1.6.11 Topology 12: RESERVED

All RESERVED pins must remain unconnected. Connection of these pins to VCC, VSS, or any other signal (including each other) may result in component malfunction or incompatibility with a future Pentium 4 processor with HT Technology.

#### 5.1.6.12 Topology 13: OPTIMIZED/COMPAT#, IMPSEL and RSP#

For the Pentium 4 processor or a Pentium 4 processor with HT Technology, the OPTIMIZED/COMPAT# pin on the processor socket should be left as a no connect (NC).

For the Pentium 4 processor with 512 KByte L2 cache on 0.13 micron process, the IMPSEL pin on the processor socket should be left as an NC.

The RSP# signal on the processor socket should be left as an NC for the Pentium 4 processor with 512 KByte L2 Cache on 0.13 micron process, the Pentium 4 processor with HT Technology, or the Pentium 4 processor.

### 5.1.6.13 Host VREFs

The AGTL+ VREF provides a reference voltage for all of the FSB signals on the CPU and MCH. It is required that a voltage divider yields  $0.63 * VCC\_AVG$ , where  $VCC\_AVG$  is the average voltage of VCC (CPU core) and MCH\_VTT. The output is then routed to the CPU's GTLREF and to the MCH's HDVREF pin. The trace should be a minimum of 12 mils wide and have a minimum of 15 mils separation from any other trace.

Figure 43. HD\_VREF Circuit Topology

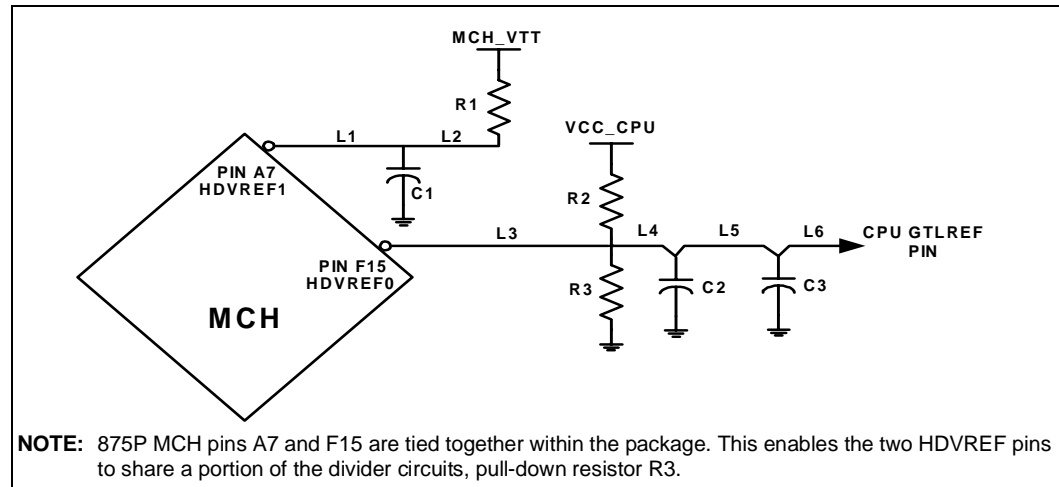


Table 33. Host VREF Resistor Values

Resistor	Value
R1	$200 \Omega \pm 1\%$
R2	$200 \Omega \pm 1\%$
R3	$169 \Omega \pm 1\%$
C1 <sup>1</sup>	0.1 $\mu$ F or 220 pF
C2	0.1 or 1.0 $\mu$ F
C3 <sup>2</sup>	220 pF

**NOTES:**

1. C1 should be placed as close to the MCH pin as possible.
2. C3 should be placed as close to the CPU pin as possible.

Table 34. Host VREF Trace Lengths

Segment	Value
L1 + L2	3.5" maximum
L3	3" maximum
L4 + L5 + L6	1.5" maximum

### 5.1.6.14 Host VID Topology

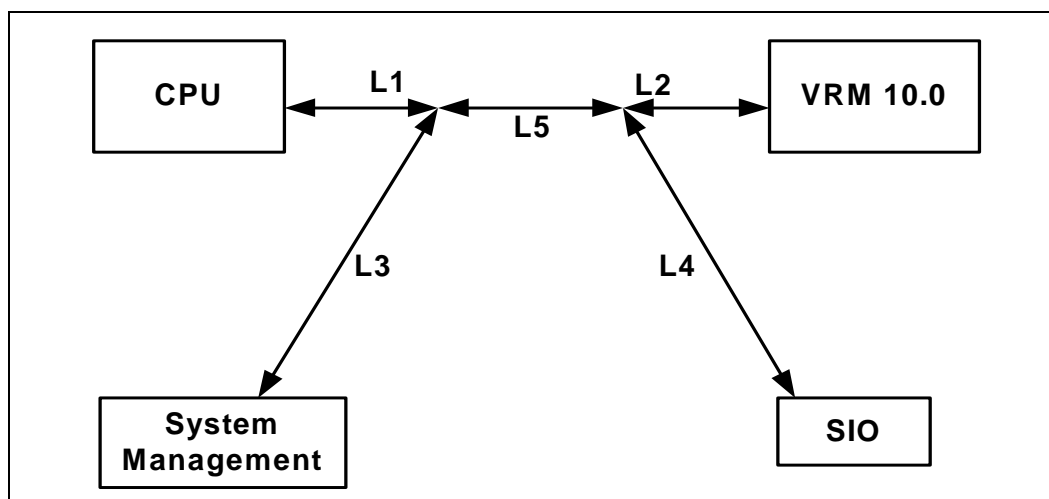
The host VID signals are used to set the VCC (CPU core) voltages. These signals are open drain and require pull-up resistors. The resistors should be  $1\text{ k}\Omega \pm 5\%$  and pulled up to 3.3 V.

In order for the VID code to arrive at the VRD, System Management Controller, and SIO with good signal integrity, it is required that the VID topology be as follows.

Note that it is not required to route each leg of the diagram. For instance, if you only need to route the VID lines from the CPU to the VRM, you do not need to route legs L3 and L4.

If the following topology cannot be achieved, then it is recommended that thorough simulation be done to ensure good signal integrity. The pull-up resistors may be located anywhere in the topology.

**Figure 44. VID Topology**



**Table 35. VID Topology Trace Lengths**

Dimension	Min	Max	Units
L1	--	12	Inches
L2	--	--	Inches
L1+L2+L5	--	15	Inches
L3	--	6	Inches
L4	--	6	Inches
L5	--	12	Inches

### 5.1.6.15 THERMDA/THERMDC

The processor incorporates an on-die thermal diode. THERMDA (diode anode) and THERMDC (diode cathode) pins on the processor may be connected to a thermal sensor located on the system board to monitor the die temperature of the processor for thermal management/long-term die temperature change monitoring purposes. This thermal diode is separate from the Thermal Monitor's thermal sensor and cannot be used to predict the behavior of the Thermal Monitor.

Because the thermal diode is used to measure a very small voltage from the remote sensor, care must be taken to minimize noise induced at the sensor inputs. Below are some guidelines:

- Remote sensor should be placed as close as possible to the THERMDA/THERMDC pins. It may be approximately four to eight inches away as long as the worst noise sources such as clock generators, data buses and address buses, etc., are avoided.
- Route the THERMDA/THERMDC lines in parallel and close together with ground guards enclosing the them.
- Use wide traces to reduce inductance and noise pickup that may be introduced by narrow traces or the system. A width of 10 mils and spacing of 10 mils is recommended.

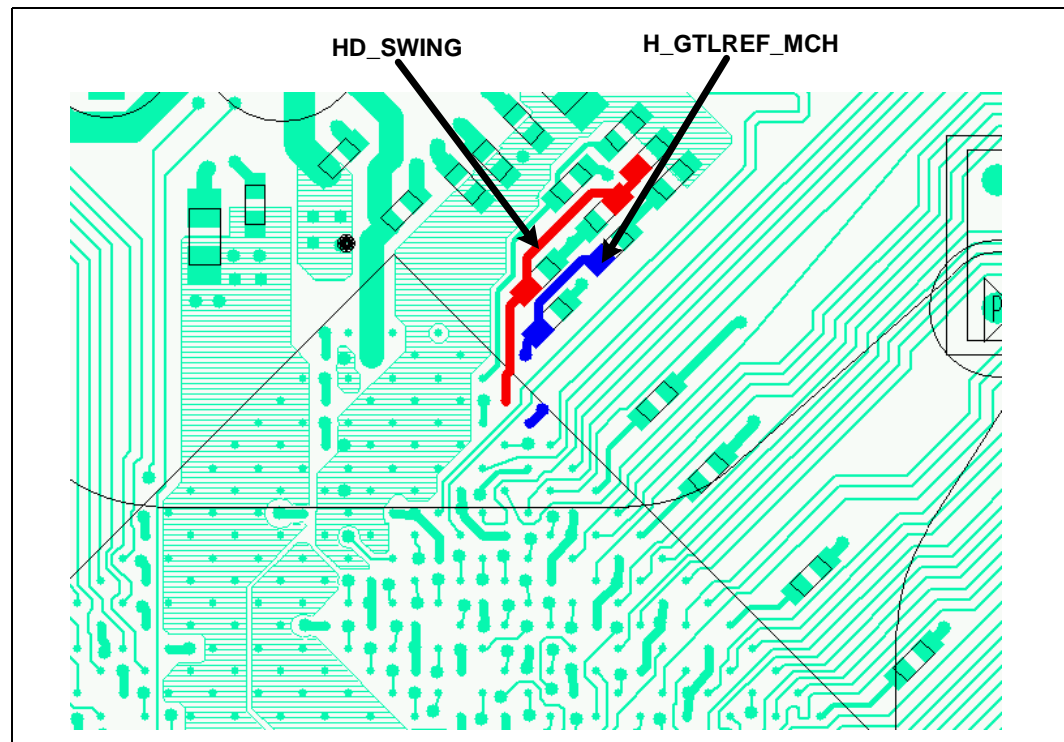
#### 5.1.6.16 Host RCOMP

The RCOMP pins are used to calibrate the AGTL+ buffers and need to be terminated to a  $20\ \Omega \pm 1\%$  pull-down resistor. It is recommended that the trace be a maximum of 0.5 inches long and be a minimum of 10 mils wide to reduce trace inductance. Keep this trace a minimum of 7 mils away from other traces.

#### 5.1.6.17 Host SWING

VSWING needs to be  $1/4 * MCH\_VTT$ , so a resistor divider with a  $301\ \Omega \pm 1\%$  pull-up and a  $102\ \Omega \pm 1\%$  pull-down are recommended. The HXSWING and HYSWING may be tied together on the motherboard to reduce redundant circuitry. Decouple with one  $0.01\ \mu F$  capacitor at the MCH. The trace to the MCH should be routed at a maximum of 3 inches long at 12 mils wide and 10 mil spacing. This may be accomplished on Layer 2 (see Figure 45).

**Figure 45. Host SWING Routing Example**



### 5.1.6.18 BSEL

The BSEL circuit determines the FSB frequency. Connect the processor's BSEL0 signal to the CK409's FSA pin. There should be a pull-up resistor and two pull-down resistors whose values are listed in Table 36. The middle of the voltage divider circuit should then connect to the MCH's BSEL0 pin. The two pull-down resistors form a voltage divider and are required for proper voltage levels for the MCH. Connect the MCH's BSEL1 to the CK409 FSB pin in the same manner.

Figure 46. BSEL Topology

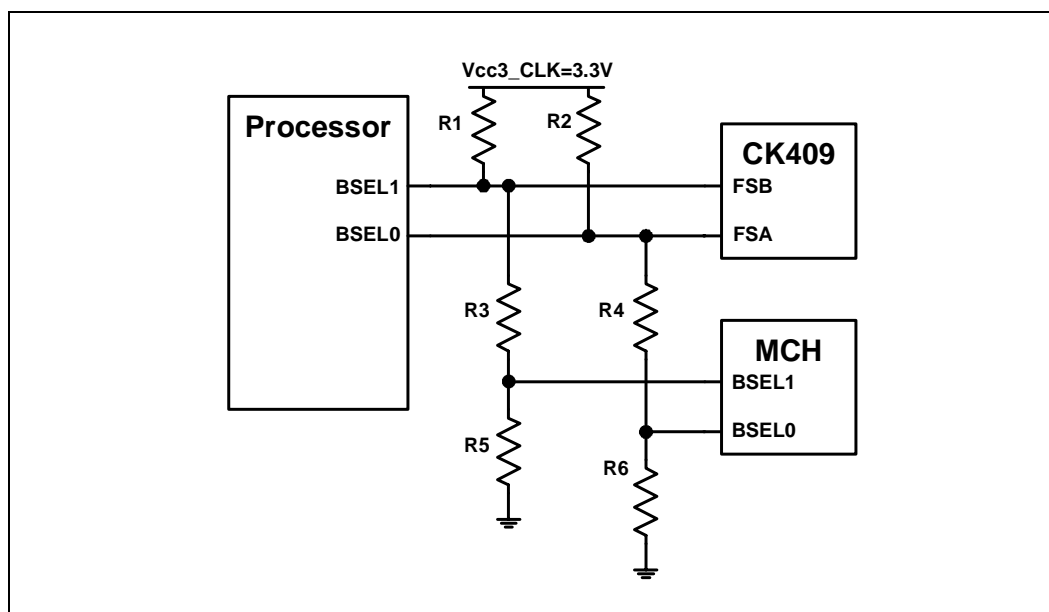


Table 36. BSEL Resistor Values

Resistor	Value
R1	1 k $\Omega$ $\pm$ 1%
R2	1 k $\Omega$ $\pm$ 1%
R3	2 k $\Omega$ $\pm$ 1%
R4	2 k $\Omega$ $\pm$ 1%
R5	2.49 k $\Omega$ $\pm$ 1%
R6	2.49 k $\Omega$ $\pm$ 1%

Table 37. FSB Frequency Selection

FSA, FSB	FSB Frequency
0, 0	400 MHz
1, 0	533 MHz
0, 1	800 MHz

**NOTE:** For FSA and FSB input latching, refer to the *Intel Pentium 4 Processor with HT Technology Electrical, Mechanical, and Thermal Specifications*.

## 5.2 Trace Length Matching

Trace length matching is required within each source synchronous group to compensate for the package trace length differences between data signals and the associated strobe. This will balance the strobe-to-signal skew in the middle of the setup and hold window. An example of trace length matching is given in [Example 1 on page 76](#).

Trace length matching consists of matching the pad-to-pad lengths for every signal within a signal group (e.g., HA[35:17]# and ADSTB1#). A pad-to-pad length is measured as follows:

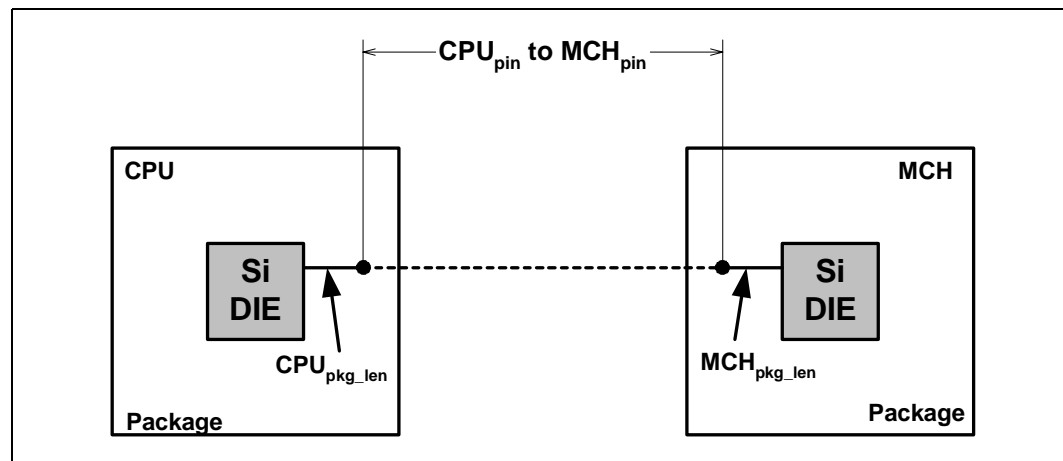
$$\text{CPU}_{\text{pad-to-MCH}_{\text{pad}}} \text{ Length} = \text{CPU}_{\text{pkg\_len}} + \text{CPU}_{\text{pin-to-MCH}_{\text{pin}}} + \text{MCH}_{\text{pkg\_len}}$$

Where:

- $\text{CPU}_{\text{pin-to-MCH}_{\text{pin}}}$  = Motherboard trace length between Processor 1 and MCH.
- $\text{pkg\_len}$  = Pad to pin length within the package.

The package trace lengths for 875P MCH are available in the *Intel 875 Memory Control Hub (MCH) Datasheet*. The package trace lengths for E7210 MCH are available in the *Intel E7210 Memory Controller Hub (MCH) Datasheet*. The package trace lengths for the Pentium 4 processor are available in the *Intel Pentium 4 Processor with HT Technology I/O Buffer Models*.

**Figure 47. Trace Length Matching for the Front Side Bus**



When length matching, the board designer should set every signal's pad-to-pad length equal to each other, within  $\pm 25$  mils. This yields the following equation:

$$\begin{aligned} \text{CPU}_{\text{pkg\_len}} (\text{Signal 1}) + \text{CPU}_{\text{pin\_len to MCH}_{\text{pin\_len}}} (\text{Signal 1}) + \text{MCH}_{\text{pkg\_len}} (\text{Signal 1}) = \\ \text{CPU}_{\text{pkg\_len}} (\text{Signal 2}) + \text{CPU}_{\text{pin\_len to MCH}_{\text{pin\_len}}} (\text{Signal 2}) + \text{MCH}_{\text{pkg\_len}} (\text{Signal 2}) \end{aligned}$$

To length match Signal 1 and Signal 2, hold one of the signals constant, and vary the second signal until the equation is satisfied. Since all the  $\text{pkg\_len}$  values are constant, we may solve for Signal 2:

$$\begin{aligned} \text{CPU}_{\text{pin\_len to MCH}_{\text{pin\_len}}} (\text{Signal 2}) = \text{CPU}_{\text{pkg\_len}} (\text{Signal 1}) + \text{CPU}_{\text{pin\_len to MCH}_{\text{pin\_len}}} (\text{Signal 1}) \\ + \text{MCH}_{\text{pkg\_len}} (\text{Signal 1}) - (\text{CPU}_{\text{pkg\_len}} (\text{Signal 2}) + \text{MCH}_{\text{pkg\_len}} (\text{Signal 2})) \end{aligned}$$

Generally, when length matching a group of signals, a designer will first lay out all signals to the shortest length possible allowed by specification. Then, keeping the longest signal as the constant value (Signal 1), lengthen all the other signals so that the pad-to-pad lengths are all equal.

### Example 1. Trace Length Matching

**Consider the signals D4# and DSTBP0# and DSTBN0# from the same group. Calculate CPU to MCH length for D4#:**

$$\text{CPU}_{\text{pkg\_len}}(\text{DSTBP0\#}) = 0.190 \text{ inch}$$

$$\text{CPU}_{\text{pkg\_len}}(\text{DSTBN0\#}) = 0.180 \text{ inch}$$

$$\text{CPU}_{\text{pin\_len}} \text{ to MCH}_{\text{pin\_len}}(\text{DSTBP0\#}) = 5.0 \text{ inches}$$

$$\text{CPU}_{\text{pin\_len}} \text{ to MCH}_{\text{pin\_len}}(\text{DSTBN0\#}) = 5.1 \text{ inches}$$

$$\text{MCH}_{\text{pkg\_len}}(\text{DSTBP0\#}) = 0.240 \text{ inch}$$

$$\text{MCH}_{\text{pkg\_len}}(\text{DSTBN0\#}) = 0.250 \text{ inch}$$

$$\text{CPU}_{\text{pad-to-MCH}_{\text{pad}}} \text{ Length}(\text{DSTBP0\#}) = 5.43 \text{ inches}$$

$$\text{CPU}_{\text{pad-to-MCH}_{\text{pad}}} \text{ Length}(\text{DSTBN0\#}) = 5.53 \text{ inches}$$

$$\text{CPU}_{\text{pad-to-MCH}_{\text{pad}}} \text{ Length}(\text{DSTBavg}) = 5.48 \text{ inches}$$

$$\text{CPU}_{\text{pkg\_len}}(\text{D4\#}) = 0.198 \text{ inch}$$

$$\text{MCH}_{\text{pkg\_len}}(\text{D4\#}) = 0.225 \text{ inch}$$

$$\text{CPU}_{\text{pin\_len-to-MCH}_{\text{pin\_len}}}(\text{D4\#}) = \text{CPU}_{\text{pad-to-MCH}_{\text{pad}}} \text{ Length}(\text{DSTBavg}) - (\text{CPU}_{\text{pkg\_len}}(\text{D4\#}) + \text{MCH}_{\text{pkg\_len}}(\text{D4\#}))$$

Therefore, the PCB trace length of D4# must be within  $\pm 25$  mils of 5.057 inches from the processor to MCH.

## 5.3 Retention Mechanism Placement and Keep-Outs

The retention mechanism requires a keep-out zone, for limited component height area under the retention mechanism as shown in the following figures. [Figure 48](#) and [Figure 49](#) show the relationship between the retention mechanism mounting holes and pin one of the socket. In addition they also document the keep-outs.

For heatsink volumetric information, refer to the *Intel Pentium 4 Processor on 90 nm Process Thermal and Mechanical Design Guide* and the *Intel Pentium 4 Processor with 512 KByte L2 Cache on 0.13 Micron Process Thermal Design Guidelines*.



Figure 48. Retention Mechanism Keep-Out Drawing 1

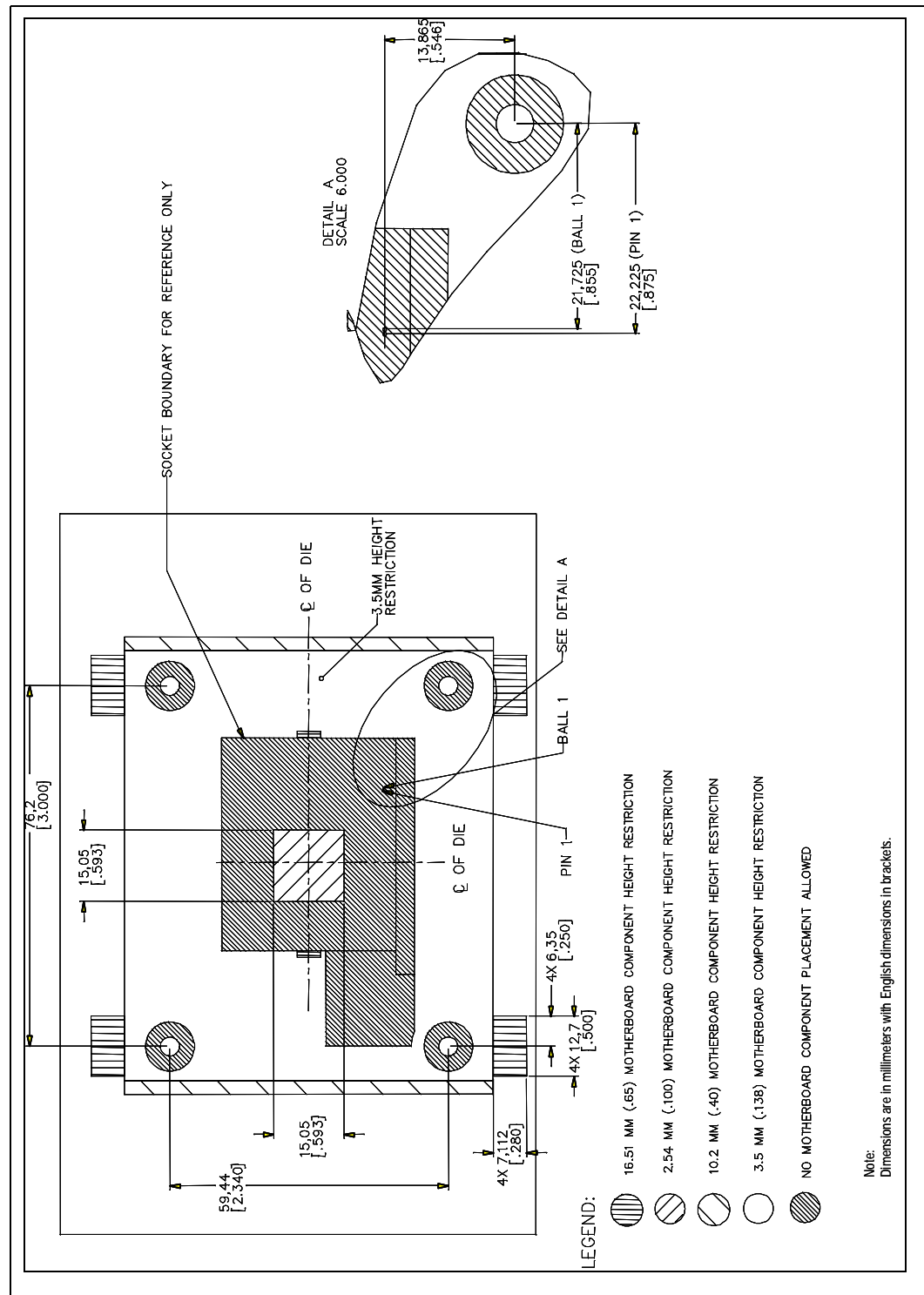
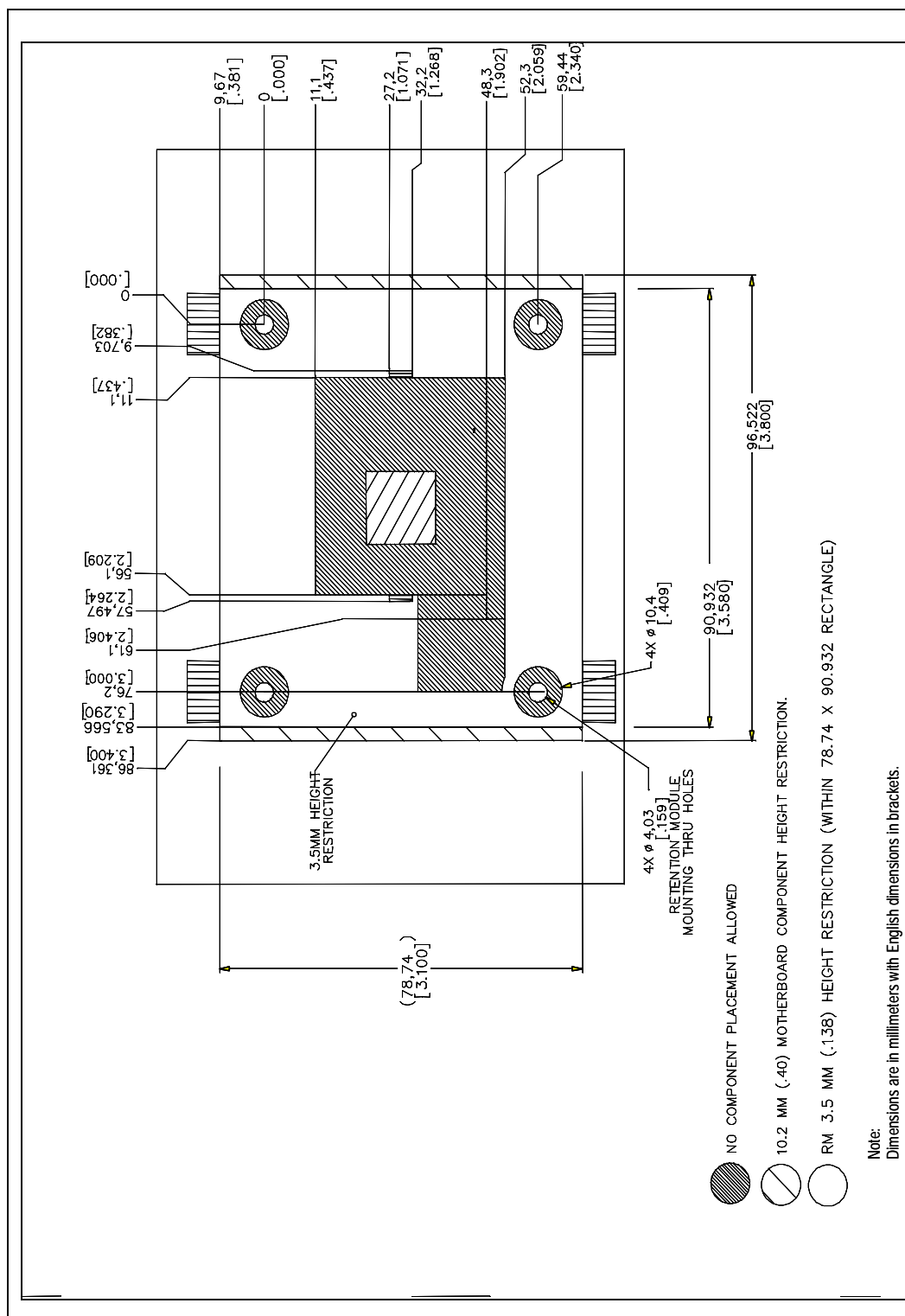


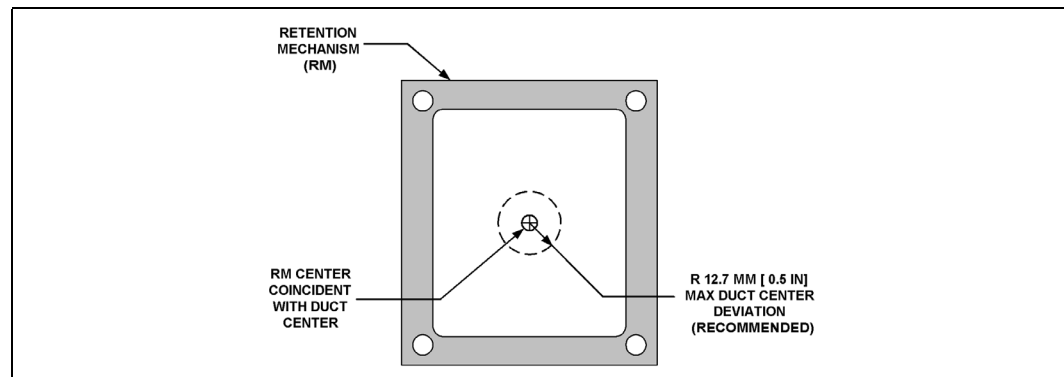
Figure 49. Retention Mechanism Keep-Out Drawing 2



## 5.4 Processor Location Relative to Retention Mechanism

To ensure compatibility with chassis using a duct based on the reference Chassis Air Guide ducting solution, the processor should be placed at a location corresponding to the center of the duct. Information on duct position is available in the *Desktop System Air Duct Design Suggestions*.

Board layouts should locate the center the processor heatsink retention mechanism within a 12.7 mm [0.5 inch] radius of the duct center location. The sketch below illustrates the placement guideline.



## 5.5 Power Header for Active Cooling Solutions

The reference-design heatsink solution includes an integrated fan. The recommended connector for the active cooling solution is a Walden\*/Molex\* 22-01-3037, AMP\* 643815-3, or equivalent. The integrated fan requires the system board to supply a minimum of 740 mA at 12 V for proper operation. The fan connector pinout is described in [Table 38](#).

**Table 38. Reference Solution Fan Power Header Pinout**

Pin Number	Signal
1	Ground
2	+12 V
3	No Connect

The Intel boxed processor heatsink solution includes an integrated fan. The recommended connector for the active cooling solution is a Walden/Molex 22-23-2037, AMP 640456-3, or equivalent. The integrated fan requires the system board to supply a minimum of 740 mA at 12 V for proper operation. The fan connector pinout is described in [Table 39](#).

**Table 39. Boxed Processor Fan Power Header Pinout**

Pin Number	Signal
1	Ground
2	+12 V
3	Sense

The fan heatsink outputs a SENSE signal which is an open-collector output that pulses at a rate of two pulses per fan revolution. The system board requires a pull-up resistor to provide the appropriate V<sub>OH</sub> level to match the fan speed monitor. Use of the SENSE signal is optional. If the SENSE signal is not used, pin 3 should be tied to ground.

For more information on boxed processor requirements, refer to the *Intel Pentium 4 Processor 90 nm Process Datasheet* and the *Intel Pentium 4 Processor with 512 KB L2 Cache on 0.13 micron Process Datasheet*.

## 5.6 Debug Port Guidelines

Please refer to the latest revision of the *Intel Pentium 4 processor Debug Port Design Guide* for details on the implementation of the debug port.

### 5.6.1 Debug Tools Specifications

#### 5.6.1.1 Logic Analyzer Interface (LAI)

Intel is working with two logic analyzer vendors to provide logic analyzer interfaces (LAIs) for use in debugging the Pentium 4 / Pentium 4 with HT Technology processors in the 478-pin package system. Tektronix\* and Agilent\* should be contacted to get specific information about their logic analyzer interfaces. The following information is general in nature. Specific information must be obtained from the logic analyzer vendor.

Due to the complexity of these processors, the LAI is critical in providing the ability to probe and capture system bus signals. When designing a system based on these processors that may make use of an LAI, there are two sets of considerations to keep mind: mechanical and electrical.

#### 5.6.1.2 Mechanical Considerations

The LAI is installed between the processor socket and the processor. The LAI pins plug into the socket, while the processor pins plug into a socket on the LAI. Cabling that is part of the LAI egresses the system to allow an electrical connection between the processor and a logic analyzer. The maximum volume occupied by the LAI, known as the keep-out volume, as well as the cable egress restrictions, should be obtained from the logic analyzer vendor. System designers must make sure that the keep-out volume remains unobstructed inside the system. Note that it is possible that the keep-out volume reserved for the LAI may include space normally occupied by the processor heat sink. If this is the case, the logic analyzer vendor will provide a cooling solution as part of the LAI.

#### 5.6.1.3 Electrical Considerations

The LAI will also affect the electrical performance of the system bus; therefore, it is critical to obtain the electrical load models from each of the logic analyzer vendors to be able to run system level simulations to prove that their tool will work in the system. Contact the logic analyzer vendor for electrical specifications and load models for the LAI solution they provide.

# DDR System Memory Guidelines

## 6

### 6.1 Introduction

**Caution:** All signals in this section are assumed to be routed microstrip. If you choose to route on inner layers, you must perform thorough signal integrity and timing simulations on each design.

The MCH memory interface consists of two DDR memory channels that may operate in either single-channel or dual-channel modes. Each channel consists of 64 data bits.

This section covers routing guidelines for the DDR interface. Note that these guidelines apply to both channel A and channel B. Each DDR interface has six signal groups: Clocks, Address/Command, Data, Control, and Miscellaneous. [Table 40](#) summarizes the signal groupings. The MCH contains two complete sets of these signals, one set per channel. Refer to the *Intel 875P MCH Memory Controller Hub (MCH) Datasheet* or the *Intel E7210 MCH Memory Controller Hub (MCH) Datasheet* for details on the signals listed in [Table 40](#).

Please refer to [Chapter 13](#) for DDR power delivery considerations.

The DDR guidelines are structured in the following fashion:

[Section 6.6](#) contains guidelines necessary to implement a two-DIMM-per-channel solution. Using these guidelines, the motherboard designer may choose to implement both one-DIMM and two-DIMM-per-channel solutions. [Section 6.7](#) details exceptions to the following guidelines for a one-DIMM-per-channel solution.

**Table 40. MCH DDR Signal Groups**

Section	Group	Signal	Description
<a href="#">Section 6.6.2</a>	Clocks	SCMDCLK[5:0] SCMDCLK[5:0]#	DDR Differential Clocks DDR Differential Inverted Clocks
<a href="#">Section 6.6.4</a>	Address/Command	SMA[12:0] SRAS# SCAS# SWE# SBA[1:0]	Memory Address Bus Row Address Select Column Address Select Write Enable Bank Address (Bank Select)
<a href="#">Section 6.6.5</a>	Data	SDQS[8:0] SECC[7:0] SDQ[63:0]	Data Strokes Check Bits for ECC Function Data Bus
<a href="#">Section 6.6.3</a>	Control	SCS[3:0]# SCKE[3:0]	Chip Select Clock Enable

**NOTE:** The signals listed above are for a single channel only. When in dual-channel mode there will be two of each of these signals, one for channel A and one for channel B; for example, DQ[0]A and DQ[0]B.

## 6.2 DDR Length Matching Strategy

### 6.2.1 Strategy Overview

Consider the following information before you attempt to route the DDR interface. There are two levels of length constraints placed on each signal group within the interface.

- The absolute length constraints are provided in the constraint tables for each signal group. These constraints define the length range over which the signals will meet signal integrity rules.
- A subset of this solution space is then defined by a set of secondary length constraints which are based on length matching to clock. The clock relative length matching formulas are not concerned with signal integrity compliance, but purely based on clock relative timing margins. These two sets of overlapping length constraints then define the final routing solution space.

**Note:** The absolute length constraints are based on motherboard routing lengths, while the length matching formulas are based on pad-to-pin lengths. Therefore, care must be taken when trying to reconcile the two sets of constraints with respect to each other. It is recommended that an automated routing length spreadsheet be used to calculate motherboard routing lengths as required to implement the length matching formulas. Only after package lengths have been factored into the length matching formulas may motherboard lengths be compared directly. In some cases motherboard length boundaries will be determined by the length matching formulas, whereas in other cases the absolute motherboard length limits will come into play.

### 6.2.2 Defining the Target Clock Reference Length

Since all signal groups are directly or indirectly timing referenced back to clock, the clock is the logical choice to serve as the master reference for all other signal groups, by way of length matching formulas. It is recommended that following a preliminary test route which establishes the natural bounds on all signal groups, that target reference lengths be defined for each clock group routed between the MCH and the DIMM connectors. Throughout this chapter, the target Clock Reference length is defined as:

**DIMM0 Clock: Target Reference Length = X0**

**DIMM1 Clock: Target Reference Length = X1**

For optimal timing margins, all clocks to a particular DIMM connector should be length tuned to the target reference length for that DIMM. These reference lengths will then feed into the length matching formulas to determine the secondary constraints on minimum and maximum length for each signal group, as routed to the corresponding DIMM connector. Generally speaking, the offset in clock target length between DIMMs should be approximately equal to the routing length between the DIMMs. This provides length matching consistency between DIMMs.

In some cases, it is helpful to base the target clock lengths on the natural routing lengths of certain critical path signals as opposed to the natural lengths of the clocks themselves. In the case of the 875P MCH, the control group setup margin is a critical path. Therefore, it is recommended that the target clock length be partially based on providing adequate setup margin as per the length matching formula. This may require that the clocks be lengthened slightly from their natural length.

## 6.3 Length Matching and Length Formulas

The routing guidelines presented in the main body of this document define the recommended routing topologies, trace width and spacing geometries, absolute minimum and maximum routed lengths for each DDR signal group. This is recommended to meet signal integrity requirements. In addition to the absolute length limits provided in the guideline tables for each signal group, more restrictive length matching formulas are also provided which further restrict the minimum to maximum length range of each signal group with respect to clock. These are within the overall boundaries defined in the guideline tables as required to ensure adequate timing margins. These secondary constraints are referred to as length matching constraints, and the formulas used are referred to as length matching formulas.

All signal groups except the clocks and feedback signals are length matched per slot to the associated clocks, with the clocks themselves being length tuned to a fixed length range across each DIMM slot. The amount of minimum to maximum length variance allowed for each group around the clock reference length varies from signal group to signal group depending on the amount of timing variance which may be tolerated.

A simplified summary of the length matching formulas for each signal group is provided in the table below. As the table indicates, all signal groups are somewhat biased in length to be shorter than clock. This is done to optimize setup and hold margins.

**Table 41. Length Matching Formulas**

Signal Group	Minimum Length	Maximum Length
Control to Clock	Clock (max) - 2.0"	Clock (min) - 0.5"
Command to Clock	Clock (max) - 2.0"	Clock (min) - 0.5"
Strobe to Clock	Clock (max) - 2.0"	Clock (min) + 1.0"
Data to Strobe	Strobe - 25 mils	Strobe +25 mils

**NOTE:** All length matching formulas are based on MCH die-pad to DIMM pin total length.

The clock length used for length matching may vary by DIMM slot, based on DIMM spacing. Length formulas should be applied to each DIMM slot independently. The full geometry and routing guidelines along with the exact length matching formulas and associated diagrams are provided in the individual signal group guidelines sections to follow.

**Note:** For short clock lengths the command to clock maximum length rule may be slightly relaxed, due to crisper clock edge rates and more setup margin at shorter lengths. See clock section for more detailed information.

## 6.4 Package Length Compensation

As mentioned briefly above, all length matching is done MCH die-pad to DIMM pin. The reason for this is to compensate for the package length variance across the signal group in order to minimize timing variance. The MCH does not attempt to equalize package lengths internally as some previous MCH components have, and therefore requires a more tedious matching or tuning process. The justification for this is based on the belief that length variance in the package based on ball position will be at least partially tuned out when the pin escape is completed to the edge of the package. Length matching in the package would then tend to create mismatch at the package edge.

Package length compensation should not be confused with length matching as discussed in the previous section. Length matching as discussed previously refers to constraints on the minimum and maximum length bounds of a signal group based on clock length, whereas package length compensation refers to the process of adjusting out package length variance across a signal group. There is, of course, some overlap in that both affect the target length of an individual signal. It is recommended that a routing length spreadsheet be used to facilitate the package compensated routing.

## 6.5 Stack-Up and Referencing Guidelines

875P MCH/E7210 MCH/6300ESB ICH chipset designs require ground referencing for all DDR signals. Based on a typical six-layer stack-up, the DDR channel will require the following stack-up in order to ground reference all of the DDR signals from the MCH to the termination at the end of the channel. Note that the DDR channel stack-up applies to the DDR channel only.

**Table 42. DDR Channel Referencing Stack-Up**

Motherboard Layer	Description
Layer 1, Signal Top	Signal/Power
Layer 2, Power	Ground Cutouts
Layer 3, Signal	Signal
Layer 4, Signal	Signal
Layer 5, Ground	Ground
Layer 6, Signal Bottom	Signal/Power

**Caution:** All signals in this section are assumed to be routed microstrip. If you choose to route on inner layers, you must perform thorough signal integrity and timing simulations on each design.

A solid ground flood needs to be placed under the DDR channel on layer 2 from the MCH DDR signal pins all the way beyond the DDR\_TERM termination capacitors at the end of the channel to provide an optimal return current path. Any split in the ground flood will provide a sub-optimal return path.

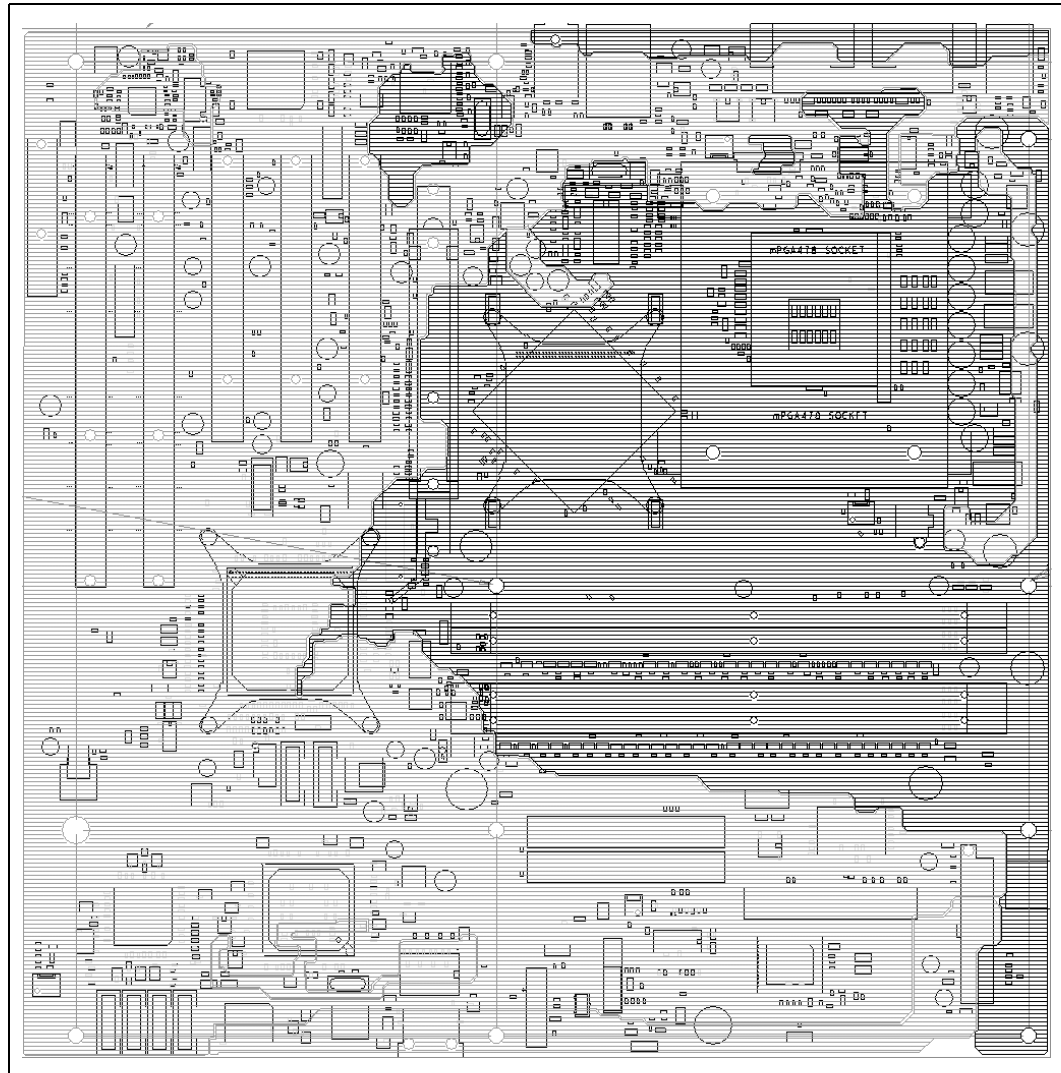
### 6.5.1 Ground Stitching

Ground floods must be well stitched to the ground plane on layer 5 to ensure the same potential between the two planes. Any ground pin or ground via that is placed in the DDR routing area must connect to both the ground flood and the ground plane.

It is also important to note that no power to the MCH is delivered on Layer 2. This is due to the strict ground referencing requirements. As a result, this region on Layer 2 is a large ground flood. Power must be delivered on Layers 1 and 6 (top and bottom); care must be taken to allow for proper power delivery on these external layers. Refer to [Chapter 13, “Power Distribution Guidelines”](#) for more information.



Figure 50. Example of Ground Flood on Layer 2



## 6.6 DDR Design Topologies and Guidelines

The layout guidelines in this chapter were developed with the following design assumptions:

- A standard 6-layer motherboard stack up
- Two DDR channels, with one or two DIMMs each
- **All** channel A DDR signals are routed on layer 1
- **All** channel B DDR signals are routed on layer 6

Signals routed on Layer 6 (bottom) may use the last row of pins on the DIMM connector to transition to Layer 1 (top) instead of using a via to get back to the top layer before reaching the termination resistors.

For 1 DIMM per-channel designs please refer to [Section 6.7](#) for design considerations specific to a 1 DIMM per-channel implementation.

### 6.6.1 Target Impedances

The target impedances listed throughout [Section 6.6](#) all refer to the area between MCH and first DIMM.

Due to the congested routing in the DIMM connector and termination regions of the routing channel it is not possible to meet the target impedances in these regions. As a result, it is not possible to maintain the target impedances once the signals reach the first DIMM connector. The resulting guidelines for the DIMM connector regions do not meet the target impedance but have been simulated and are believed to offer the best possible electrical characteristics given the severely constrained routing area.

### 6.6.2 Clock Signal Group Routing Guidelines (SCMDCLK/SCMDCLK#)

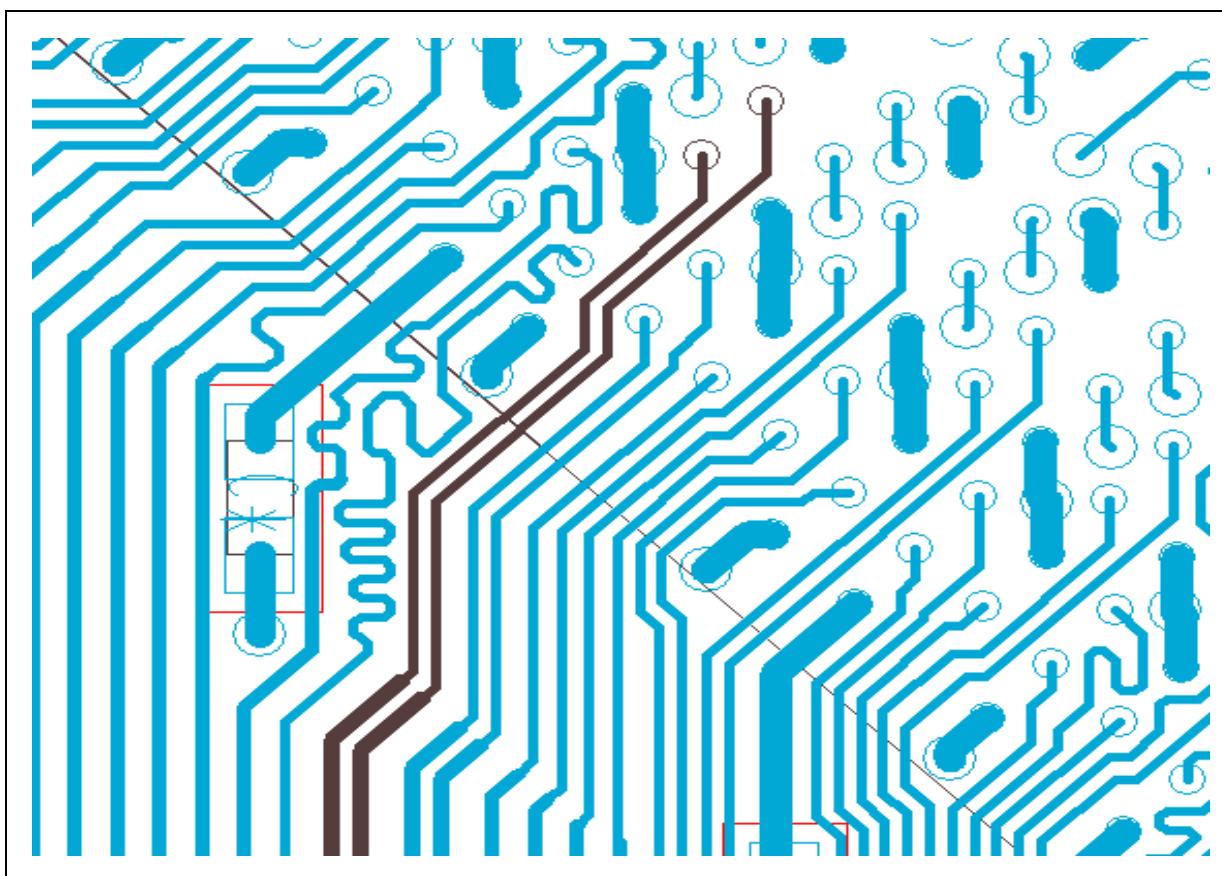
The clock signals include six differential clock pairs per channel. The MCH generates and drives these differential clock signals required by the DDR interface. Therefore, no external clock driver is required for the DDR interface. Since the MCH only supports unbuffered DDR DIMMs, three differential clock pairs are routed to each DIMM connector.

**Table 43. Clock Signal DIMM Mapping per DIMM**

Signal	Relative To
SCMDCLK[2:0] SCMDCLK#[2:0]	DIMM 0
SCMDCLK[5:3] SCMDCLK#[5:3]	DIMM 1

DDR clocks may break out of the MCH with reduced width (neckdown to five on five) for a maximum length of 500 mils; however, use of this reduced trace width should be minimized where possible. [Figure 51](#) shows an example of the clock neckdown in the MCH breakout.

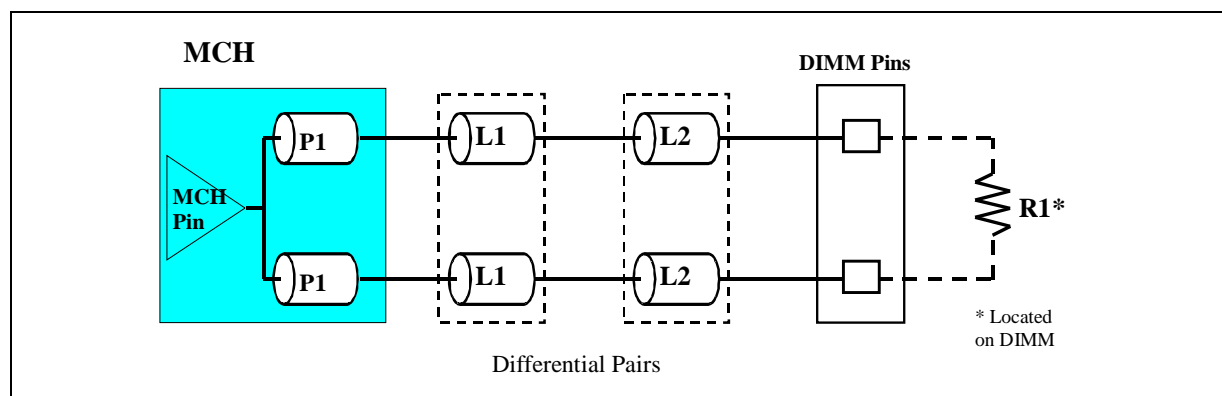
Figure 51. Example of DDR Clock Neckdown at MCH



The clock pairs must be routed differentially from the MCH to their DIMM pins. They must maintain correct spacing of 5 mils between themselves to remain differential. Additionally, the clocks must maintain an isolation spacing of 20 mils away from other signals or from itself in a serpentine.

There are no external termination resistors needed for the SCMDCLK/SCMDCLK# signals. Figure 52 and Table 44 depict the recommended topology and layout routing guidelines for the DDR differential clocks.

**Figure 52. DDR Differential Clock Routing Topology**



**Table 44. Clock Signal Group Routing Guidelines (Sheet 1 of 2)**

Parameter	Definition
Signal group	SCMDCLK[5:0] and SCMDCLK#[5:0]
Topology	Differential Pair Point-to-Point
Reference plane	Ground Referenced
Layer assignment	Layers 1 and 6 - Microstrip
Single ended trace impedance ( $Z_0$ )	$42 \Omega \pm 15\%$
Differential mode impedance ( $Z_{diff}$ )	$70 \Omega \pm 20\%$
Nominal trace width (see exceptions for breakout region below)	8 mils
Nominal pair spacing (edge to edge)	5 mils
Minimum pair to pair spacing (see exceptions for breakout region below)	20 mils
Minimum serpentine spacing	20 mils
Minimum spacing to other DDR signals (see exceptions for breakout region below)	20 mils
Minimum isolation spacing to non-DDR signals	20 mils
Maximum via count	2 (per side)
Package length (P1)	750 mils $\pm$ 500 mils (see package length report)

**NOTES:**

1. Overall target length should be established based on test route results and a cursory review of length matching formulas. In particular, the target length should be set to a minimum of the longest control signal length plus 0.5 inches, in order to optimize that path. Once the target length is established all clocks to that DIMM should be length tuned to the target length as defined. The resulting motherboard segment lengths of each clock must fall within the ranges specified.
2. The difference in target length between DIMM0 clocks and DIMM1 clocks should be approximately equivalent to the routing distance between DIMMs, in order to facilitate length matching on bussed signals. The maximum length variance across all clocks should not exceed 1.0 inch, as defined above.
3. Exceptions to the trace width and spacing geometries are allowed in the breakout region in order to fanout the interconnect pattern. Reduced spacing should be avoided as much as possible. Reduced trace width and spacing is also allowed in DIMM pin field region. Once reduced the trace should stay reduced to final connection.

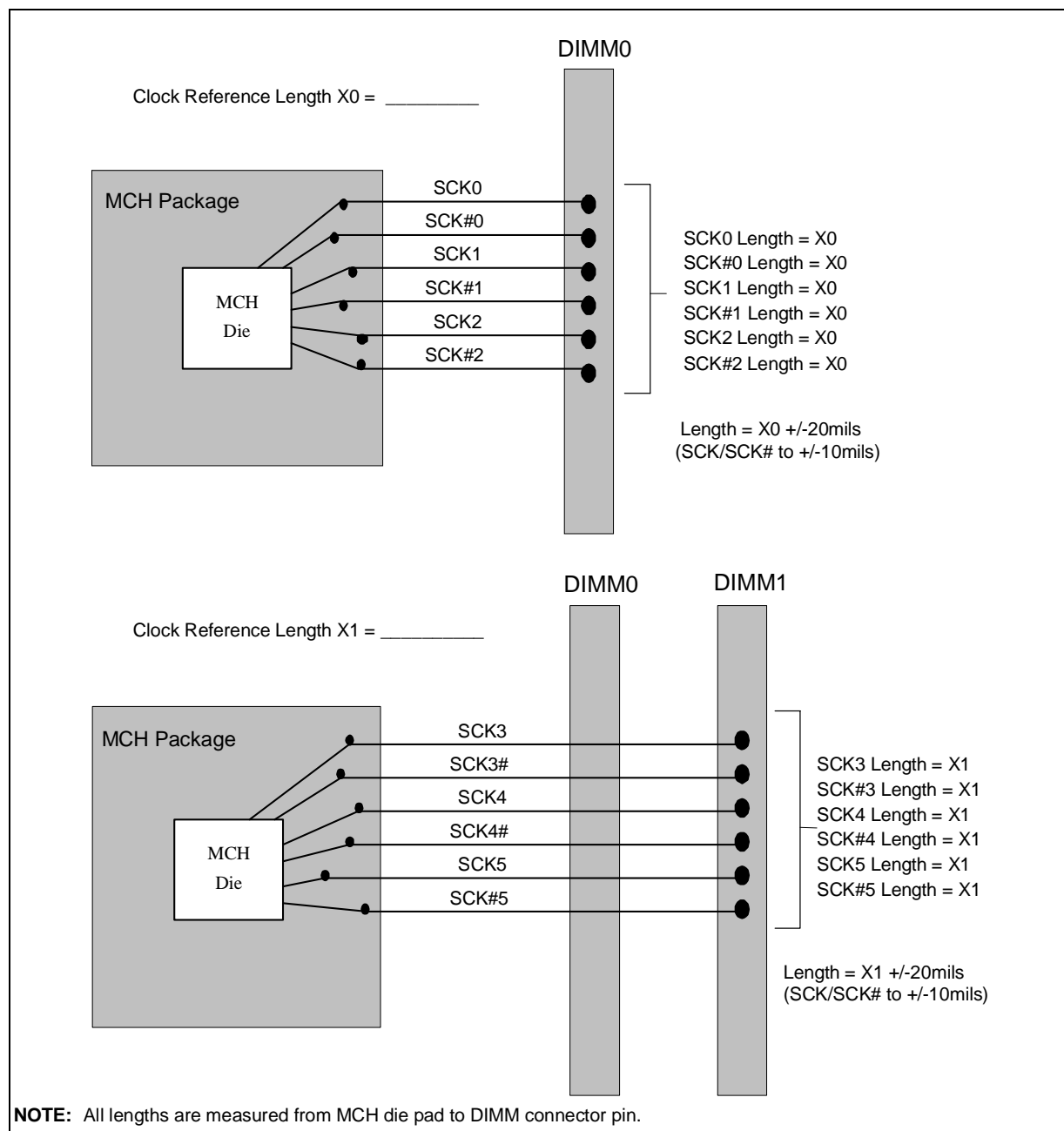
**Table 44. Clock Signal Group Routing Guidelines (Sheet 2 of 2)**

Parameter	Definition
Breakout length (L1)	Max = 500 mils
Total motherboard length limits (L1 + L2)	Min = 3.5 inches Max = 6.0 inches
Total length limits (P1 + L1 + L2)	Max = 6.3 inches
Clock target lengths	Total length for DIMM0 group = X0 (See <a href="#">Section 6.2.2</a> for target reference length X0 definition) Total length for DIMM1 group = X1 (See <a href="#">Section 6.2.2</a> for target reference length X0 definition)
SCLK to SCLK# length matching	Match total length to $\pm 10$ mils
Clock to clock length matching (total length)	Match all DIMM0 clocks to $X0 \pm 20$ mils (See <a href="#">Section 6.2.2</a> for target reference length X0 definition) Match all DIMM1 clocks to $X1 \pm 20$ mils (See <a href="#">Section 6.2.2</a> for target reference length X0 definition) Maximum clock length variance = 1.0 inch
Breakout exceptions (reduced geometries for MCH breakout region)	5 mil trace with 5 mil pair space allowed 5 mil pair to pair spacing allowed 10 mil spacing to other DDR signals allowed Maximum breakout length is 0.5 inch
DIMM field exceptions (reduced geometries for DIMM pin field region)	6 mil trace with 5 mil pair space allowed Maximum reduced trace width length is 1.5 inches 10 mil spacing to other DDR signals allowed Maximum reduced spacing length is 1.0 inch

**NOTES:**

- Overall target length should be established based on test route results and a cursory review of length matching formulas. In particular, the target length should be set to a minimum of the longest control signal length plus 0.5 inches, in order to optimize that path. Once the target length is established all clocks to that DIMM should be length tuned to the target length as defined. The resulting motherboard segment lengths of each clock must fall within the ranges specified.
- The difference in target length between DIMM0 clocks and DIMM1 clocks should be approximately equivalent to the routing distance between DIMMs, in order to facilitate length matching on bussed signals. The maximum length variance across all clocks should not exceed 1.0 inch, as defined above.
- Exceptions to the trace width and spacing geometries are allowed in the breakout region in order to fanout the interconnect pattern. Reduced spacing should be avoided as much as possible. Reduced trace width and spacing is also allowed in DIMM pin field region. Once reduced the trace should stay reduced to final connection.

Figure 53. Clock-to-Clock Length Matching Requirements



### 6.6.3 Control Signal Group Routing Guidelines (SCKE[3:0]#, SCS[3:0]#)

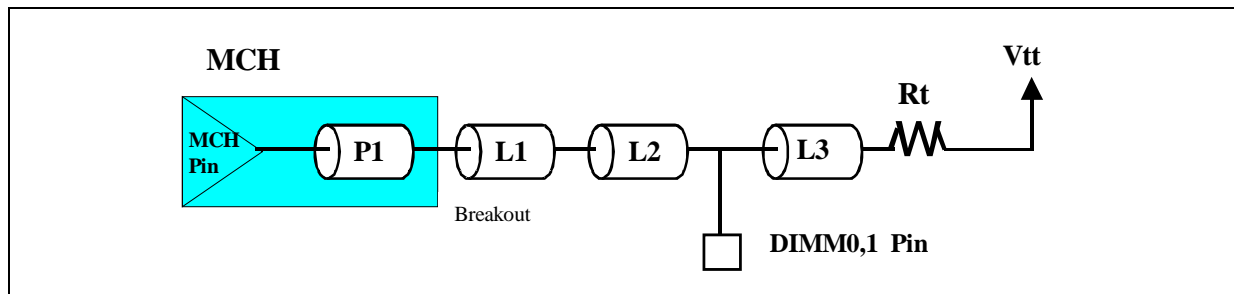
The MCH control signals that include the enable (SCKE) and chip select (SCS#) are source-clocked signals. One SCKE and SCS# are needed per row. SCKE and SCS# are tuned to SCMDCLK.

**Table 45. Control Signal to DIMM Mapping**

Control Signal Mapping (per Channel)	Relative To
SCKE[1:0]	DIMM 0
SCS[1:0]#	DIMM 0
SCKE[3:2]	DIMM 1
SCS[3:2]#	DIMM 1

Figure 54, Figure 55 and Figure 46 depict the recommended topology and layout guidelines for the DDR control signals.

**Figure 54. Control Signal Group Routing Topology**



**Table 46. Control Signal Group Routing Guidelines (Sheet 1 of 2)**

Parameter	Definition
Signal group	SCKE[3:0], SCS#[3:0]
Topology	Point-to-point with parallel termination
Reference plane	Ground referenced
Layer assignment	Layers 1 and 6 - Microstrip
Characteristic trace impedance ( $Z_0$ )	$60 \Omega \pm 15\%$
Nominal trace width	5 mils
Minimum trace to trace spacing (see breakout and DIMM field exception below)	12 mils
Minimum isolation spacing to non-DDR signals	20 mils

**NOTES:**

1. The actual motherboard routed length to each DIMM must fall within the range defined by the clock length matching formulas, based on the clock target length. The length limits defined in this table represent absolute limits for acceptable signal integrity.
2. Power distribution vias from Rt to VTT are not included in via count.
3. The reduced spacing exception in the DIMM field refers to total reduced spacing length. This region may include either DIMM field as well as the routing segment to Rt.

**Table 46. Control Signal Group Routing Guidelines (Sheet 2 of 2)**

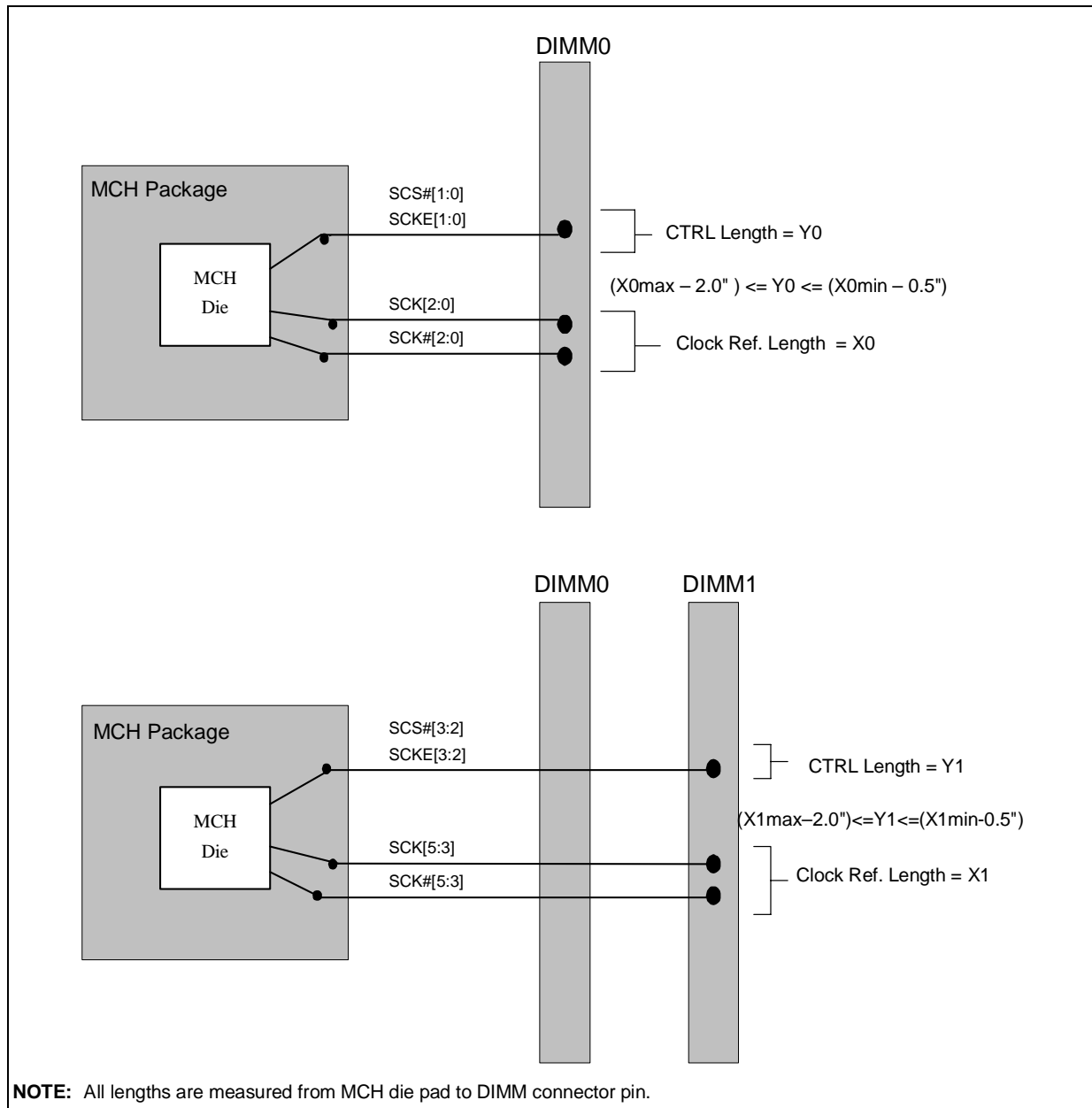
Parameter	Definition
Package length (P1)	750 mils $\pm$ 500 mils (see package length report)
Breakout length (L1)	Max = 550 mils
Total length (L1+ L2), MCH to first DIMM pin	Min = 1.5 inches Max = 5.0 inches
Trace length (L3), last DIMM pin to parallel termination resistor pad	Max = 1.2 inches
Parallel termination resistor (Rt)	47 $\Omega \pm 5\%$
Maximum recommended motherboard via count	2
CTRL to SCMDCLK length matching (Total length including package)	(CLKmax - 2.0 inches) < CTRL < (CLKmin - 0.5 inch) See length matching section for details
Breakout exceptions (Reduced geometries for MCH breakout region)	5 mil spacing to other DDR signals allowed Maximum breakout length is 0.5 inch
DIMM field exceptions (Reduced geometries for DIMM pin field region)	5 mil spacing to other DDR signals allowed Maximum reduced spacing length is 1.5 inches total.

**NOTES:**

1. The actual motherboard routed length to each DIMM must fall within the range defined by the clock length matching formulas, based on the clock target length. The length limits defined in this table represent absolute limits for acceptable signal integrity.
2. Power distribution vias from Rt to VTT are not included in via count.
3. The reduced spacing exception in the DIMM field refers to total reduced spacing length. This region may include either DIMM field as well as the routing segment to Rt.



**Figure 55. Control Signal to Clock Length Matching Requirements**

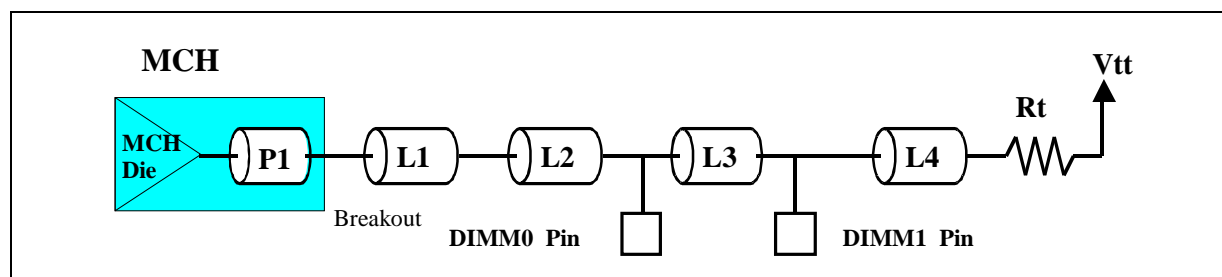


## 6.6.4 Address/Command Signal Group Routing Guidelines (SMA[12:0], SBA[1:0], SRAS#, SCAS#, SWE#)

The MCH address/command signals are source-clocked signals that include memory address signals SMA[12:0], SBA[1:0], SRAS#, SCAS#, SWE#. The address/command signals are tuned to SCMDCLK.

The diagrams and table below depict the recommended topology and routing guidelines for the DDR address/command signals.

**Figure 56. DDR Address/Command Routing Topology**



**Table 47. Address/Command Signal Group Routing Guidelines (Sheet 1 of 2)**

Parameter	Definition
Signal group	SMA[12:0], SBA[1:0], SRAS#, SCAS#, SWE#
Topology	Daisy Chain with Parallel Termination
Reference plane	Ground Referenced
Layer assignment	Layers 1 and 6 - Microstrip
Characteristic trace impedance (Zo)	L2 segment: 50 $\Omega \pm 15\%$ L1, L3, and L4 segments: 60 $\Omega \pm 15\%$
Nominal trace width	L2 segment: 7 mils L1, L3, and L4 segments: 5 mils
Minimum trace to trace spacing (see breakout and DIMM field exceptions below)	12 mils
Minimum isolation spacing to non-DDR Signals	20 mils
Package length (P1)	750 mils $\pm$ 500 mils (see package length report)
Breakout length (L1)	Max = 500 mils
Total length (L1 + L2), MCH to First DIMM pin	Min = 1.5 inches
Trace length (L3), First DIMM pad to Last DIMM pin	Min = 0.2 inch Max = 0.6 inch
Total motherboard length (L1 + L2 + L3), MCH ball to last DIMM pin	Max = 5.0 inches

**NOTES:**

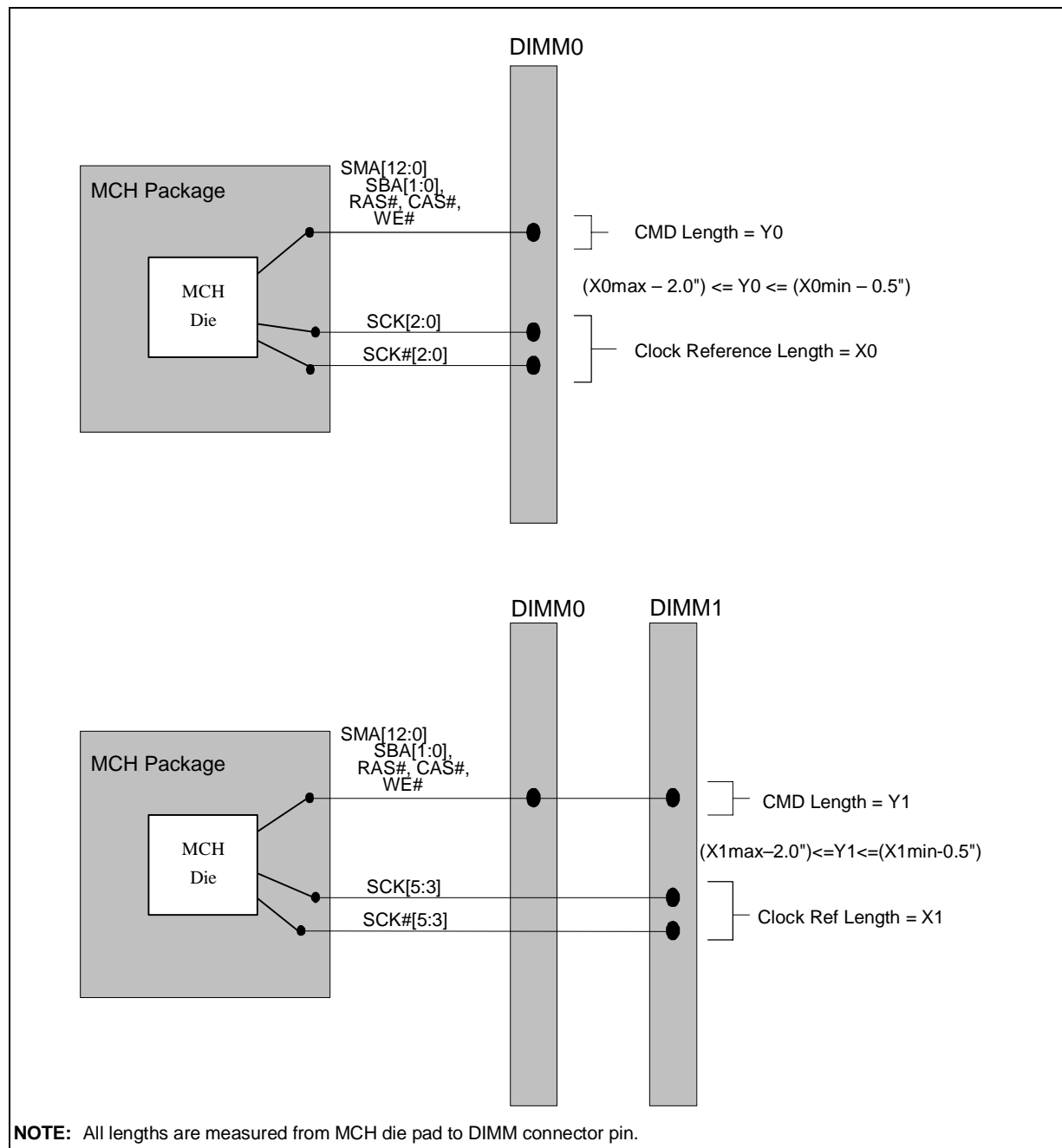
1. The actual motherboard routing length to each DIMM must fall within the range defined by the clock length matching formulas, based on the clock target length. The limits defined in this table represent absolute limits for acceptable signal integrity.
2. The routing distance between DIMMs may be as little as 0.2 inch or as much as 0.6 inch. However, in a given design the amount of variance across a signal group should be minimized in order to facilitate length matching.
3. Power distribution vias from Rt to VTT are not included in via count.

**Table 47. Address/Command Signal Group Routing Guidelines (Sheet 2 of 2)**

Parameter	Definition
Total length (P1 + L1+ L2 + L3), MCH die to last DIMM pin	Max = 5.3 inches
Trace length (L4), Last DIMM pad to parallel termination resistor pin	Max = 1.0 inch
Parallel termination resistor (Rt)	47 $\Omega$ $\pm$ 5%
Maximum recommended motherboard via count per signal	2
CMD to SCMDCLK length matching (total length including package)	(CLKmax - 2.0 inches) < CMD < (CLKmin - 0.5 inch) See length matching section for details
Breakout exceptions (reduced geometries for MCH breakout region)	5 mil spacing to other DDR signals allowed Maximum breakout length is 0.5 inch
DIMM field exceptions (reduced geometries for DIMM pin field region)	5 mil spacing to other DDR signals allowed Maximum reduced spacing length is 1.5 inches total

**NOTES:**

1. The actual motherboard routing length to each DIMM must fall within the range defined by the clock length matching formulas, based on the clock target length. The limits defined in this table represent absolute limits for acceptable signal integrity.
2. The routing distance between DIMMs may be as little as 0.2 inch or as much as 0.6 inch. However, in a given design the amount of variance across a signal group should be minimized in order to facilitate length matching.
3. Power distribution vias from Rt to VTT are not included in via count.

**Figure 57. Address/Command to Clock Length Matching Requirements**


## 6.6.5 Data Signal Group Routing Guidelines (SDQ[63:0], SDQS[8:0], SECC[7:0])

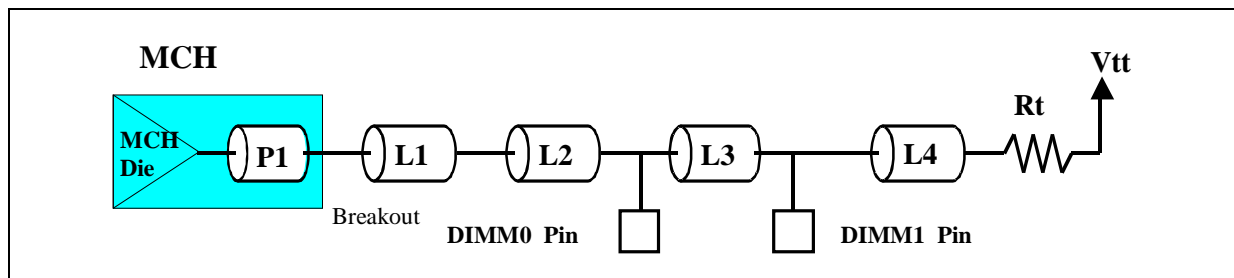
The MCH DDR data signals are source synchronous signals. Each channel includes the 64-bit wide data bus, nine data strobe signals, and eight ECC signals. There is an associated data strobe (SDQS) for each data group and ECC signal group. Table 48 summarizes the SDQ and SECC to SDQS mapping. SDQ and SECC signals are tuned to their associated SDQS signal, and SDQS signals are tuned to SCMDCLK lengths.

**Table 48. SDQ and SECC to SDQS Mapping**

SDQ/SDM	SDQS
SDQ[8:0]	SDQS0
SDQ[15:8]	SDQS1
SDQ[23:16]	SDQS2
SDQ[31:24]	SDQS3
SDQ[39:32]	SDQS4
SDQ[47:40]	SDQS5
SDQ[55:48]	SDQS6
SDQ[63:56]	SDQS7
SECC[7:0]	SDQS8

The diagrams and tables below depict the recommended topology and layout routing guidelines for the DDR data signals.

**Figure 58. Data Signal Routing Topology**



**Table 49. Data Signal Group Routing Guidelines (Sheet 1 of 2)**

Parameter	Definition
Signal group	SDQ[63:0], SECC[7:0], SDQS[8:0]
Topology	Daisy Chain with Parallel Termination
Reference plane	Ground Referenced
Layer assignment	Layers 1 and 6 - Microstrip
Characteristic trace impedance ( $Z_0$ )	L2 Segment = $50 \Omega \pm 15\%$ (40 $\Omega$ for length > 5.7 inches) L1, L3 and L4 Segments = $60 \Omega \pm 15\%$
Nominal trace width	L2 Segment = 7 mils (11 mils for length > 5.7 inches) L1, L3 and L4 Segments = 5 mils
Minimum trace to trace spacing (see breakout and DIMM field exception below)	SDQ signals: 12 mils (15 mils for length > 5.7 inches) SDQS signals: 15 mils (17 mils for length > 5.0 inches)
Minimum isolation spacing to non-DDR signals	20 mils
Package length (P1)	750 mils $\pm$ 500 mils (see package length report)
Breakout length (L1)	Max = 550 mils
Total length (L1 + L2), MCH ball to first DIMM pin	Min = 1.5 inches
Trace length (L3), 1st DIMM pad to last DIMM pin	Min = 0.2 inch Max = 0.6 inch
Total length (L1 + L2 + L3), MCH ball to last DIMM pin	Max = 6.5 inches
Total Length (P1 + L1 + L2 + L3), MCH Die to last DIMM pin	Max = 6.9 inches
Trace length (L4), last DIMM pin to termination resistor pad	Max = 1.0 inch
Parallel termination resistor ( $R_t$ )	$56 \Omega \pm 5\%$
Maximum recommended motherboard via count per signal	2
SDQS to SCMDCLK length matching (total length including package)	(CLKmax - 2.0 inches) < SDQS < (CLKmin + 1.0 inch) See length matching section for details

**NOTES:**

1. The actual MB routing length to each DIMM must fall within the range defined by the clock length matching formulas, based on the clock target length. The limits defined in this table represent absolute limits for acceptable signal integrity.
2. The width and spacing rules for DQ and DQS routing are length dependent as shown in the table. Note that the length cutoff of 5.7 inches refers to the total combined MB and package length (P1 + L1 + L2 + L3).
3. When implementing the wider 11 mil trace width rule on long byte lanes the wider trace width should be implemented on all DQ and DQS signals within a byte lane or none. If required the higher trace width should be achieved incrementally by transitioning to 7 mils for up to 1.0 inch additional length following the breakout region before transitioning to 11 mils. If required an additional region of 9 mils could be used for up to 1.0 inch additional length following the 7 mil region. It is not required that these stepping lengths be matched exactly across each trace in a byte lane. Normal L2 spacing rules apply for the transition region.
4. The routing distance between DIMMs (L3) may be as little as 0.2 inch or as much as 0.6 inch; however, in a given design the amount of variance across a signal group or bus should be minimized in order to facilitate and optimize length matching.
5. The DIMM pin field exception region is defined to include the DIMM pin field and termination region for each channel, but also includes any reduced spacing region in channel B routing required to route through the channel A pin field region.
6. Power distribution vias from  $R_t$  to VTT are not included in via count.

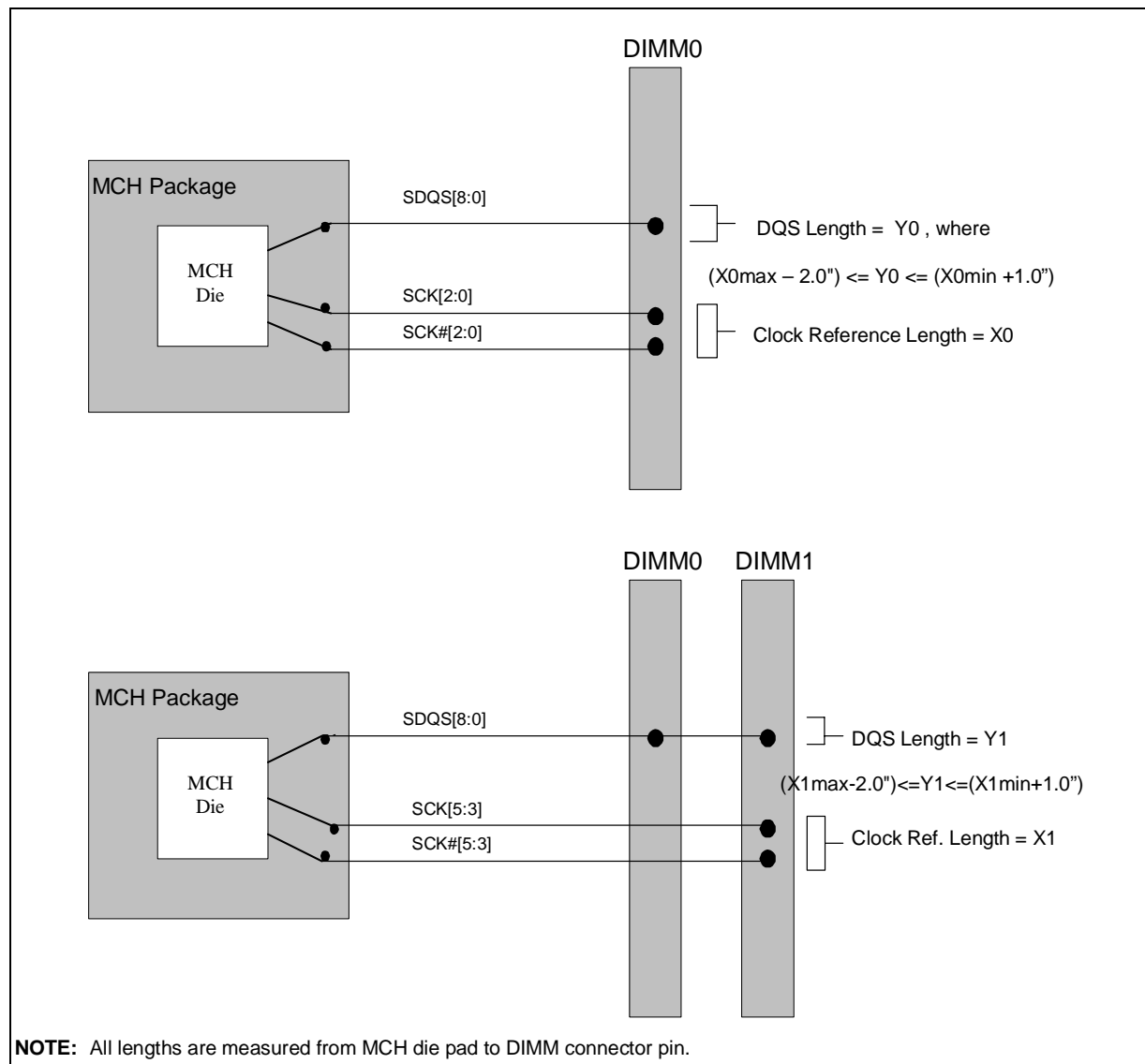
**Table 49. Data Signal Group Routing Guidelines (Sheet 2 of 2)**

Parameter	Definition
SDQ/SECC to SDQS length matching (total length including package)	Match SDQ/SECC to SDQS, to $\pm 25$ mils, per byte lane See length matching sections
Breakout exceptions (reduced geometries for MCH breakout region)	5 mil trace allowed 5 mil spacing to other DDR signals allowed Maximum breakout length is 0.5 inch
DIMM Field Exceptions (reduced geometries for DIMM pin field region)	5 mil trace allowed 5 mil spacing to other DDR signals is allowed (DQ only) 10 mil spacing to other DDR signals is allowed (DQS only) Maximum reduced spacing length is 2.5 inches total

**NOTES:**

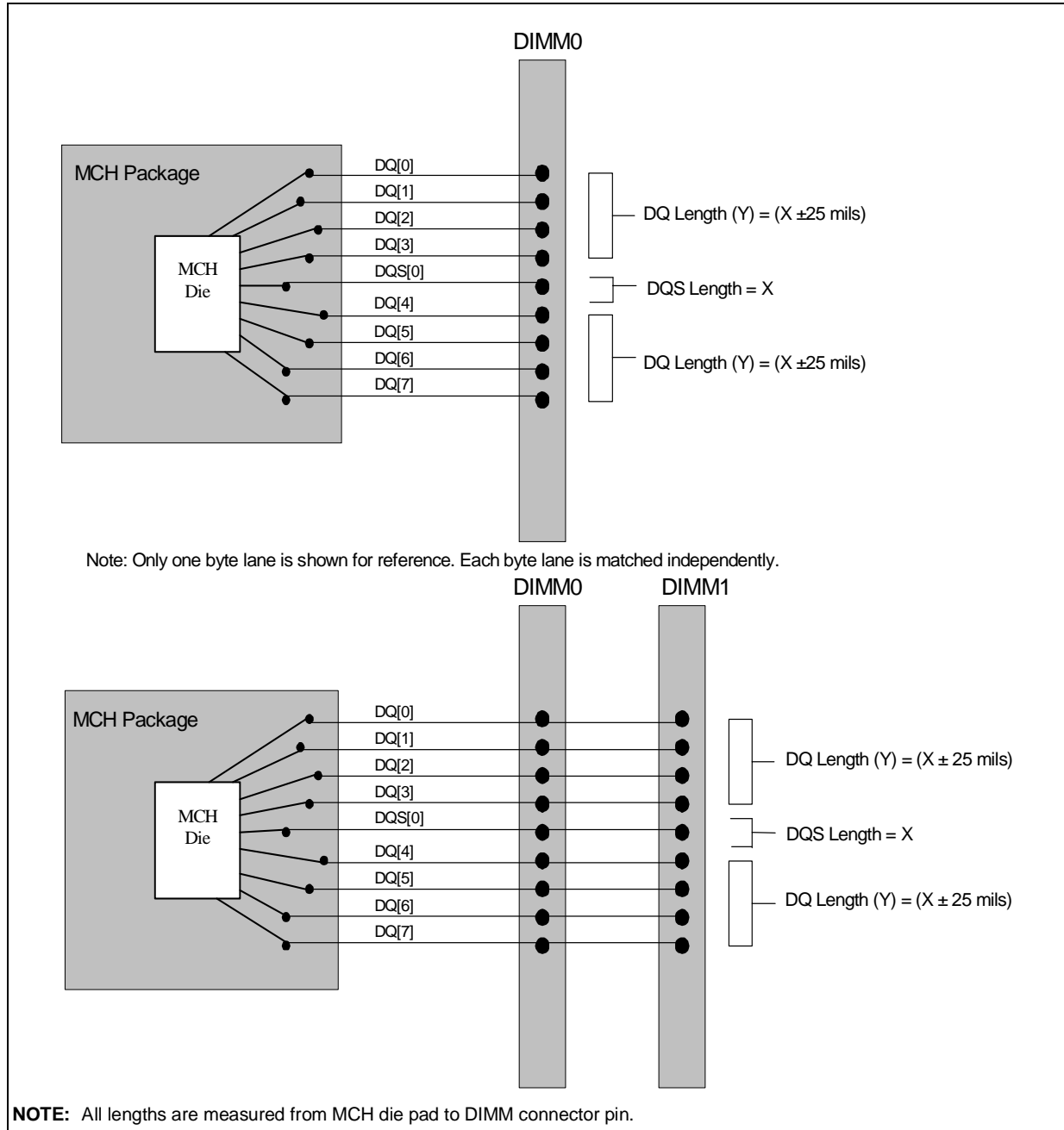
1. The actual MB routing length to each DIMM must fall within the range defined by the clock length matching formulas, based on the clock target length. The limits defined in this table represent absolute limits for acceptable signal integrity.
2. The width and spacing rules for DQ and DQS routing are length dependent as shown in the table. Note that the length cutoff of 5.7 inches refers to the total combined MB and package length ( $P1 + L1 + L2 + L3$ ).
3. When implementing the wider 11 mil trace width rule on long byte lanes the wider trace width should be implemented on all DQ and DQS signals within a byte lane or none. If required the higher trace width should be achieved incrementally by transitioning to 7 mils for up to 1.0 inch additional length following the breakout region before transitioning to 11 mils. If required an additional region of 9 mils could be used for up to 1.0 inch additional length following the 7 mil region. It is not required that these stepping lengths be matched exactly across each trace in a byte lane. Normal L2 spacing rules apply for the transition region.
4. The routing distance between DIMMs ( $L3$ ) may be as little as 0.2 inch or as much as 0.6 inch; however, in a given design the amount of variance across a signal group or bus should be minimized in order to facilitate and optimize length matching.
5. The DIMM pin field exception region is defined to include the DIMM pin field and termination region for each channel, but also includes any reduced spacing region in channel B routing required to route through the channel A pin field region.
6. Power distribution vias from  $R_t$  to VTT are not included in via count.

Figure 59. SDQS to Clock Length Matching Requirements





**Figure 60. SDQ/SECC to SDQS Length Matching Requirements**



## 6.7 One-DIMM-per-Channel Design Exceptions

In a one-DIMM-per-channel design there are several signals that will not be needed, compared to a two-DIMM-per-channel design. These signals are second-DIMM specific, and if there is only one DIMM on the channel they do not need to be routed. These unused signals are:

SCMDCLK[3:5] and SCMDCLK[3:5]#

SCS[3:2]

SCKE[3:2]

**Note:** If X-Or chain testing will be used in the manufacturing process then these unused signals will require a test point. Please see the *Intel 875P Memory Controller Hub (MCH) Datasheet* or the *Intel E7210 MCH Memory Controller Hub (MCH) Datasheet* for more information on X-Or chain testing.

The layout guidelines in this chapter were developed with the following design assumptions:

- A standard 6-layer motherboard stack up
- Two DDR channels, with 1 DIMM each
- **All** channel A DDR signals are routed on layer 1
- **All** channel B DDR signals are routed on layer 6

Signals routed on layer 6 (bottom) may use the last row of pins on the DIMM connector to transition to layer 1 (top) instead of using a via to get back to the top layer before reaching the termination resistors.

### 6.7.1 Ground Referencing Exceptions

Due to lighter loading of the DDR channel in a one DIMM per channel design, it is acceptable to power reference a DDR signal from the last DIMM pin with which it connects to its termination resistor.

The benefit of using this limited power referencing scheme may be improved power delivery. By referencing these regions of the DDR channel to the 2.6 V plane for DDR it is possible to deliver power to the DIMMs with these floods.

## 6.8 Miscellaneous Signals

### 6.8.1 TESTP[4:11] and TESTP[17:24] Termination

The TESTP[4:11] and TESTP[17:24] signals are not used in the MCH implementation; however, these MCH balls may be left as no-connects on the motherboard.

## 6.8.2 DDR VREF Overview

The DDR system memory reference voltage (VREF) is used by the DDR devices to compare the input signal levels of the data, command and control signals, and is also used by the MCH to compare the input data signal levels.

Three VREF circuits are used to generate the VREF voltage for the DDR interface, one for the MCH and one for each DDR channel at the DIMMs.

### 6.8.2.1 DDR VREF at the MCH

On the MCH there are two VREF pins, SMVREF\_A and SMVREF\_B. These two pins are connected inside the package. As such, only one of these pins requires a VREF voltage divider; the other should be decoupled.

On the reference design, the VREF circuitry is attached to SMVREF\_B and the decoupling is attached to SMVREF\_A. The VREF divider is shown in [Figure 61](#) below. It should be generated from a typical resistor divider using 1% tolerance resistors. The VREF resistor divider should be placed no further than 1.0 inch from the SMVREF pin being used. The VREF signal should be routed with as wide a trace as possible (12 mils minimum width) and isolated from other signals with a minimum of 12-mils spacing. In the MCH breakout a 7 mil trace may be used, if needed, for up to a maximum length of 350 mils.

**Figure 61. DDR VREF Generation Example Circuit at the MCH**

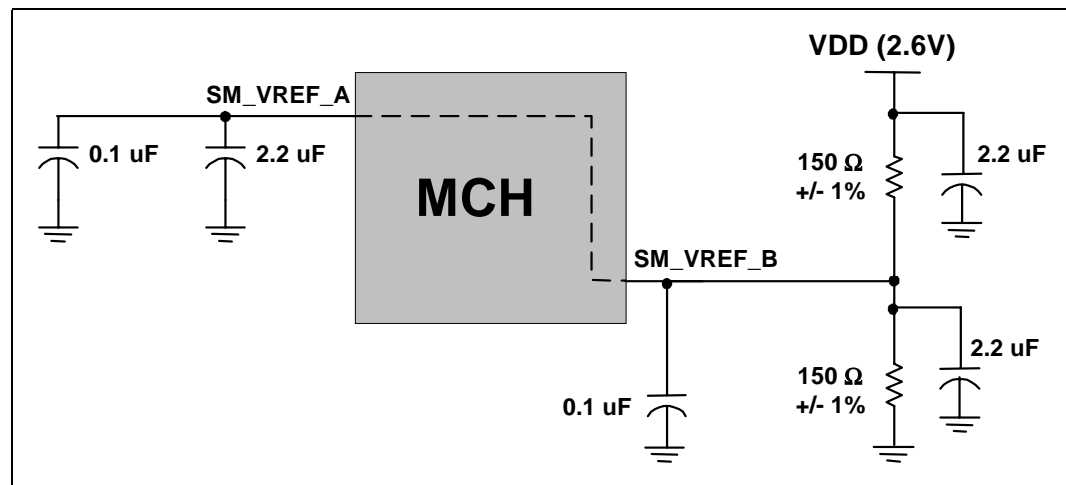


Table 50. DDR VREF Generation Requirements at the MCH

Parameter	Guideline
VREF routing	Minimum 12 mils wide and separated from other traces by a minimum of 12 mils spacing, except during breakout, which allows for 7 mil spacing to other signals for no more than 350 mils.
Voltage divider	Place resistor divider consisting of two 150 $\Omega$ 1% resistors within 1.0 inch of the MCH pin being used.
Decoupling at the resistor divider	Two, 2.2 $\mu$ F capacitors. Place one 2.2 $\mu$ F capacitor between SM_VREF and ground and the other between VDD (2.6 V) and ground. <b>NOTE:</b> The 2.2 $\mu$ F capacitor between VDD (2.6 V) and ground is only need if no other decoupling on the 2.6 V plane is near by.
Decoupling at SM_VREF source pin	Place one 0.1 $\mu$ F capacitor as close as possible to the MCH SM_VREF source pin.
Decoupling for un-used SM_VREF pin	Place two capacitors, a 2.2 $\mu$ F and a 0.1 $\mu$ F, on the unsourced SM_VREF pin.

### 6.8.3 DDR VREF at the DIMMs

A separate DDR VREF circuit is needed for each DDR channel.

The VREF divider for each channel is shown in Figure 62 below. It should be generated from a typical resistor divider using 1% tolerance resistors. The VREF resistor divider should be placed no farther than 1.0 inch from the VREF pin being used. The VREF signal should be routed with as wide a trace as possible (12 mils minimum width) and isolated from other signals, with a minimum of 12 mils spacing.

Figure 62. DDR VREF Generation Example Circuit at the DIMMs

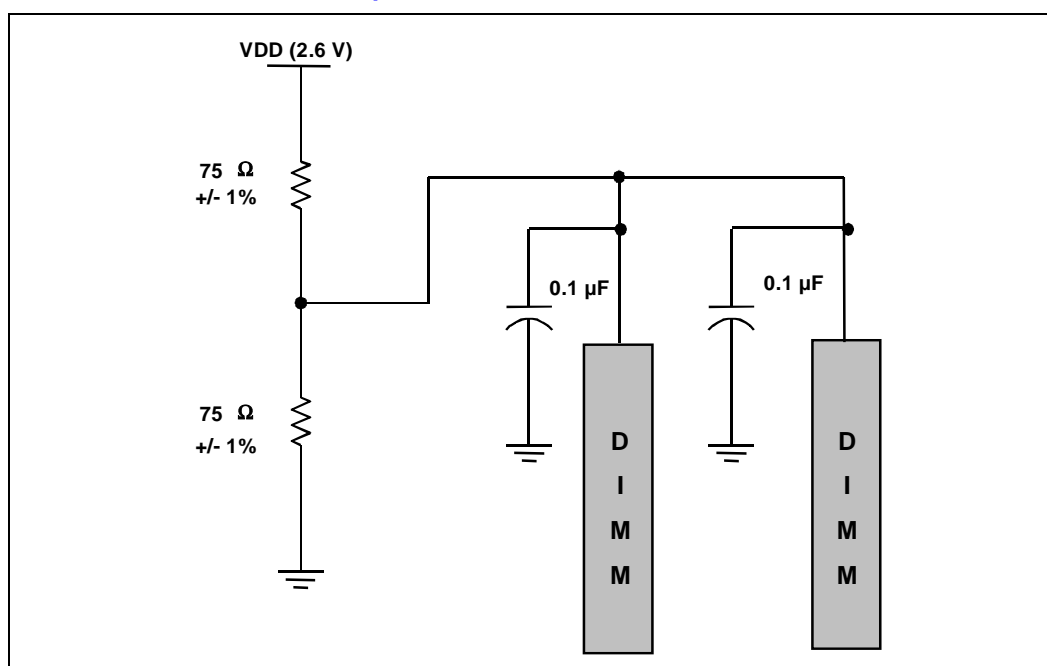


Table 51. DDR VREF Generation Requirements at the DIMMs

Parameter	Guideline
VREF routing	Minimum 12 mils wide and separated from other traces by a minimum of 12 mils spacing.
Voltage divider	Place resistor divider consisting of two 75 $\Omega$ 1% resistors within 1.0 inch of the DIMM connectors.
Decoupling at the resistor divider	Two 0.1 $\mu$ F capacitors: one as close as possible to each DIMM VREF pin.

## 6.9 DDR Resistive Compensation (SMRCOMP) per Channel

The MCH uses a compensation signal to adjust the system memory buffer characteristics over temperature, process and voltage variations. The DDR system memory compensation (SMRCOMP) must be connected to the VDD (2.6 V) rail through a 42.2  $\Omega \pm 1\%$  resistor and a 42.2  $\Omega \pm 1\%$  to ground as shown in Figure 63.

An additional 2.2  $\mu$ F capacitor from 2.6 V to ground is needed at the resistor divider depending on whether the power is drawn from the flood or the package. If the resistor divider power is drawn from the flood, the 2.2  $\mu$ F capacitor is needed. If instead, the power is drawn from the package, the capacitor is not needed. See Figure 64 for an illustration of flood vs. package power sourcing.

Place the resistors and capacitor within 1.0 inch of the MCH package; however, they should be placed as close as possible to the MCH. The compensation signal and the VDD trace should be routed a minimum of 12 mils wide and isolated from other signals with a minimum of 10 mils spacing.

Figure 63. DDR (SMRCOMP) Resistive Compensation

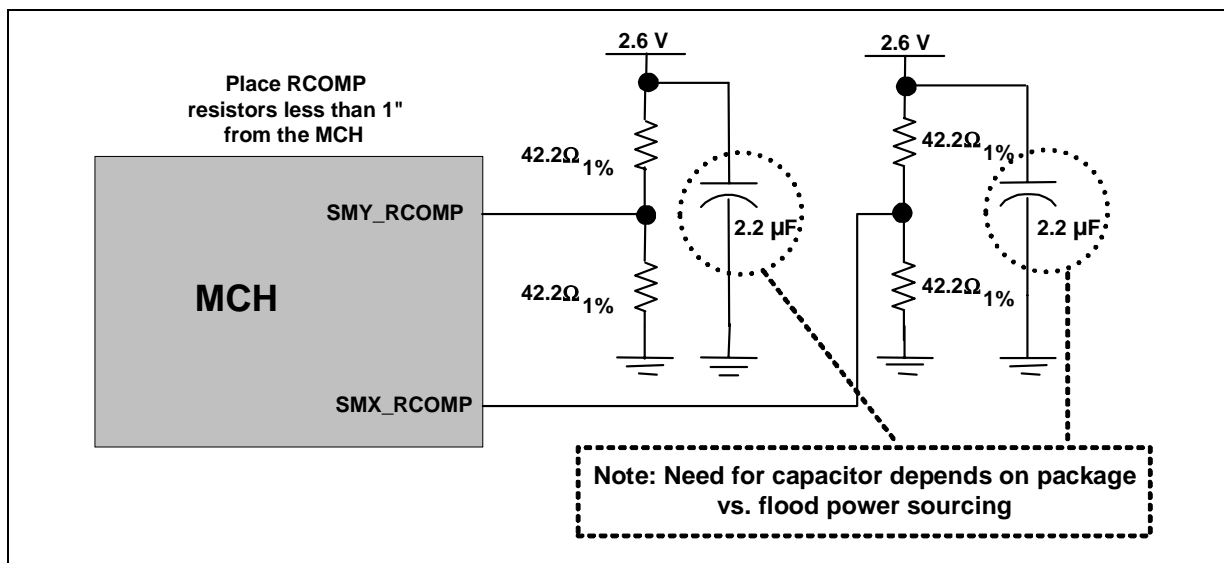


Figure 64. DDR SMRCOMP Resistor Divider Power (Flood vs. Package)

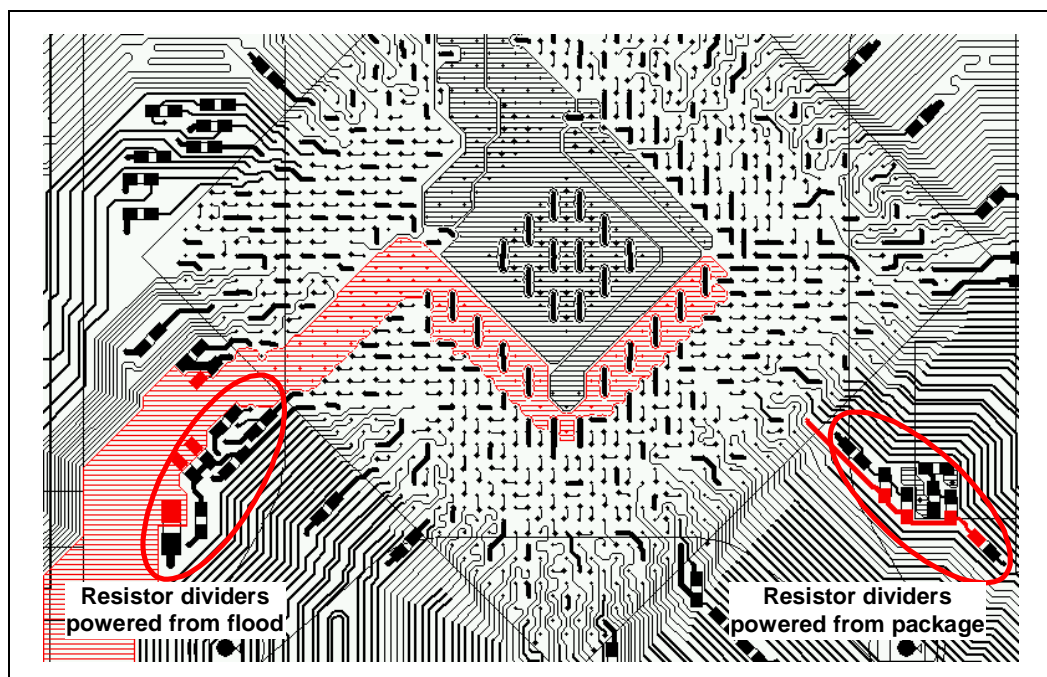


Table 52. DDR SMRCOMP Requirements

Parameter	Guideline
RCOMP resistors	42.2 $\Omega$ 1% pulled to VDD (2.6 V), 42.2 $\Omega$ 1% pulled to ground; place resistors within 1.0 inch of the MCH.
RCOMP routing	Minimum trace width of 12 mils and minimum spacing from other signals of 10 mils.
Decoupling	Decouple each RCOMP circuit as shown in Figure 63 and Figure 64 with 2.2 $\mu$ F capacitors.

The SMRCOMP VOH and VOL signals must be connected to the VDD (2.6 V) rail and ground through resistor dividers as shown in Figure 65 below. A 2.2  $\mu$ F capacitor from 2.6 V to ground is required at the resistor divider depending on whether the power is drawn from the flood or the package. If the resistor divider power is drawn from the flood, the 2.2  $\mu$ F capacitor is needed. If instead, the power is drawn from the package, the capacitor is not needed. See Figure 64 for an illustration of flood vs. package power sourcing.

If the resistor divider is more than 1 inch from the MCH package, decouple with a 1  $\mu$ F capacitor at the resistor divider. Place the 0.01  $\mu$ F capacitor within 1.0 inch of the MCH package; however, it should be placed as close as possible to the MCH. The compensation signal and the VDD trace should be routed a minimum of 12 mils wide and isolated from other signals with a minimum of 10 mils spacing.

Figure 65. DDR RCOMP VOH and VOL Circuitry

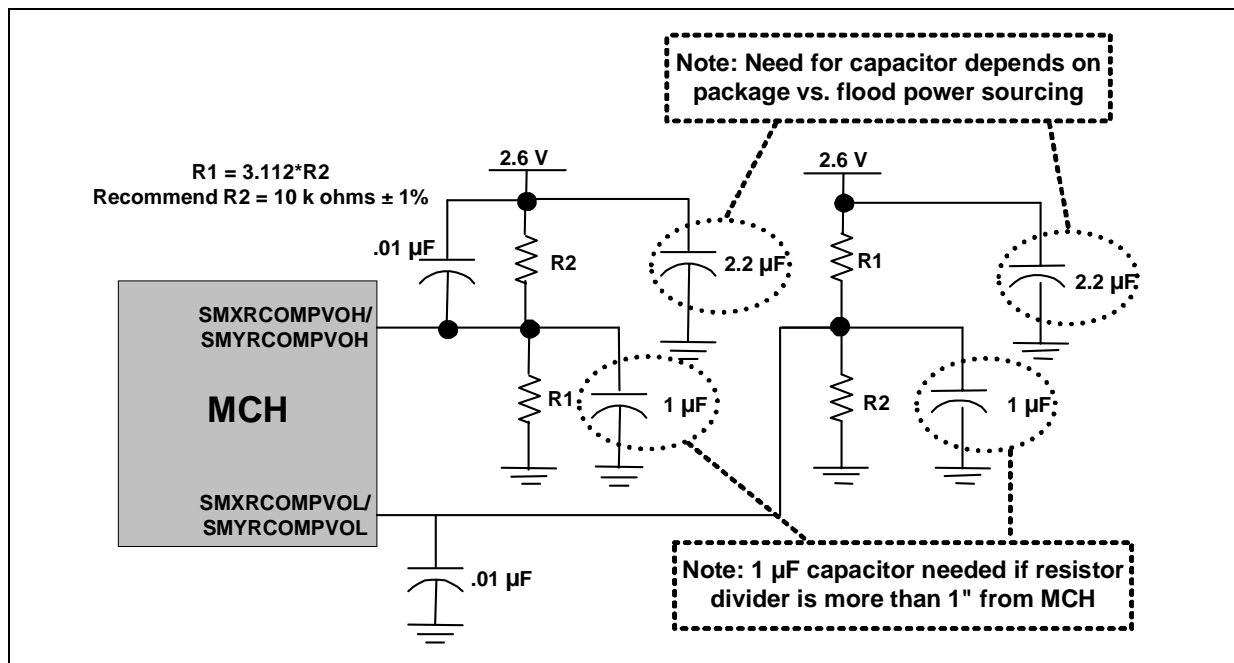


Table 53. DDR RCOMP VOH and VOL Requirements

Parameter	Guideline
RCOMP resistors	$R1 = 3.112 * R2$ , Recommend $R2 = 10 \text{ k } \Omega \pm 1\%$
RCOMP routing	Minimum trace width of 12 mils and minimum spacing from other signals of 10 mils
Decoupling	Place the $0.01 \mu\text{F}$ capacitors no more than 1 inch from the MCH. If the resistor divider is more than 1" from the MCH, place a $1 \mu\text{F}$ capacitor at the resistor divider. Decouple each VOH and VOL circuit as shown in Figure 65 and Figure 64 with $2.2 \mu\text{F}$ capacitors.

# AGP 8X

# 7

This AGP 8X section applies only to the 875P MCH. AGP 8X is not a feature of the E7210 MCH. See the *Intel E7210 MCH External Design Specification* for pin definitions.

**Note:** For the E7210 MCH, the GVREF circuitry must still be connected. See [Section 7.2.4.4](#). All other signals can be left as no connect.

**Caution:** **AGP\_VCC pins on the E7210 MCH must be connected to the 1.5 V power plane.**

**Caution:** All signals in this section are assumed to be routed microstrip. If you choose to route on inner layers, you must perform thorough signal integrity and timing simulations on each design.

## 7.1 AGP 3.0

For AGP 2.0 mode, the peak bandwidth is 1066 MBytes/s and this is achieved by using a quad clocked data transfer methodology. In AGP 3.0 (8X speed) mode the data is octal-pumped from the common clock frequency of 66 MHz achieving a peak bandwidth of 2.1 GBytes/s. In order to achieve these higher data rates across the standard AGP connector, AGP 3.0 mode uses a parallel-terminated bus with low signal swings of about 0.8 V, ground referenced. The AGP 2.0 mode 1.5 V I/O power supply is used for backward compatibility for designs which need to be universal low voltage.

If the AGP port is not used leave all the AGP interface signals disconnected on the E7210 MCH except AGPREF, GRCOMP, and AGP\_SWING. See [Section 7.2.4.3](#) through [Section 7.2.4.5](#) for implementation details.

### 7.1.1 AGP Interface Signal Groups

This section describes layout and routing guidelines to ensure a robust AGP interface design. These guidelines ensure that the AGP specifications may be met and that the motherboard will function properly. This solution is based on the reference platform. Other implementations of AGP routing may be used with proper simulation based on parameters specified in the design guide available at [www.agpforum.org](http://www.agpforum.org).

[Table 54](#) and [Table 55](#) show the signal groups and associated strobes.



**Table 54. Signal Groups**

Group	Signals	Signal Type
1	GAD[15:0], DBI_LO, GCBE[1:0], GADSTBF0, GADSTBS0	Source Synchronous
2	GAD[31:16], GCBE[3:2], DBI_HI, GADSTBF1, GADSTBS1	Source Synchronous
3	GSBA#[7:0], GSBSTBF, GSBSTBS	Source Synchronous
4	GIRDY, GTRDY, GFRAME, SERR, PERR, GSTOP, GDEVSEL, GPAR	Common Clock
5	GRBF, GWBF, GREQ, GGNT	Common Clock

**Table 55. Associated 1st and 2nd Strokes**

Group	Signals	1st Strobe	2nd Strobe
1	GAD[15:0], GCBE[1:0]	GADSTBF0	GADSTBS0
2	GAD[31:16], GCBE[3:2], DBI_HI, DBI_LO	GADSTBF1	GADSTBS1
3	GSBA#[7:0]	GSBSTBF	GSBSTBS

## 7.2 AGP 8X Implementations

### 7.2.1 Motherboard Layout Recommendations

The traces should be as short and direct as route length matching rules allow. Avoid changing the power plane reference during routing. Any change in reference plane will need to be bypassed by capacitors placed as close to the vias as possible. The power plane design should be considered during the entire design process and not left to the end. The planes should be cut so that the number of “neckdown” points are minimized.

### 7.2.2 AGP 8X Routing Guidelines

The AGP 8X signals must be routed directly from the 875P MCH to the AGP connector with all signals referenced to ground. A consistent ground reference plane must be maintained at all times. In addition, all signals within a address/data group must be routed on the same layer (see [Table 55](#) for address/data groups). [Table 56](#) summarizes the routing parameters for the AGP interface.

The 8X mode source synchronous signals and the 66 MHz clock signal should not cross any plane splits (crossing two separate voltage planes) If the common clock signals cross split planes, they should be simulated to ensure signal quality is not compromised.

Since the strobe signals (GADSTBF0, GADSTBS0, GADSTBF1, GADSTBS1, GSBSTBS, and GSBSTBF) act as clocks on the source synchronous AGP interface, special care should be taken when routing these signals. In an AGP 8X design the strobe signal spacing should be routed together also but separated by 5/1 S/H rule to each other and to any other signal routed adjacent to the strobe. This recommendation is intended to reduce the crosstalk noise coupled onto the strobes from other signals on the bus, as well as to reduce the noise coupled from the strobe signals onto adjacent lines. The strobe pair must be length matched to less than 10 mils.

Table 56. Motherboard Interconnect Requirements

Parameter	Min	Max	Units	Notes
<b>Source Synchronous Signals (Groups 1, 2 and 3)</b>				
Interconnect Length	0.5	3.5	inches	2
Strobe-to-Strobe (Interconnect Mismatch)		5	mils	2
Strobe-to-Data (Interconnect Mismatch)		25	mils	3
Data-to-Data Spacing	3/1		S/H	4
Strobe-to-Strobe Spacing	5/1		S/H	4
Strobe-to-Data Spacing	5/1		S/H	4
Trace Impedance	54	66	$\Omega$	
Connector Breakout		200	mils	10
875P MCH Breakout		550	mils	
<b>Common Clock Signals (Groups 4 and 5)</b>				
Interconnect Length	0.5	3.5	inches	2
Common Clock-to-Common Clock Spacing	2/1		S/H	4
Common Clock-to-Data Spacing	3/1		S/H	4
Common Clock-to-Strobe Spacing	5/1		S/H	4
Trace Impedance	54	66	$\Omega$	
Connector Breakout		200	mils	10
875P MCH Breakout		550	mils	

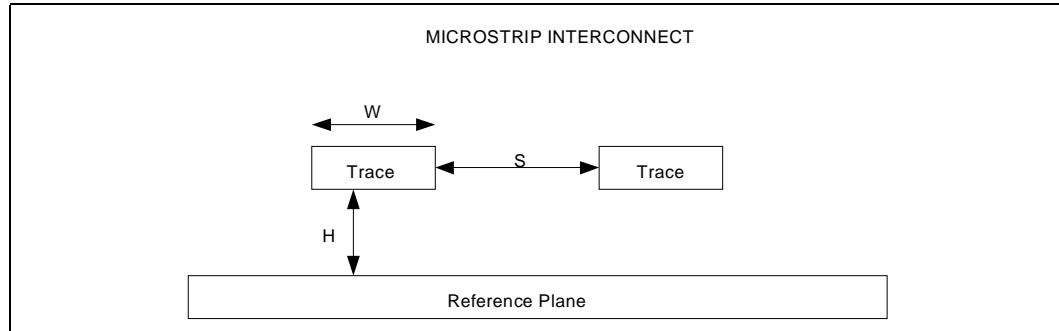
**NOTES:**

1. All interconnects must be ground referenced.
2. Worst-case interconnect skews listed in this table are based on simulations that take into account likely layout topologies and a wide range of interconnect. Listed trace lengths include pin-to-trace breakout and trace-to-connector fan-in/out.
3. This mismatch budget applies to the combined trace lengths of the package **and** board signals. Further, note that the set of 16 data signals and the corresponding strobes, etc., must be routed on the same PCB layer(s).
4. Parameter refers to the Space-to-Height ratio of spacing between signal traces and the height above the associated ground plane. Definitions for microstrip and described in subsequent text.
5. Sum of all interconnect skew contributors, including crosstalk, interconnect mismatch, etc., across the entire channel (including package and connector).
6. Propagation delay must account for all contributors up to the connector pins.
7. Effective impedance incorporates all coupling effects including crosstalk.
8. This represents the contribution to skew on the motherboard and includes **all** causes, not just interconnect.
9. Package information is added here for simple reference. Flip-chip packaging is highly recommended.
10. This is the fan-in/out length that does not follow the normal trace separation requirements in the connector area on the motherboard and the edge fingers of the graphic cards.

Table 56 gives the routing rules for the control signals and clock lines. There are no external pull-up or pull down resistors for control signals on AGP 8X mode board design. The resistors are integrated inside the device buffers.

### 7.2.2.1 Board Constraints

Figure 66. Spacing to Dielectric Height Diagram



All AGP 3.0 mode source synchronous signals should be routed on a layer referenced to a ground plane. To minimize the effect of trace velocity difference between circuit board layers, the source synchronous signals within the same group should be routed on the same layer. The total number of trace via transitions should match within the group. Dummy vias should be used to match the total via count for each group.

In all cases, it is best to reduce the line length mismatch wherever possible to minimize timing variations. It is also best to separate the traces by as much as possible to reduce trace-to-trace coupling. The physical/electrical length matching requirements include compensation for the package length delta. For motherboard layouts, length matching is specified from pad to connector pins.

## 7.2.3 AGP Signal Noise Decoupling Guidelines

### 7.2.3.1 1.5 V AGP Connector Decoupling

The designer should ensure that the AGP connector is well decoupled. The following recommendations are derived from the *AGP Design Guide Rev 1.0, Section 1.5.3.3 Connector AC Signal Decoupling Requirements*:

The decoupling capacitors recommendations for the AGP connector are intended to address AC signaling issues and not power delivery issues. The main reason for not addressing power delivery issues with the motherboard connector decoupling is due to the connector inductance and the distance the capacitors are from the graphic device. These two factors negate much of the usefulness of the connector decoupling on the motherboard for power delivery purposes. The following recommendations for decoupling at the AGP connector on the motherboard:

- VCC3.3:
  - Three low ESL capacitors, 1  $\mu$ F or larger
  - One 22  $\mu$ F capacitor
  - One 100  $\mu$ F electrolytic capacitor

Each capacitor should be placed as close as possible to a VCC3.3 pair of pins on the connector.

- VDDQ:
  - Six low ESL capacitors, 1  $\mu$ F or larger

- One 22  $\mu$ F capacitor
- Two 100  $\mu$ F tantalum capacitors

Each capacitor should be placed as close as possible to a VDDQ pair of pins on the connector.

- +5 V:
  - One low ESL capacitor, 0.1  $\mu$ F or larger, placed as close as possible to the +5 V connector pins
- +12 V:
  - One low ESL capacitor, 0.1  $\mu$ F or larger
  - One 470 pF electrolytic capacitor placed as close as possible to the +12 V connector pin
- 3.3VAUX:
  - One low ESL capacitor, 0.1  $\mu$ F or larger, placed as close as possible to the 3.3VAUX connector pin(s)

## 7.2.4 Miscellaneous Signal Requirements

### 7.2.4.1 PERR

See [Figure 67](#) for a PERR reference circuit. The circuit will supply pull-down to ground during AGP 3.0 Mode operation and a pull-up to 1.5 V during AGP 2.0 Mode operation.

### 7.2.4.2 AGP 2.0 and AGP 3.0 Mode Detection

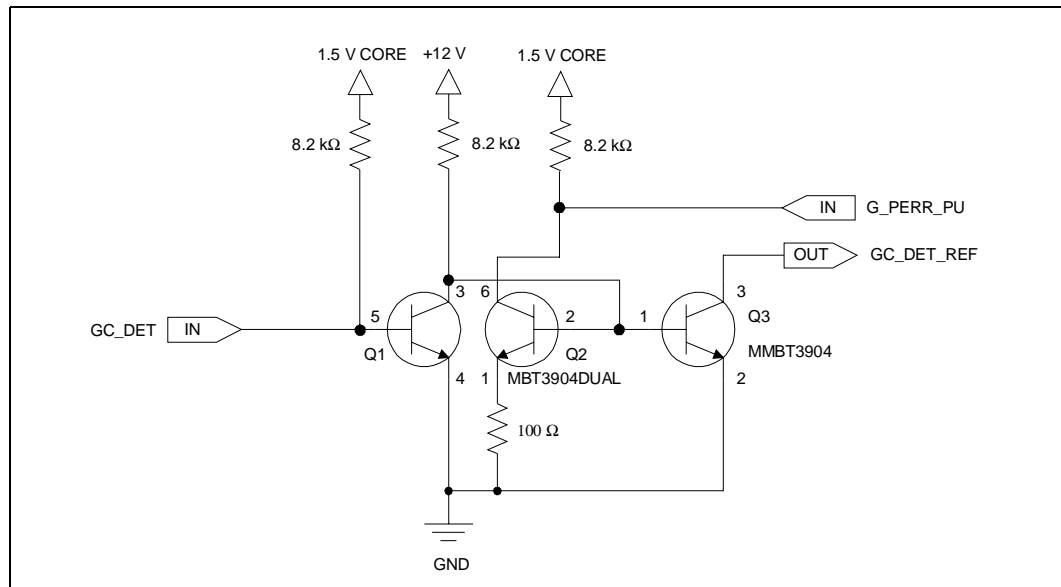
Two new signals are provided in the AGP 3.0 specification to allow for detection of an AGP 3.0 capable graphics card by the motherboard and an AGP 3.0 capable motherboard by the graphics card respectively.

- GC\_DET#: Pulled low by an AGP 3.0 graphics card and left floating by an AGP 2.0 graphics card.
- MB\_DET#: Pulled low by an AGP 3.0 motherboard and left floating by an AGP 2.0 motherboard.

The 875P MCH uses GC\_DET# to determine whether to generate VREF of 0.75 V (floating GC\_DET# for 2.0 graphics card) or 0.35 V (GC\_DET# low) to the graphics card. This is sent to the graphics card via the VREFCG pin on the AGP connector.

Refer to [Figure 67](#) for details on how to utilize the GC\_DET# for AGP 2.0 and AGP 3.0 modes of operation.

**Figure 67. AGP Mode Detection Circuit**



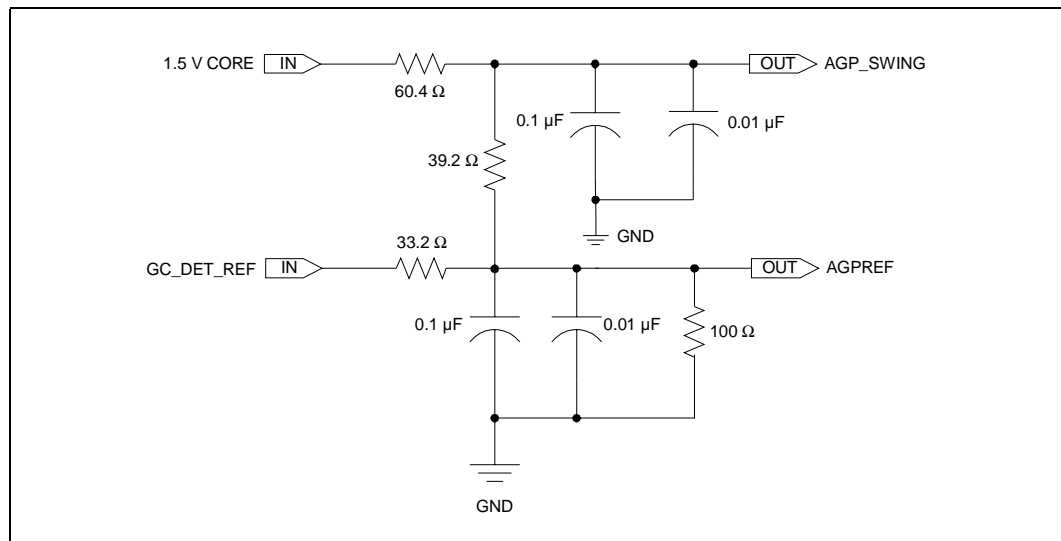
### 7.2.4.3 GRCOMP

These signals are used to calibrate the AGP buffers. The GRCOMP signals need to be pulled up to VDDQ through a 43 Ω resistor.

### 7.2.4.4 AGPREF

A complex AGPREF circuit is required to meet the reference voltage requirements for AGP 2.0 and 3.0 modes. See [Figure 68](#) for complete detailed information.

**Figure 68. GVREF/GSWING Circuit**



#### **7.2.4.5 AGP\_SWING**

Provide the reference voltages used by the GRCOMP circuits. AGP\_SWING is based on a resistor divider circuit and comes off of 1.5 V. The voltage level is 0.8 V and is the maximum voltage for the AGP signal bus in AGP 3.0 mode.

It is important to place the 0.01  $\mu$ F capacitors within 0.25 inch of the device pins (875P MCH, 6300ESB ICH, and AGP), and to place the 0.1  $\mu$ F capacitors close to the resistor circuit. See [Figure 68](#) for details.

# CSA Port

# 8

This section of the Design Guide describes the layout guidelines when implementing the Communications Streaming Architecture (CSA) port on the 875P MCH/E7210 MCH/6300ESB ICH chipset. The CSA port is a dedicated 11-bit connection between the 875P MCH/E7210 MCH and a Gigabit Ethernet (GbE) LAN controller, the 82547GI GbE controller. The CSA port provides a theoretical bandwidth of 266 MBytes/s. The CSA port is a point-to-point interface; therefore, it may only support one device.

This document will cover the CSA port connection to the 82547GI GbE controller. For CLK66 routing guidelines to the MCH and the GbE controller, please refer to [Section 4.2](#).

If the CSA port is not used, leave all the CSA interface signals disconnected on the MCH except CIVREF, CISWING, and CIRCOMP. See [Section 8.2](#) for CIVREF and CISWING and [Section 8.3](#) for CIRCOMP details.

## 8.1 CSA Port Routing Guidelines

**Caution:** All signals in this section are assumed to be routed microstrip. If you choose to route on inner layers, you must perform thorough signal integrity and timing simulations on each design.

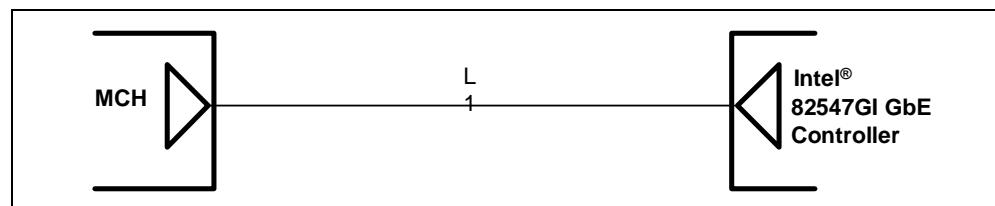
These guidelines should be followed when CSA interface is routed to the 82547GI GbE controller.

The CSA Port signal groups are listed in [Table 57](#).

**Table 57. CSA Port Signal Groups**

Group	Signals	
	MCH	82547GI GbE Controller
Common Clock Signals	CI[10:8]	CI[10:8]
Source Synchronous Signals	CIA[7:0], CISTBF, CISTBS	CIA[7:0], CISTBF, CISTBS
Miscellaneous Signals	CIRCOMP, CISWING, CIVREF	CIRCOMP, CISWING, CIVREF

**Figure 69. CSA Port Signal Routing Topology**



**Table 58. CSA Port Routing Parameters**

Parameters	Routing Guidelines	Notes
Group	CSA Port	
Topology	Point-to-Point	
Reference Plane	Ground referenced (contiguous over entire length)	
Characteristic Trace Impedance ( $Z_0$ )	$60 \Omega \pm 15\%$	
Trace Width	5 mils	
Trace spacing	15 mils	
L1	2 inches to 10 inches	†
MCH Breakout	5 on 5 for 2 inches	
82547GI GbE Controller Breakout	5 on 5 for 0.3 inch	
Strobe to Strobe Length Matching	$\pm 10$ mils	
Strobes to Data Length Matching	$\pm 50$ mils	

† L1 also includes MCH and the 82547GI GbE controller breakout length.

Using the recommended stack-up, the CSA port data signal traces must be routed 5 mils wide. There must be 15 mils spacing between traces (5/15). To break out of the MCH, the CSA port data signals may be routed 5/5 for a distance of up to two inches only. To break out of the 82547GI GbE controller, the CSA port data signals may be routed 5/5 for a distance of up to 0.3 inches only. Again, all CSA port signals should be continuously referenced to GND.

The strobes, CI STBF and CISTBS should be routed next to each other to reduce the coupling on the strobes. Also, each strobe signal trace must be length matched to  $\pm 10$  mils, and each data signal trace must be matched within  $\pm 50$  mils of the strobes.

## 8.2 CSA Port Generation/Distribution of Reference Voltages

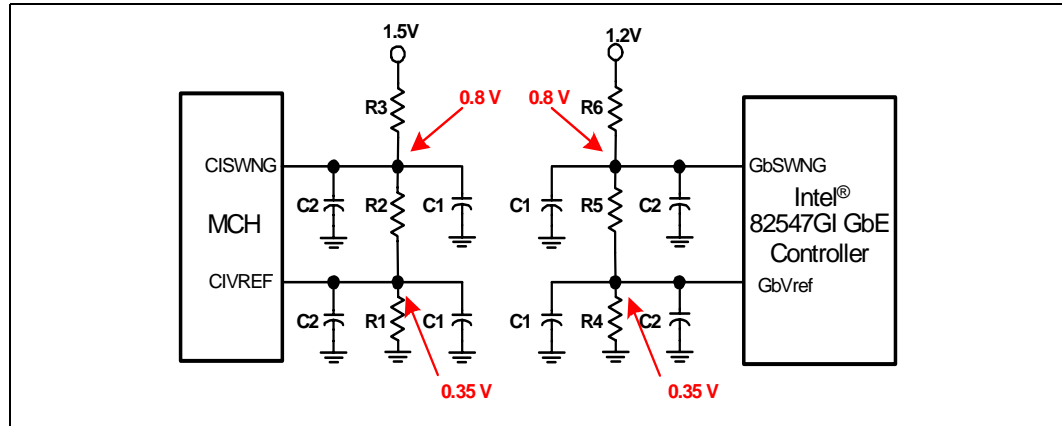
The 11-bit CSA port on the MCH has a dedicated CIVREF pin to sample this reference voltage. The nominal CSA port reference voltage is  $0.35 \text{ V} \pm 3\%$ . In addition to the reference voltage, a reference swing voltage, CISWING must be supplied to control buffer voltage swing characteristics. The nominal CSA port reference voltage swing must be  $0.8 \text{ V} \pm 3\%$ . The 82547GI GbE controller also has a dedicated VREF and SWING pins. The reference voltage is  $0.35 \text{ V} \pm 3\%$  and the swing voltage must be  $0.8 \text{ V} \pm 3\%$ .

**Table 59. CSA Port Reference Circuit Specifications**

Reference Voltage Specification (V)	Reference Swing Voltage Specification (V)	1.5 V Voltage Divider Circuit Recommended Resistor Values ( $\Omega$ )	1.2 V Voltage Divider Circuit Recommended Resistor Values ( $\Omega$ )
$0.350 \text{ V} \pm 3\%$	For MCH and 82547GI GbE controller = $0.8 \text{ V} \pm 3\%$	R1 = $226 \pm 1\%$ R2 = $147 \pm 1\%$ R3 = $113 \pm 1\%$	R4 = $523 \pm 1\%$ R5 = $665 \pm 1\%$ R6 = $604 \pm 1\%$



**Figure 70. CSA Port Locally Generated Reference Divider Circuits**



The values of R1, R2, R3, R4, and R5 must be rated at  $\pm 1\%$  tolerance. The selected resistor values must also ensure that the reference voltage and reference swing voltage tolerance are maintained over the input leakage specification. A  $0.1\ \mu\text{F}$  capacitor (C1 in Figure 70) should be placed within 0.5 inch of each resistor divider, and a  $0.01\ \mu\text{F}$  bypass capacitor (C2 in Figure 70) should be placed within 0.25 inch of reference voltage pins. If the length of the trace from the voltage divider to the pin is greater than one inch, place more than one  $0.01\ \mu\text{F}$  capacitor near the reference voltage pin. The trace length from the voltage divider circuit to the CIREF and GBREF pins must be no longer than 3.5 inches.

Both the voltage reference and voltage swing reference signals should be routed at least 10 mils wide and spaced at least 20 mils from all other signals.

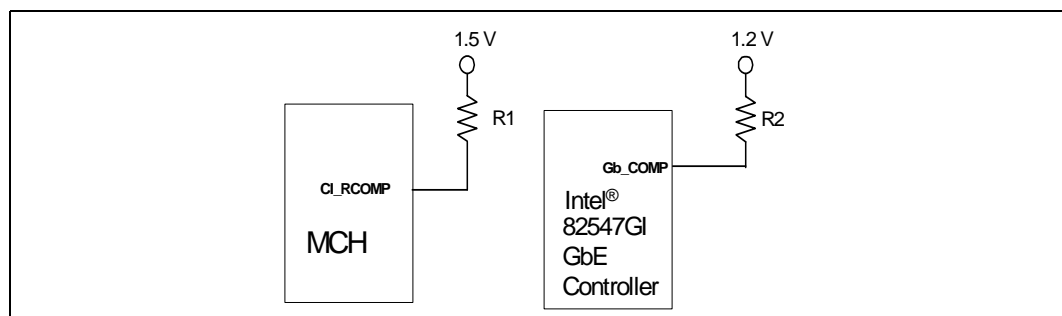
## 8.3 CSA Port Resistive Compensation

The CSA port uses a resistive compensation signal (RCOMP) to compensate buffer characteristics for temperature, voltage, and process.

**Table 60. CSA Port RCOMP Resistor Values**

Component	Trace Impedance	RCOMP Resistor Value	RCOMP Resistor Tied To
MCH	$60\ \Omega \pm 15\%$	$R1 = 52.3\ \Omega \pm 1\%$	VCC1.5
82547GI GbE Controller	$60\ \Omega \pm 15\%$	$R2 = 30.0\ \Omega \pm 1\%$	VCC1.2

**Figure 71. CSA Port RCOMP Circuits**



# Intel® 6300ESB ICH Layout/Routing Guidelines

## 9

This section documents motherboard layout and routing guidelines for 6300ESB ICH-based systems. This section does not discuss the functional aspects of any bus, or the layout guidelines for an add-in device.

**Caution:** When the guidelines listed in this document are not followed, it is very important that thorough signal integrity and timing simulations are completed for each design.

Even when the guidelines are followed, critical signals should still be simulated to ensure proper signal integrity and flight time. As bus speeds increase, it is imperative that the guidelines documented are followed precisely.

## 9.1 General Recommendations

The trace impedance typically noted ( $60\ \Omega \pm 15\%$ ) is the nominal trace impedance. That is, the impedance of the trace when not subjected to the fields created by changing current in neighboring traces. When calculating flight times, it is important to consider the minimum and maximum impedance of a trace based on the switching of neighboring traces. Using wider spaces between the traces may minimize this trace-to-trace coupling. In addition, these wider spaces reduce crosstalk and settling time.

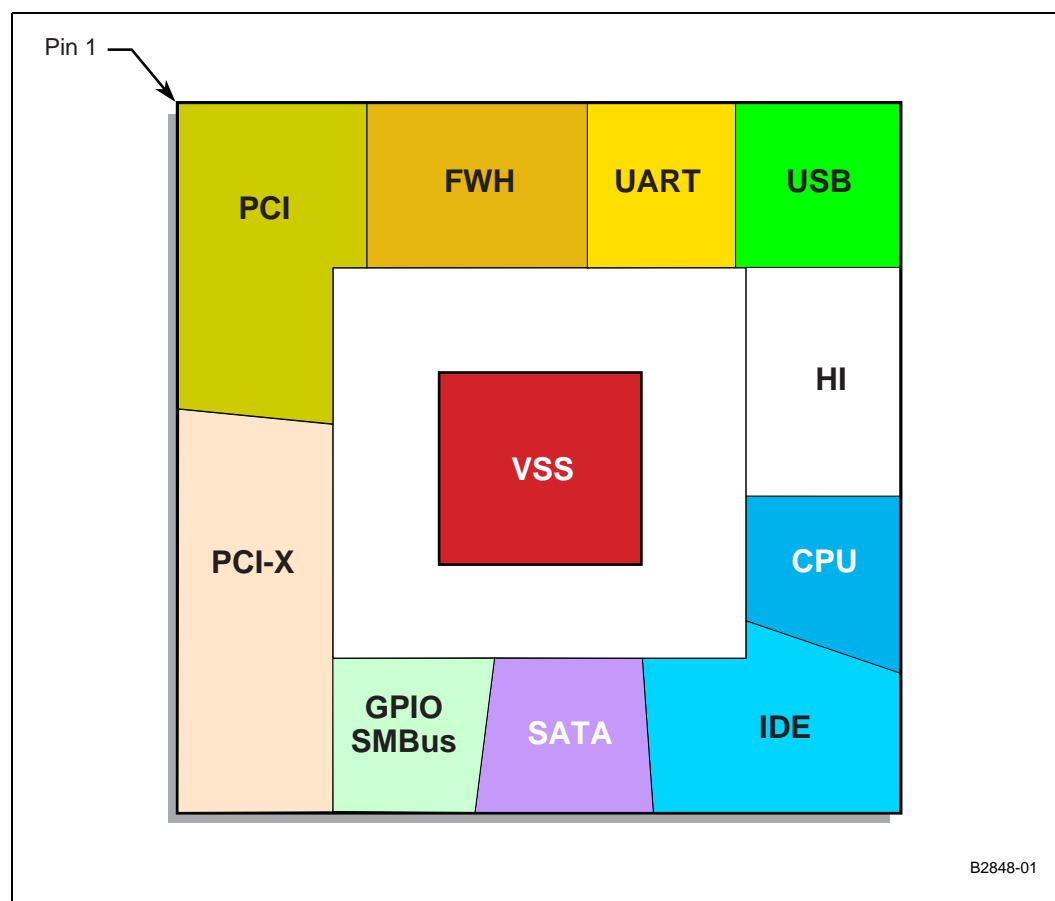
Coupling between two traces is a function of the coupled length, the distance separating the traces, the signal edge rate, and the degree of mutual capacitance and inductance. In order to minimize the effects of trace-to-trace coupling, follow the routing guidelines documented in this section. In addition, the PCB should be fabricated as documented in [Section 3.2, “Board Stack-Up” on page 34](#). If this stack-up is not used, thorough simulations of all interfaces must be completed. Using a thicker dielectric (prepreg) makes routing very difficult or impossible.

**Note:** All spacing is referenced from edge to edge.

## 9.2 Component Quadrant Layout

The quadrant layouts shown are approximate and the exact ball assignments should be used to conduct routing analysis. These quadrant layouts are designed for use during component placement.

**Figure 72. Intel® 6300ESB ICH Quadrant Layout (Top View)**

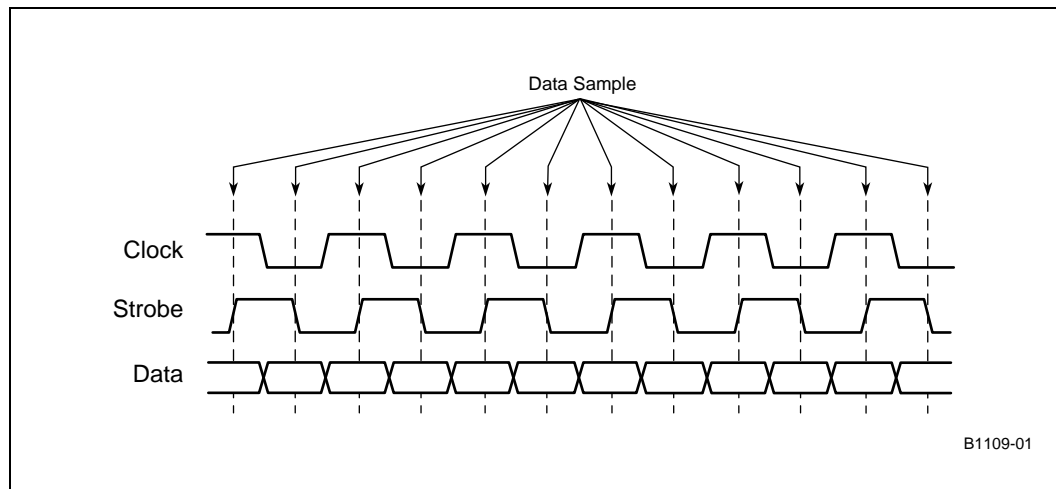


## 9.3 Source Synchronous Strobing

Source synchronous strobing is one of the technologies used in the Hub Interface that allows very high data transfer rates. As buses get faster, and cycle times get shorter, the propagation delay is becoming a limiting factor in bus speed. The use of source synchronous strobing minimizes the impact of propagation delay ( $T_{prop}$ ) on maximum bus frequency.

A source synchronous interface uses strobe signals instead of the clock to indicate data is valid. Refer to [Figure 73](#) for an example.

**Figure 73. Data Strobing Example**



For a source synchronous strobed interface, it is very important that the strobe signals are routed carefully. These signals must be free of noise. Data signals are typically latched on the rising edge, falling edge, or both edges of the strobe signal. Noise on these signals may cause incorrect data to be latched. Refer to [Figure 74](#) and [Figure 75](#).

Figure 74. Correct Strobing Example (No Noise)

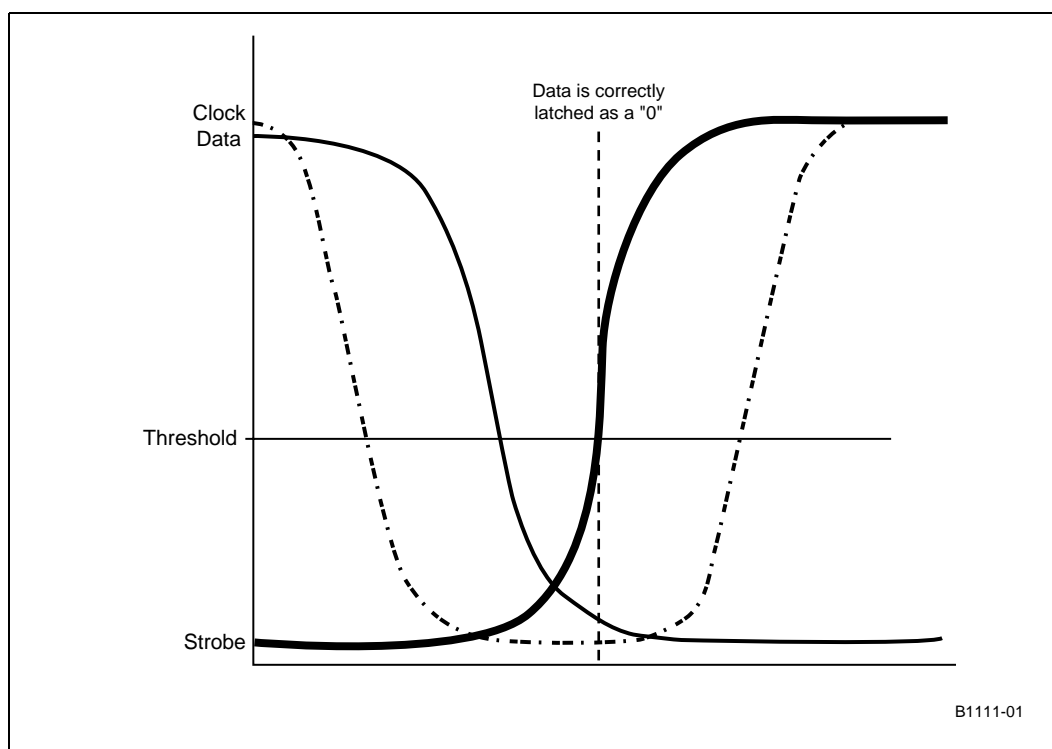
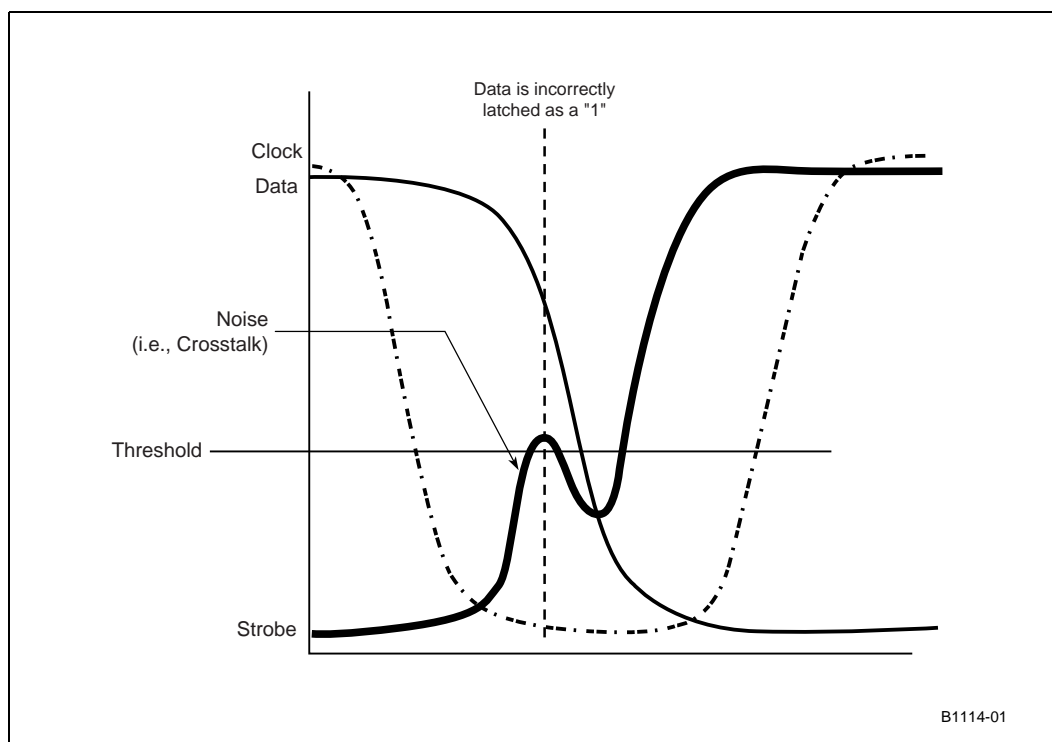


Figure 75. Effect of Crosstalk on Strobe Signal



When routing strobes and their associated data lines, trace length matching is very important, in addition to noise immunity. A benefit of source synchronous strobing is that the data and the strobe arrive at the receiver simultaneously. Thus, a strobe and its associated data signals have very critical length matching requirements. With accurately matched trace lengths and impedance, the propagation delay for the strobe, and the data will be similar. As a result, the strobe and the data arrive at the receiver simultaneously. For some interfaces, the trace length mismatch requirement is to be less than 0.25 inches.

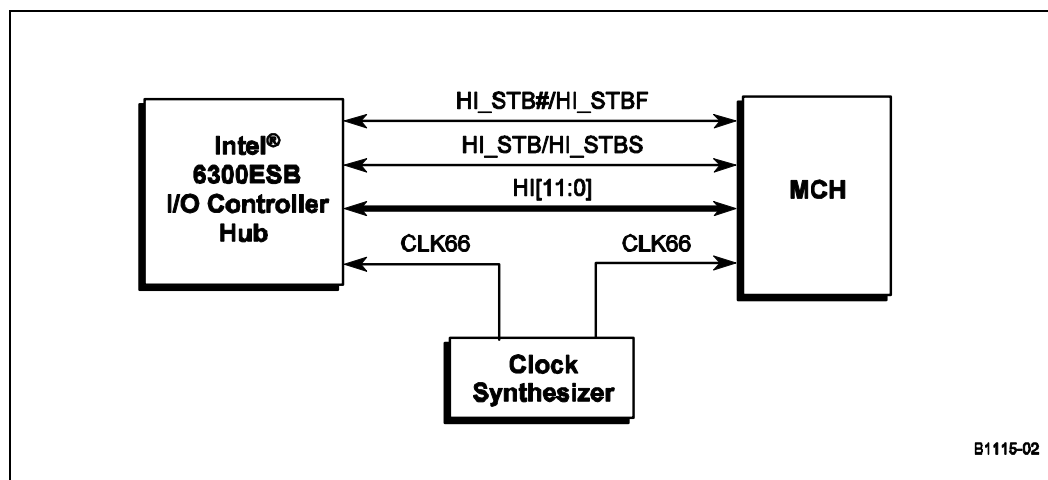
## 9.4 Hub Interface

The MCH and 6300ESB ICH ballout assignments have been optimized to simplify the Hub Interface routing between these devices. It is recommended that the Hub Interface signals be routed directly from the MCH to the 6300ESB ICH with all signals referenced to  $V_{SS}$ . Layer transition should be kept to a minimum. When a layer change is required, use only two vias per net and keep all data signals and associated strobe signal on the same layer.

The Hub Interface signals are broken into two groups: data signals (HI) and strobe signals (HI\_STB). For the 8-bit Hub Interface, HI[11:0] are associated with HI\_STB/HI\_STBS and HI\_STB#/HI\_STBF.

**Note:** These routing guidelines are created using the stack-up described in [Section 3.2, “Board Stack-Up”](#) on page 34.

**Figure 76. 8-Bit Hub Interface Routing Example**



## 9.4.1 8-Bit Hub Interface Routing Guidelines

**Note:** The following guidelines apply to platforms with nominal impedances of  $60\ \Omega \pm 15\%$ .

### 9.4.1.1 8-Bit Hub Interface Data Signals

The 8-bit Hub Interface data signal traces (HI[11:0]) should be routed through stripline or microstrip routing with 5 mil width and 15 mil spacing. (See Table 61.) These signals may be routed 5 mil width and 5 mil spacing for navigation around components, mounting holes or in order to break out of the MCH and the 6300ESB ICH package. The signals must be separated no longer than 300 mils from the package.

**Table 61. Hub Interface 1.5 Data Signals Routing Summary**

Digital Signal Requirement	Maximum Trace Length	Referencing	Data Signal Length Matching
5 mil width, 15 mil spacing	8 inches	Ground	Each strobe signal must be the same length, and each data signal must be matched within $\pm 0.25$ inches of the strobe signals.

### 9.4.1.2 8-Bit Hub Interface Signal Referencing

The 8-bit Hub Interface data signal traces (HI[11:0]) and the two Hub Interface strobe signals (HI\_STB/HI\_STBS and HI\_STB#/HI\_STBF) must all be referenced to ground to ensure proper noise immunity.

### 9.4.1.3 8-Bit Hub Interface Strobe Signals

The Hub Interface strobe signals should be routed 5 mil width, 15 mil spacing. (See Table 62.) This strobe pair should have a minimum of 20 mils spacing from any adjacent signals.

**Table 62. Hub Interface 1.5 Strobe Signals Routing Summary**

Strobe Signal Requirements	Maximum Trace Length	Referencing	Strobe Signal Length Matching
5 mil width, 20 mil spacing (from other signals), 15 mil spacing (intra-pair)	8 inches	Ground	Each strobe signal must be the same length, and each data signal must be matched within $\pm 0.25$ inches of the strobe signal.

### 9.4.1.4 8-bit Hub Interface HIREF and HI\_VSWING Generation/Distribution

HIREF is the Hub Interface reference voltage. The 6300ESB ICH uses HI\_VSWING to control voltage swing and impedance strength of the Hub Interface buffers. The HIREF and HI\_VSWING voltage requirement and associated resistor recommendations for the voltage divider circuit are listed in Table 63. Four options are given for the divider circuit; choose the one that best supports your platform.

**Table 63. 8-Bit Hub Interface HIREF/HI\_VSWING Generation Circuit Specifications**

HIREF Voltage Specification (V)	HI_VSWING Voltage Specification (V)	Recommended Values for the HIREF / HI_VSWING Divider Circuit ( $\Omega$ )
350 mV $\pm$ 2%	800 mV $\pm$ 2%	Option A (Figure 77 and Figure 78) <ul style="list-style-type: none"> <li>• R1 = 226 <math>\Omega \pm</math> 1%</li> <li>• R2 = 147 <math>\Omega \pm</math> 1%,</li> <li>• R3 = 113 <math>\Omega \pm</math> 1%</li> </ul> Option B (Figure 77 and Figure 78) <ul style="list-style-type: none"> <li>• R1 = 80.6 <math>\Omega \pm</math> 1%</li> <li>• R2 = 51.1 <math>\Omega \pm</math> 1%</li> <li>• R3 = 40.2 <math>\Omega \pm</math> 1%</li> </ul> Option C (Figure 77 and Figure 78) <ul style="list-style-type: none"> <li>• R1 = 255 <math>\Omega \pm</math> 1%</li> <li>• R2 = 162 <math>\Omega \pm</math> 1%</li> <li>• R3 = 127 <math>\Omega \pm</math> 1%</li> </ul> Option D (Figure 79 and Figure 80) <ul style="list-style-type: none"> <li>• R4 = 78.7 <math>\Omega \pm</math> 1%</li> <li>• R5 = 24.2 <math>\Omega \pm</math> 1%</li> <li>• R6 = 43.2 <math>\Omega \pm</math> 1%</li> <li>• R7 = 49.9 <math>\Omega \pm</math> 1%</li> </ul>

**NOTES:**Capacitance Values For All Options

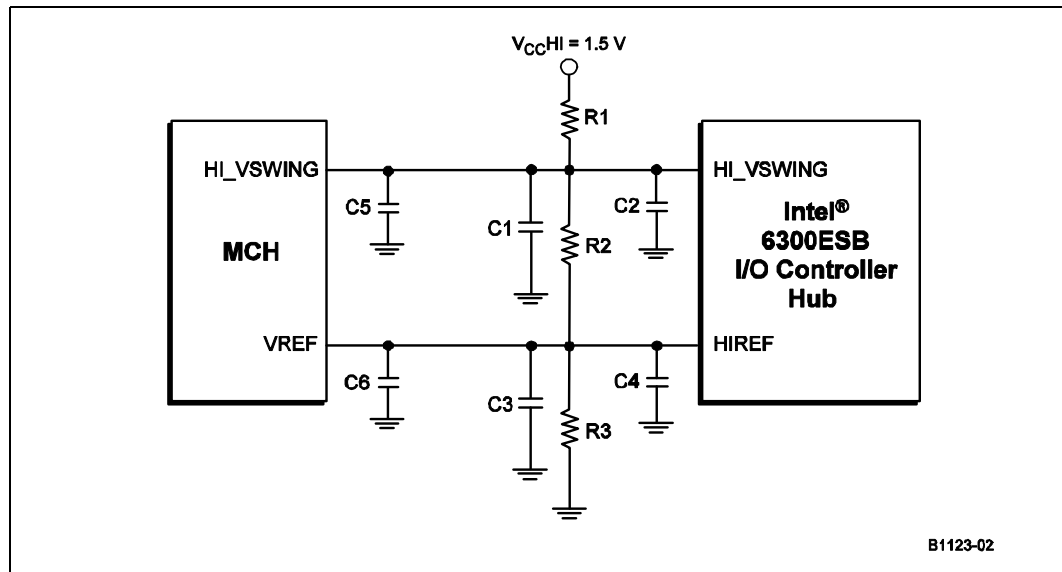
1. C1 and C3 = 0.1  $\mu$ F (near divider)
2. C2, C4, C5, C6 = 0.01  $\mu$ F (near MCH and 6300ESB ICH)
3. The resistor values R1, R2, R3, R4, R5, R6, and R7 must be rated at 1% tolerance.

**Note:** HIREF and HI\_VSWING is derived from 1.5 V which is the nominal core voltage for the 6300ESB ICH. Voltage supply tolerance for driver voltage must be within a  $\pm$  5% range of nominal.

The selected resistor values ensure that the reference voltage tolerance is maintained over the input leakage specification. The maximum distance from divider to device is four inches (less is better). Normal care needs to be taken to minimize crosstalk to other signals (<10–15 mV). When the single HIREF/HI\_VSWING divider circuit is located more than four inches away, then the locally generated reference divider should be used. Figure 77, Figure 78, Figure 79, and Figure 80 are examples of the HIREF/HI\_VSWING divider circuit.



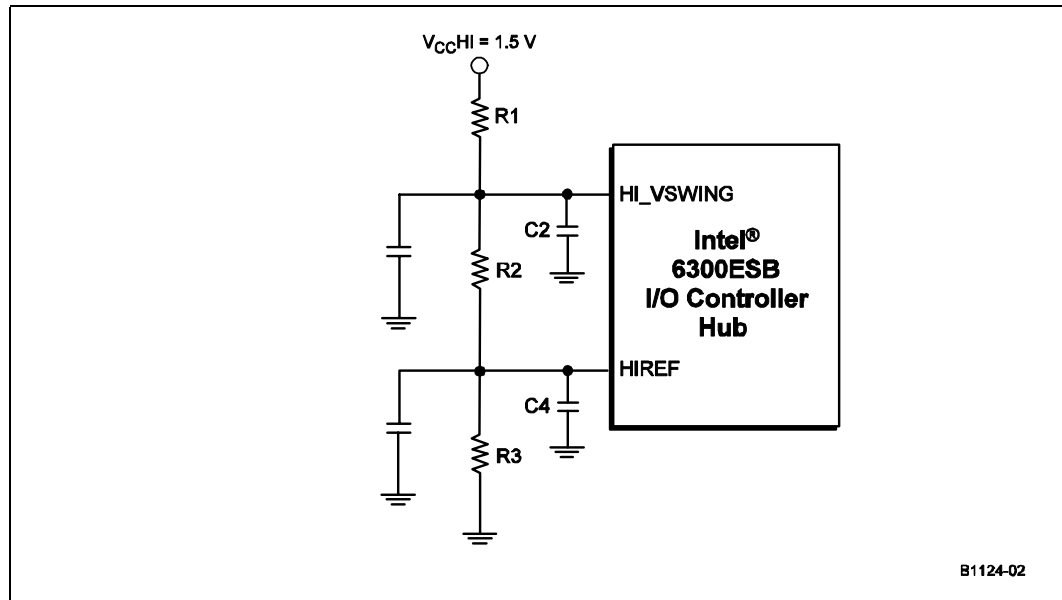
**Figure 77. 8-Bit Hub Interface Single HIREF/HI\_VSWING Generation Circuit Option A**



**NOTES:**

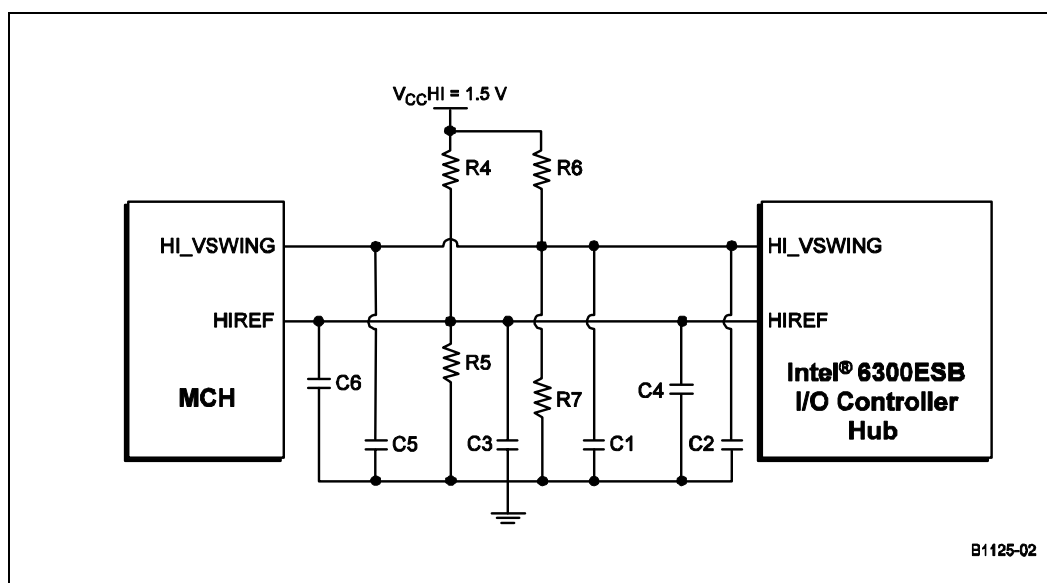
1. Two 0.1  $\mu$ F capacitors (C1 and C3) should be placed close to the divider.
2. Each 0.01  $\mu$ F bypass capacitor (C2, C4, C5, and C6) should be placed within 0.25 inches of HIREF/VREF pin (for C4 and C6) and HI\_VSWING pin (for C2 and C5).

**Figure 78. 8-Bit Hub Interface Local HIREF/HI\_VSWING Generation Circuit Option B**



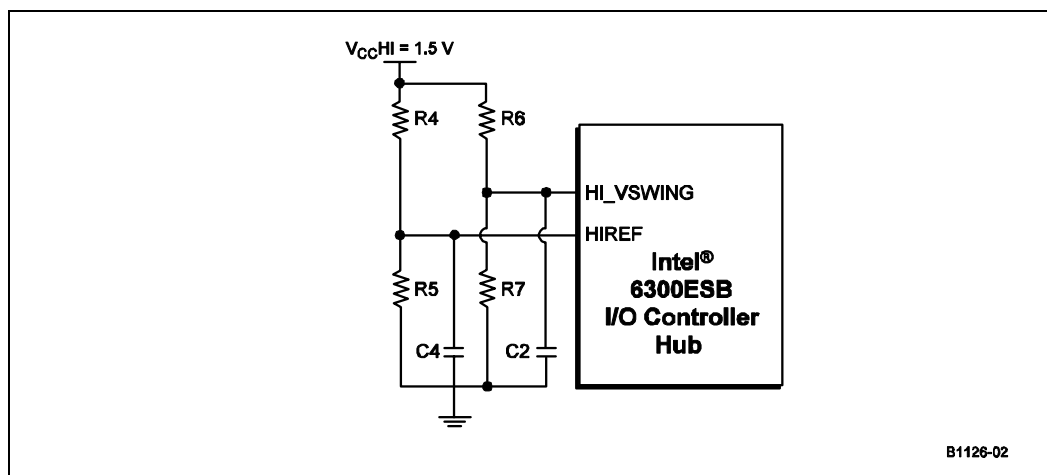
**NOTE:** Each 0.01  $\mu$ F bypass capacitor should be placed within 0.25 inches of HIREF/VREF pin (C4) and HI\_VSWING pin (C2).

Figure 79. 8-Bit Hub Interface Single HIREF/Hi\_VSWING Generation Circuit Option C

**NOTES:**

1. Two 0.1  $\mu\text{F}$  capacitors (C1 and C3) should be placed close to the divider.
2. Each 0.01  $\mu\text{F}$  bypass capacitor (C2, C4, C5, and C6) should be placed within 0.25 inches of HIREF/VREF pin (for C4 and C6) and HI\_VSWING pin (for C2 and C5)

Figure 80. 8-Bit Hub Interface Local HIREF/Hi\_VSWING Generation Circuit Option D



**NOTE:** Each 0.01  $\mu\text{F}$  bypass capacitor should be placed within 0.25 inches of HIREF/VREF pin (C4) and HI\_VSWING pin (C2).

### 9.4.1.5 8-Bit Hub Interface Compensation

The Hub Interface uses a compensation signal to adjust buffer characteristics to the specific board characteristic. The Hub Interface requires resistive compensation (HICOMP). (See Table 64.)

**Table 64. 8-Bit Hub Interface HICOMP Resistor Values**

Trace Impedance	HICOMP Calculation	HICOMP Resistor Value	HICOMP Resistor Tied to
60 $\Omega \pm 15\%$	$[(1.5-0.8)/(0.8)]*60$	52.3 $\Omega \pm 1\%$	V <sub>CC</sub> HI=1.5 V
55 $\Omega \pm 10\%$	$[(1.5-0.8)/(0.8)]*55$	48.1 $\Omega \pm 1\%$	V <sub>CC</sub> HI=1.5 V
50 $\Omega \pm 10\%$	$[(1.5-0.8)/(0.8)]*50$	43.2 $\Omega \pm 1\%$	V <sub>CC</sub> HI=1.5 V

### 9.4.1.6 8-Bit Hub Interface Decoupling Guidelines

To improve I/O power delivery, use two 0.1  $\mu$ F capacitors for each component (i.e., the 6300ESB ICH and MCH). These capacitors should be placed within 50 mils from each package, adjacent to the rows that contain the Hub Interface. When the layout allows, wide metal fingers running on the V<sub>SS</sub> side of the board should connect the V<sub>CC</sub>HI=1.5 V side of the capacitors to the V<sub>CC</sub>HI=1.5 V power pins. Similarly, when the layout allows, metal fingers running on the V<sub>CC</sub>HI=1.5 V side of the board should connect the ground side of the capacitors to the V<sub>SS</sub> power pins.

### 9.4.1.7 Terminating HI\_11 If Not Used

If HI\_11 is not used it should be terminated to V<sub>SS</sub> through: ~50  $\Omega$ /55  $\Omega$ /60  $\Omega$  depending on board trace impedance.

**Table 65. HI\_11 Termination Resistor Values**

Trace Impedance	Termination Resistor Value	HI_11 Termination Resistor Tied to
60 $\Omega \pm 15\%$	56 $\Omega$ or 62 $\Omega \pm 5\%$	V <sub>SS</sub>
55 $\Omega \pm 10\%$	51 $\Omega$ or 56 $\Omega \pm 5\%$	V <sub>SS</sub>
50 $\Omega \pm 10\%$	47 $\Omega$ or 51 $\Omega \pm 5\%$	V <sub>SS</sub>

## 9.5 Serial ATA Interface

### 9.5.1 Layout Guidelines

**Note:** These routing guidelines are created using the stack-ups described in [Section 3.2, “Board Stack-Up”](#) on page 34.

#### 9.5.1.1 General Routing and Placement

Use the following general routing and placement guidelines when laying out a new design.

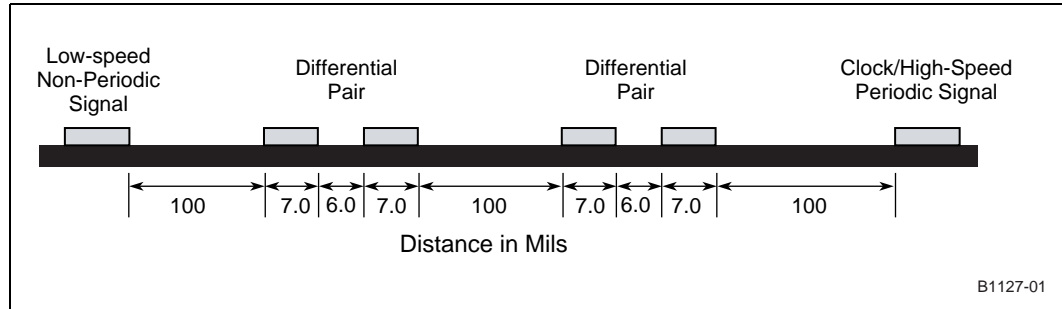
1. Serial ATA (SATA) signals must have *consistent plane referencing* maintained for the entire path between driver and receiver. Signals routed on microstrip may be referenced to either power or ground but not both. Stripline signals should be surrounded by power planes (Vcc or GND) and shall be maintained consistent along the entire transmission path.
2. Route all traces using microstrip over continuous planes (Vcc or GND), with no interruptions. Avoid crossing over anti-etch if at all possible. Any discontinuity or split in the ground plane may cause signal reflections and should be avoided.
3. No layer changes or vias other than the package ball shall be allowed.
4. Do not route SATA traces around or under crystals, oscillators, clock synthesizers, magnetic devices or ICs that use and/or duplicate clocks.
5. No 90 degree bends or stubs.
6. The allowable breakout region is 500 mils from the package.
7. Do not route SATA traces through connectors or any other obstruction that would require a deviation in the intra-pair spacing and thus, differential impedance. The exception is the breakout region from the pin whose length should be minimized to reduce reflections.

#### 9.5.1.2 Serial ATA Trace Separation

Use the following separation guidelines. [Figure 81](#) provides an illustration of the recommended trace spacing.

1. Maintain parallelism and consistent trace spacing between SATA differential signals with the trace spacing needed to achieve  $79.3 \Omega \pm 15\%$  differential impedance. Deviations will normally occur due to package breakout and routing to connector pins. Ensure that the amount and length of the deviations are kept to the minimum possible.
2. Use an impedance calculator to determine the trace width and spacing required for the specific board stackup being used, keeping in mind that the target is a  $79.3 \Omega \pm 15\%$  differential impedance. For the board stackup parameters referred to in [Section 3.2, “Board Stack-Up”](#) on page 34, 7.0 mil traces with 6.0 mil spacing results in approximately  $79.3 \Omega \pm 15\%$  differential trace impedance.
3. Based on simulation data, use 100 mil minimum spacing between 6300ESB ICH SATA signal pairs and other signal traces for optimal signal quality. This helps to reduce crosstalk.

**Figure 81. Serial ATA Trace Spacing Recommendation**



### 9.5.1.3 Serial ATA Trace Length Pair Matching

SATA signal pair traces should be trace length matched. The difference of two line traces in a differential pair should be restricted to below 10 mils.

### 9.5.1.4 Serial ATA Trace Length Guidelines

The length of the differential pairs (i.e., Tx pair and Rx pair) should be designed to within the recommend values. The recommended length of the trace is from two to eight inches. When the trace length of the differential pair is longer than recommended, the high-frequency differential signal suffers significant signal attenuation and an increase in inter-symbol interference.

**Table 66. Serial ATA Routing Summary**

Differential Trace Impedance	SATA Routing Requirements	Trace Length	SATA Signal Length Matching
79.3 $\Omega \pm 15\%$	7 mil width, 6 mil spacing (Based on stackup described in <a href="#">Section 3.</a> )	2–8 inches	Length mismatch between signals in a data pair should be no more 10 mils.

### 9.5.1.5 Serial ATA BIAS Connections

It is recommended that the SATARBIASP and the SATARBIASN pins be shorted at the package and routed to one end of a 24.9  $\Omega \pm 1\%$  resistor to ground. Place the resistor within 500 mils of the 6300ESB ICH and avoid routing next to clock pins.

**Figure 82. Serial ATA BIAS Connections**

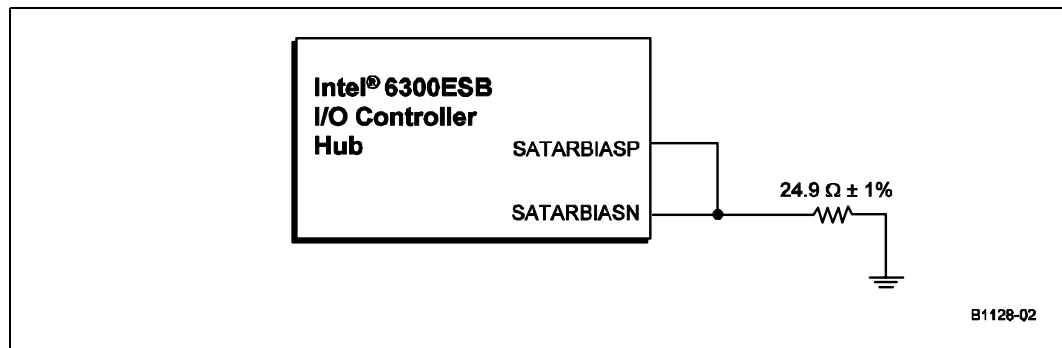


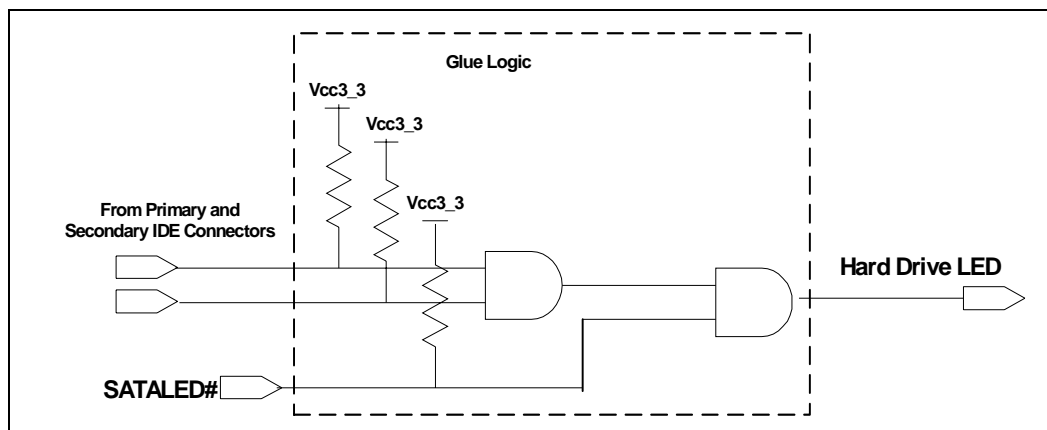
Table 67. Serial ATA BIAS Routing Summary

Trace Impedance	SATARBIASP/SATARBIASN Routing Requirements	Maximum Trace Length
60 $\Omega \pm 15\%$	5 mil width, 5 mil spacing	500 mils

### 9.5.1.6 SATALED# Implementation

The 6300ESB ICH provides a signal (SATALED#) to indicate SATA device activity. In order for this signal to work in conjunction with Parallel ATA hard drives, Intel recommends implementing the glue logic shown in Figure 83.

Figure 83. SATALED# Circuitry Example



This signal is open-drain and requires a weak external pull-up to  $V_{CC3.3}$ . When low, SATALED# indicates SATA device activity and should activate the hard drive LED. When tri-stated, the signal will not activate the LED.

**Note:** Ensure that all connectors and cables comply with the *SATA Gold Specification, Revision 1.0*, dated August 29, 2001 or later.

## 9.6 IDE Interface

**Note:** These routing guidelines are created using the stack-up described in [Section 3](#) on [page 34](#).

This section contains guidelines for connecting and routing the 6300ESB ICH IDE interface. The 6300ESB ICH has two independent IDE channels. This section provides guidelines for IDE connector cabling and motherboard design, including component and resistor placement, and signal termination for both IDE channels. The 6300ESB ICH has integrated the series resistors that have been typically required on the IDE data signals (PDD[15:0] and SDD[15:0]) running to the two ATA connectors. While it is not anticipated that additional series termination resistors will be required, OEMs should verify motherboard signal integrity through simulation. Additional external 0  $\Omega$  resistors may be incorporated into the design to address possible noise issues on the motherboard. The additional resistor layout increases flexibility by offering stuffing options at a later date. When used, place these resistors close to the connector.

**Table 68. IDE Signal Groups**

Signal Group	Primary	Secondary
Data	PDD[15:0]	SDD[15:0]
Strobes	PDIOR# (write) PDIORDY (read)	SDIOR# (write) SDIORDY (read)

The IDE interface must be routed with 5 mil width traces, 7 mil spacing (dependent upon stackup parameters), and must be less than eight inches long (from the 6300ESB ICH to the IDE connector). See [Table 69](#) below for routing summary.

**Note:** A maximum of two layer transitions are allowed. All transitions must be routed within 1.5 inches of the 6300ESB ICH pin. After the 1.5 inch layer transition boundary, all strobe and data signals must be routed on the same layer. No layer transitions are allowed at the IDE connector.

**Table 69. IDE Routing Summary**

Trace Impedance	IDE Routing Requirements	Maximum Trace Length	IDE Signal Length Matching
60 $\Omega \pm 15\%$	5 mil width, 7 mil spacing (based on stackup assumptions in <a href="#">Section 8.1</a> )	8 inches	The two strobe signals must be matched within 100 mils of each other. The data lines must be within $\pm 500$ mils of the average length of the two strobe signals.

### 9.6.1 Cabling

**Length of cable:** Each IDE cable must be equal to 18 inches.

**Capacitance:** Less than 35 pF.

**Placement:** A maximum of six inches between drive connectors on the cable. When a single drive is placed on the cable, it should be placed at the end of the cable. When a second drive is placed on the same cable, it should be placed on the next closest connector to the end of the cable (six inches away from the end of the cable).

**Grounding:** Provide a direct low impedance chassis path between the motherboard ground and hard disk drives.

## 9.7 Cable Detection for Ultra ATA/66 and Ultra ATA/100

The 6300ESB ICH IDE Controller supports PIO, Multi-word (8237 style) DMA, and Ultra DMA modes 0 through 5, and Native Mode IDE. Please note that there are no motherboard hardware requirements for supporting Native Mode IDE. Native Mode IDE is supported through the operating system and system drivers. The 6300ESB ICH needs to determine the type of cable that is present, in order to configure itself for the fastest possible transfer mode that the hardware may support.

An 80-conductor IDE cable is required for Ultra DMA modes greater than two (Ultra ATA/33). This cable uses the same 40-pin connector as the old 40-pin IDE cable. The wires in the cable alternate: ground, signal, ground, signal, ground, signal, ground. All the ground wires are tied together on the cable (and they are tied to the ground on the motherboard through the ground pins in the 40-pin connector). This cable conforms to the *Small Form Factor Specification SFF-8049*. This specification may be obtained from the Small Form Factor Committee.

To determine when Ultra DMA modes greater than two (Ultra ATA/33) may be enabled, the 6300ESB ICH requires the system software to attempt to determine the cable type used in the system. When the system software detects an 80-conductor cable, it may use any Ultra DMA mode up to the highest transfer mode supported by both the chipset and the IDE device. When a 40-conductor cable is detected, the system software must not enable modes faster than Ultra DMA Mode 2 (Ultra ATA/33).

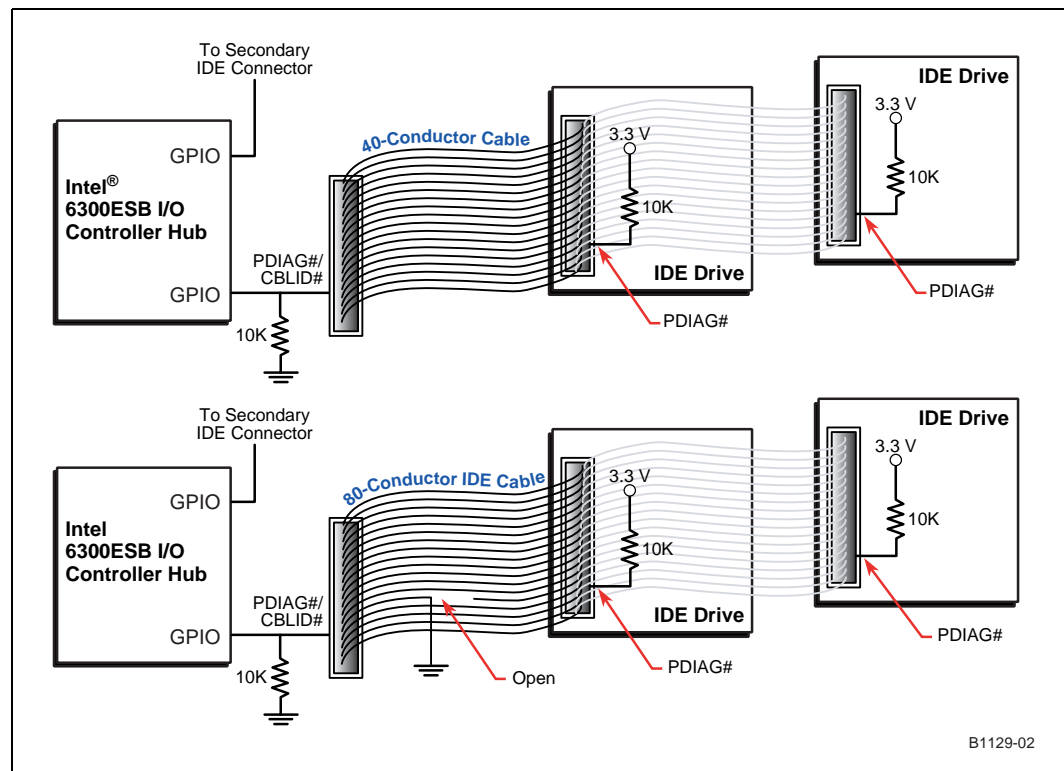
Intel recommends that cable detection be performed using a combination Host-Side/Device-Side detection mechanism. Note that Host-Side detection cannot be implemented on an NLX form factor system, since this configuration does not define interconnect pins for the PDIAG#/CBLID# from the riser (containing the ATA connectors) to the motherboard. These systems must rely on the Device-Side Detection mechanism only.

### 9.7.1 Combination Host-Side/Device-Side Cable Detection

Host-side detection (described in the *ATA/ATAPI-6 Standard*) requires the use of two GPIO pins (one for each IDE channel). The proper way to connect the PDIAG#/CBLID# signal of the IDE connector to the host is shown in [Figure 84](#). All IDE devices have a 10 K $\Omega$  pull-up resistor to 5 V on this signal. A 10 K $\Omega$  pull-down resistor on PDIAG#/CBLID# is required to prevent the GPIO from floating if a device is not present and allows for use of a non-5 V tolerant GPIO.



Figure 84. Combination Host-Side/Device-Side IDE Cable Detection



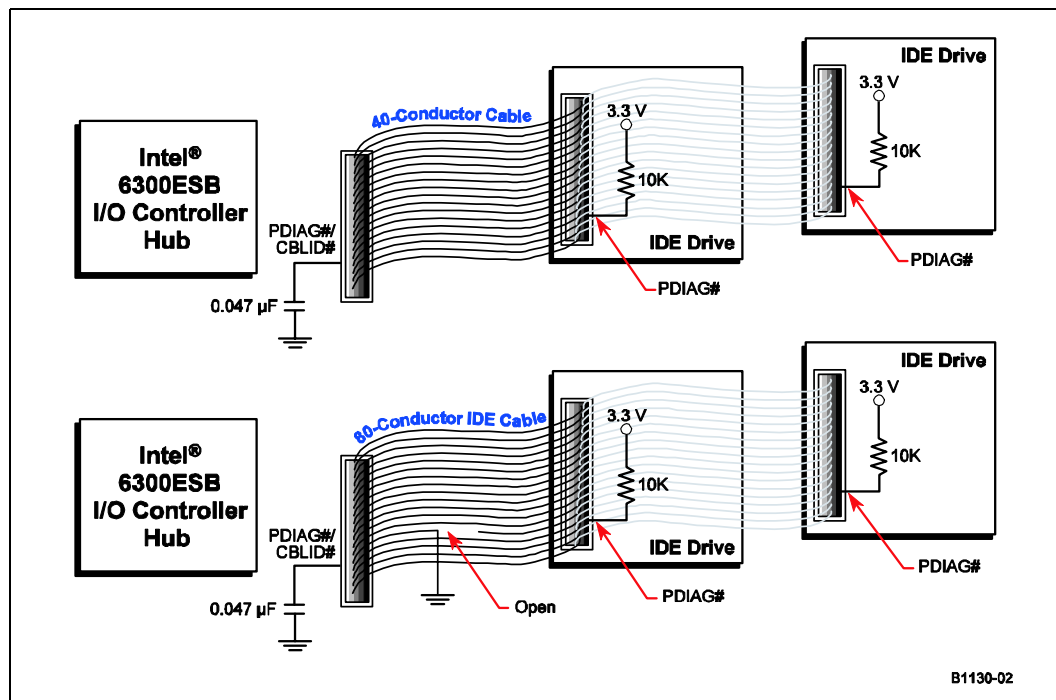
This mechanism allows the BIOS, after diagnostics, to sample PDIAG#/CBLID#. When the signal is high, there is 40-conductor cable in the system and Ultra DMA modes greater than two (Ultra ATA/33) must not be enabled.

When PDIAG#/CBLID# is detected low, there may be an 80-conductor cable in the system, or there may be a 40-conductor cable and a legacy slave device (Device 1) that does not release the PDIAG#/CBLID# signal as required by the *ATA/ATAPI-6 standard*. In this case, BIOS should check the IDENTIFY DEVICE information in a connected device that supports Ultra DMA modes higher than two. When ID Word 93, bit 13 is a one, an 80-conductor cable is present. When this bit is zero, a legacy slave (Device 1) is preventing proper cable detection and BIOS should configure the system as though a 40-conductor cable is present, and notify the user of the problem.

## 9.7.2 Device-Side Cable Detection

For platforms that must implement Device-Side detection only (e.g., NLX platforms), a 0.047  $\mu$ F capacitor is required on the motherboard as shown in Figure 85. This capacitor should not be populated when implementing the recommended combination Host-Side/Device-Side cable detection mechanism described above. Please note some drives may not support device-side cable detection.

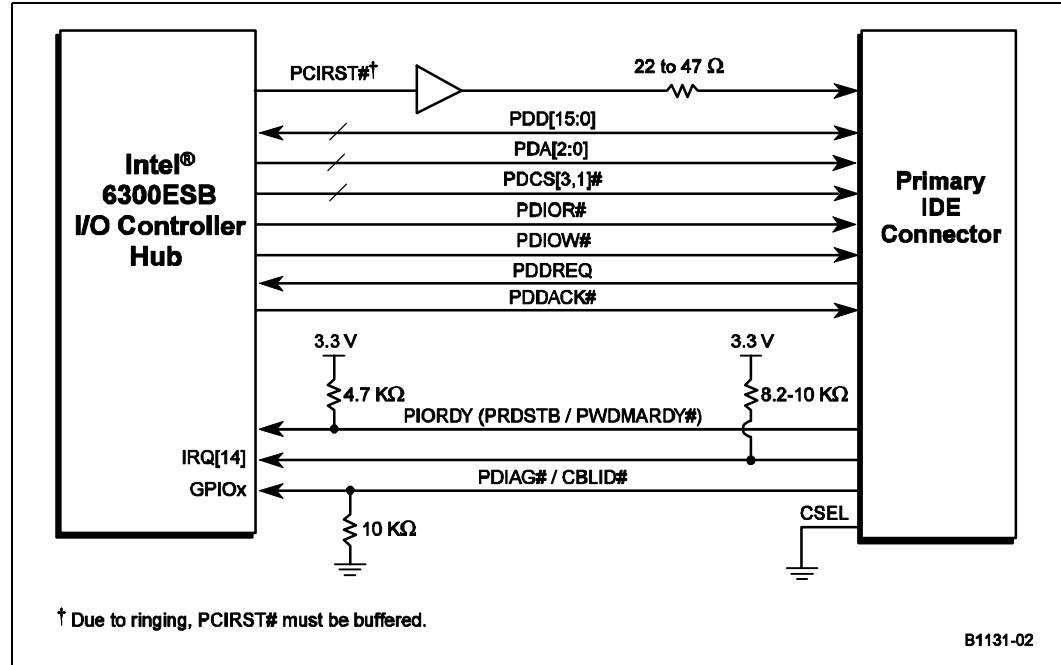
Figure 85. Device Side IDE Cable Detection



This mechanism creates a resistor-capacitor (RC) time constant. Hard drives supporting Ultra DMA modes greater than two (Ultra DMA/33) drive PDIAG#/CBLID# low and then release it (pulled up through a 10 K $\Omega$  resistor). The drive samples the signal after releasing it. In an 80-conductor cable, PDIAG#/CBLID# is not connected through to the host and therefore the capacitor has no effect. In a 40-conductor cable, the signal is connected to the host. Therefore, the signal rises slower as the capacitor charges. The drive may detect the difference in rise times and it reports the cable type to the BIOS when it sends the IDENTIFY\_DEVICE packet during system boot as described in the *ATA/ATAPI-6 Standard*.

### 9.7.3 Primary IDE Connector Requirements

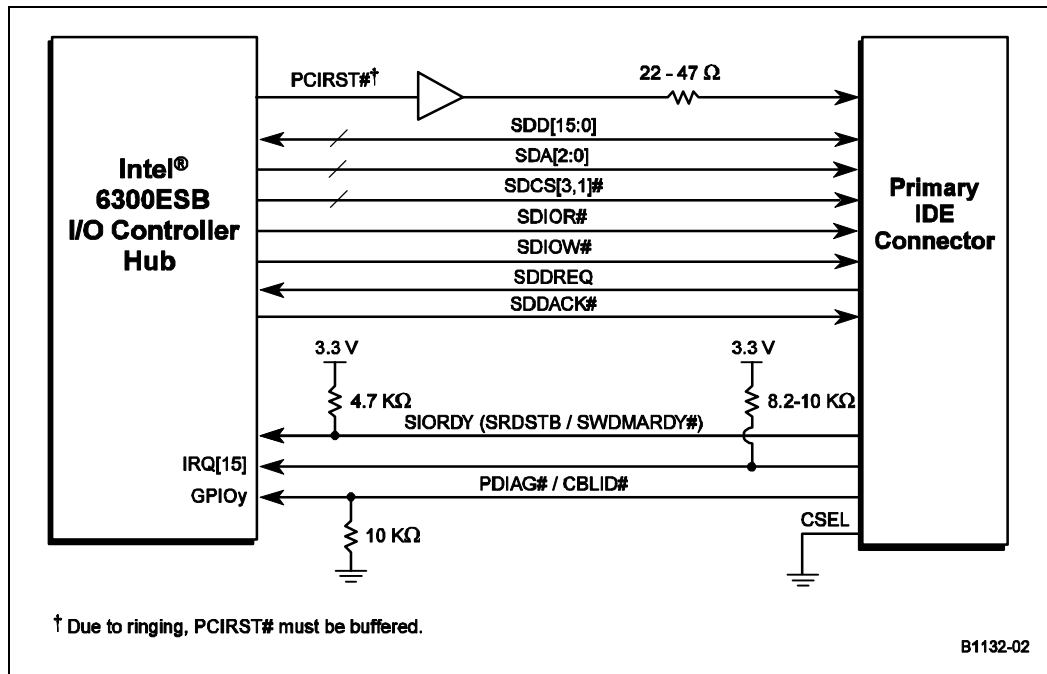
Figure 86. Connection Requirements for Primary IDE Connector



- 22  $\Omega$  - 47  $\Omega$  series resistors are required on PCIRST#. The correct value should be determined for each unique motherboard design, based on signal quality.
- An 8.2K  $\Omega$  to 10K  $\Omega$  pull-up resistor is required on IRQ14 to  $V_{CC}3.3$ .
- A 4.7K  $\Omega$  pull-up resistor to  $V_{CC}3.3$  is required on PIORDY.
- Series resistors are not required but may be placed on the control and data line to improve signal quality. Place the resistors as close to the connector as possible. Resistor values are from 33-47  $\Omega$ .
- The 10K  $\Omega$  resistor to ground on the PDIAG#/CBLID# signal is required on the Primary Connector. This change is to prevent the GPI pin from floating when a device is not present on the IDE interface.
- Place all resistors as close to the IDE connector as possible.

## 9.7.4 Secondary IDE Connector Requirements

Figure 87. Connection Requirements for Secondary IDE Connector



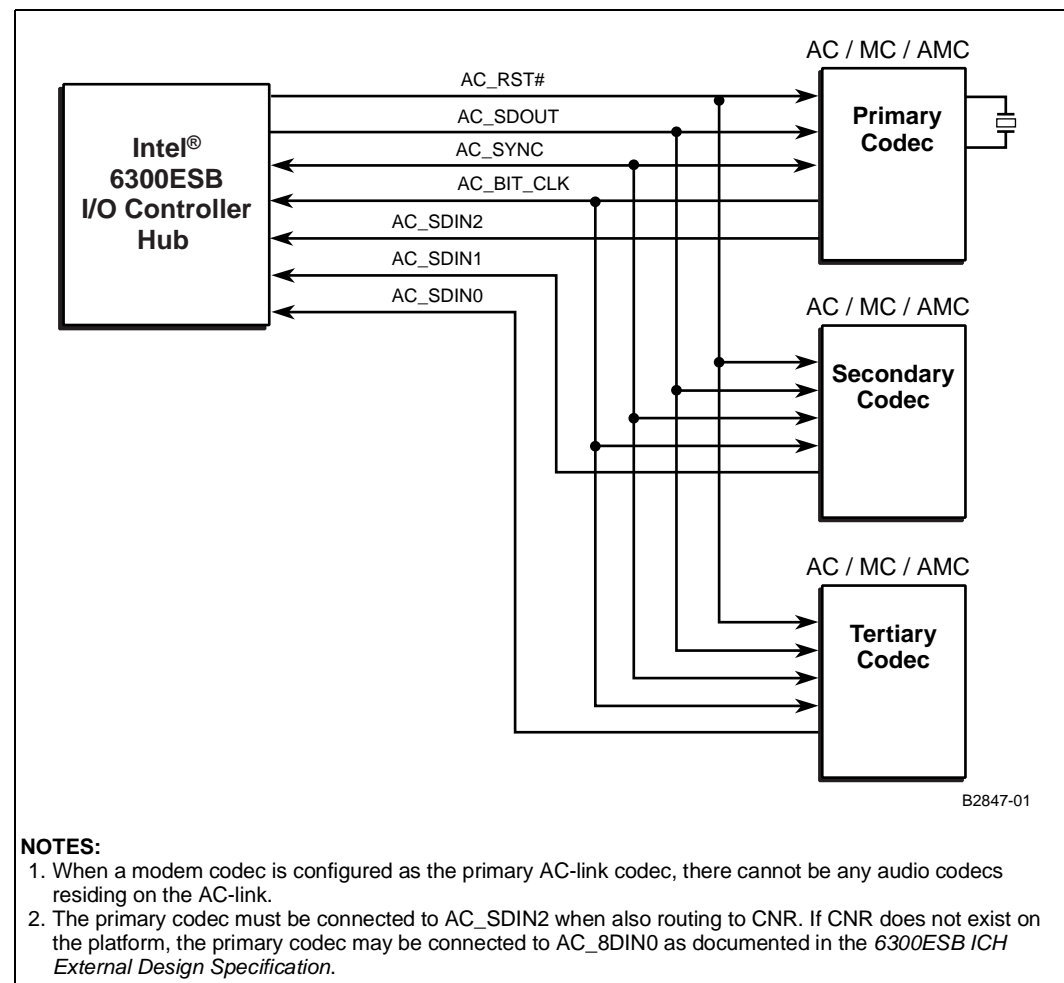
- 22 Ω - 47 Ω series resistors are required on PCIRST#. The correct value should be determined for each unique motherboard design, based on signal quality.
- An 8.2 KΩ to 10 KΩ pull-up resistor is required on IRQ15 to V<sub>CC</sub>3.3.
- A 4.7 KΩ pull-up resistor to V<sub>CC</sub>3.3 is required on SIORDY.
- Series resistors are not required but may be placed on the control and data line to improve signal quality. Place the resistors as close to the connector as possible. Resistor values are from 33 Ω - 47 Ω.
- The 10 KΩ resistor to ground on the PDIAG#/CBLID# signal is required on the Secondary Connector. This change is to prevent the GPI pin from floating when a device is not present on the IDE interface.
- Place all resistors as close to the IDE connector as possible.

## 9.8 AC '97

The 6300ESB ICH implements an AC '97 2.2-compliant digital controller. Please contact your codec IHV (independent hardware vendor) for information on 2.2-compliant products. Refer also to the *AC '97 2.2 Specification*.

The AC-link is a unidirectional, serial PCM digital stream. It handles multiple input and output data streams, as well as control register accesses, employing a time division multiplexed (TDM) scheme. The AC-link architecture provides for data transfer through individual frames transmitted in a serial fashion. Each frame is divided into 12 outgoing and 12 incoming data streams, or slots. The architecture of the 6300ESB ICH AC-link allows a maximum of three codecs to be connected. Figure 88 shows a three-codec topology of the AC-link for the 6300ESB ICH.

**Figure 88. ICH AC'97— Codec Connection**



**Note:** The following routing guidelines are created using the stack-up described in Section 3.2, “Board Stack-Up” on page 34.

Using the assumed six layer stack-up, the AC '97 interface may be routed using 5 mil traces with 10 mil spacing between the traces. Maximum length between the 6300ESB ICH and the CODEC/CNR is 14 inches. This assumes that a CNR riser card implements its audio solution with a maximum trace length of six inches for the AC-link. The CNR and motherboard target trace impedance should be  $Z_0 = 60 \Omega \pm 15\%$  dependant on platform stackup described in [Section 3.2](#), “Board Stack-Up” on page 34.

Clocking is provided from the primary codec on the link via AC\_BIT\_CLK, and is derived from a 24.576 MHz crystal or oscillator. Refer to the primary codec vendor for crystal or oscillator requirements. AC\_BIT\_CLK is a 12.288 MHz clock driven by the primary codec to the digital controller (6300ESB ICH) and to any other codec present. That clock is used as the time base for latching and driving data.

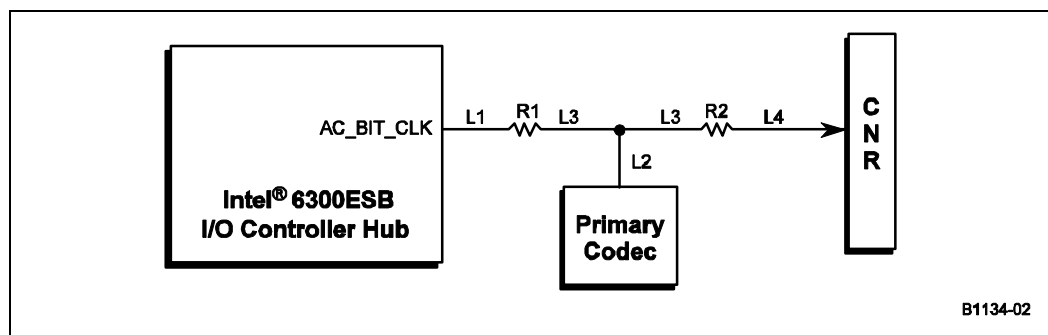
The 6300ESB ICH supports wake on ring from S1-S5 through the AC '97 link. The codec asserts AC\_SDIN to wake the system. To provide wake capability and/or caller ID, standby power must be provided to the modem codec.

The 6300ESB ICH has pull-downs/pull-ups that are always enabled. This will keep the link from floating when the AC-link is off, or when there are no codecs present.

When the Shut-off bit is not set, it implies that there is a codec on the link. Therefore, AC\_BIT\_CLK and AC\_SDOOUT will be driven by the codec and the 6300ESB ICH, respectively. However, AC\_SDIN0, AC\_SDIN1 and AC\_SDIN2 may not be driven. When the link is enabled, the assumption may be made that there is at least one codec.

**Note:** A 15 pF capacitor to Gnd should replace an unpopulated motherboard codec for the CLK and SDATA\_IN lines to reduce reflection and improve signal quality.

**Figure 89. ICH AC'97 – AC\_BIT\_CLK Topology**



**Table 70. AC '97 AC\_BIT\_CLK Routing Summary**

Trace Impedance	AC '97 Routing Requirements	Trace Lengths	Series Termination Resistance	AC_BIT_CLK Signal Length Matching
$60 \Omega \pm 15\%$	5 mil width, 10 mil spacing (based on stackup assumptions in <a href="#">Section 3.2</a> )	L1 = 3 to 8 inches L2 = 0.1 to 0.5 inches L3 = 0.1 to 0.5 inches L4 = 3 to 6 inches	R1 = $34.2 \Omega - 37.8 \Omega$ R2 = R1 (Optional 0 $\Omega$ resistor for debug purposes only).	N/A

Figure 90. ICH AC'97 – AC\_SDOUT/AC\_SYNC Topology

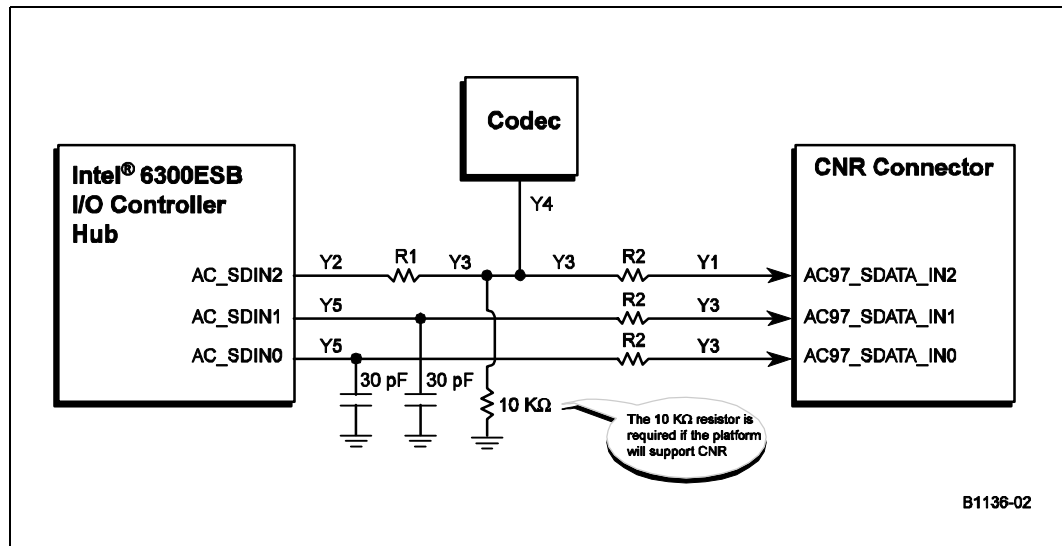


Table 71. AC '97 AC\_SDOUT/AC\_SYNC Routing Summary

Trace Impedance	AC '97 Routing Requirements	Trace Lengths	Series Termination Resistance	AC_SDOUT/AC_SYNC Signal Length Matching
60 $\Omega \pm 15\%$	5 mil width, 10 mil spacing (based on stackup assumptions in <a href="#">Section 3.2</a> )	L1 = 3 to 6 inches L2 = 3 to 6 inches L3 = 0.1 to 0.5 inches L4 = 3 to 6 inches	R1 = 34 $\Omega$ - 38 $\Omega$ R2 = R1	N/A

Figure 91. ICH AC'97 – AC\_SDIN Topology

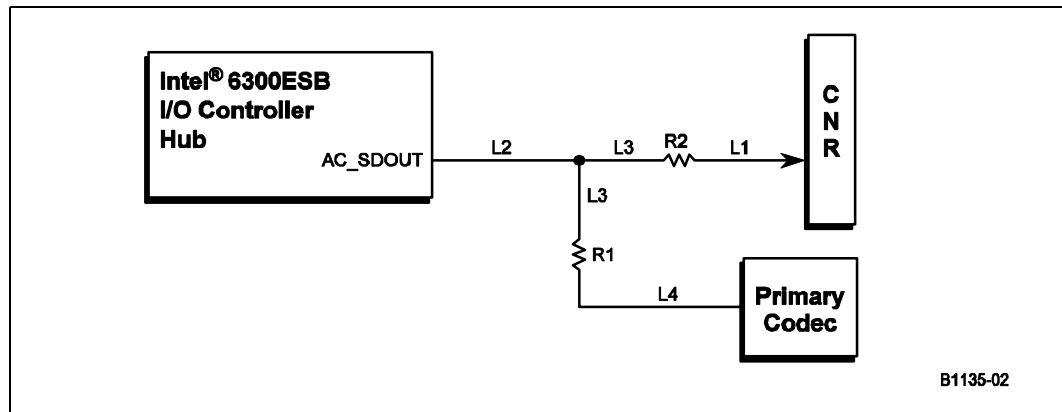


Table 72. AC '97 AC\_SDIN Routing Summary

Trace Impedance	AC '97 Routing Requirements	Trace Lengths	Series Termination Resistance	AC_SDIN Signal Length Matching
60 $\Omega \pm 15\%$	5 mil width, 10 mil spacing (based on stackup assumptions in <a href="#">Section 3.2</a> )	Y1 = 3 to 6 inches Y2 = 3 to 8 inches Y3 = 0.1 to 0.5 inches Y4 = 0.1 to 0.5 inches Y5 = 3 to 12 inches	R1 = 34 $\Omega$ - 38 $\Omega$ R2 = R1	N/A

**Note:** AC\_BIT\_CLK, SDATA\_OUT, SDATA\_IN, SYNC all need to be routed on the same layer and NO layer changes are allowed.

### 9.8.1 AC '97 Routing

To ensure the maximum performance of the codec, proper component placement and routing techniques are required. These techniques include properly isolating the codec, associated audio circuitry, analog power supplies, and analog ground planes, from the rest of the motherboard. This includes plane splits and proper routing of signals not associated with the audio section. Contact your vendor for device-specific recommendations.

The basic recommendations are as follows:

- Special consideration must be given for the ground return paths for the analog signals.
- Digital signals routed in the vicinity of the analog audio signals must not cross the power plane split lines. Analog and digital signals should be located as far as possible from each other.
- Partition the board with all analog components grouped together in one area and all digital components in another.
- Separate analog and digital ground planes must be provided, with the digital components over the digital ground plane, and the analog components, including the analog power regulators, over the analog ground plane. The split between planes must be a minimum of 0.05 inches wide.
- Keep digital signal traces, especially the clock, as far as possible from the analog input and voltage reference pins.
- Do not completely isolate the analog/audio ground plane from the rest of the board ground plane. There should be a single point (0.25 inches to 0.5 inches wide) where the analog/isolated ground plane connects to the main ground plane.
- Any signals entering or leaving the analog area must cross the ground split in the area where the analog ground is attached to the main motherboard ground. That is, no signal should cross the split/gap between the ground planes, which would cause a ground loop, thereby greatly increasing EMI emissions and degrading the analog and digital signal quality.
- Analog power and signal traces should be routed over the analog ground plane.
- Digital power and signal traces should be routed over the digital ground plane.
- Bypassing and decoupling capacitors should be close to the IC pins, or positioned for the shortest connections to pins, with wide traces to reduce impedance.



- All resistors in the signal path or on the voltage reference should be metal film. Carbon resistors may be used for DC voltages and the power supply path, where the voltage coefficient, temperature coefficient, and noise are not factors.
- Regions between analog signal traces should be filled with copper, which should be electrically attached to the analog ground plane. Regions between digital signal traces should be filled with copper, which should be electrically attached to the digital ground plane
- Locate the crystal or oscillator close to the codec.

## 9.8.2 Motherboard Implementation

The following design considerations are provided for the implementation of a 6300ESB ICH using AC '97. These design guidelines have been developed to ensure maximum flexibility for board designers, while reducing the risk of board-related issues. These recommendations are not the only implementation or a complete checklist, but they are based on the 6300ESB ICH.

- Active Components such as FET switches, buffers or logic states should not be implemented on the AC-link signals, except for AC\_RST#. Doing so would potentially interfere with timing margins and signal integrity.
- The 6300ESB ICH supports wake-on-ring from S1-S5 states through the AC '97 link. The codec asserts AC\_SDIN to wake the system. To provide wake capability and/or caller ID, standby power must be provided to the modem codec. In this case, the modem codec may be powered by either its own or an external clock source. When no codec is attached to the link, internal pull-downs will prevent the inputs from floating, so external resistors are not required.
- PC\_BEEP should be routed through the audio codec. Care should be taken to avoid the introduction of a pop when powering the mixer up or down.

### 9.8.2.1 Valid Codec Configurations

Table 73 describes the valid codec configurations.

**Table 73. Supported Codec Configurations**

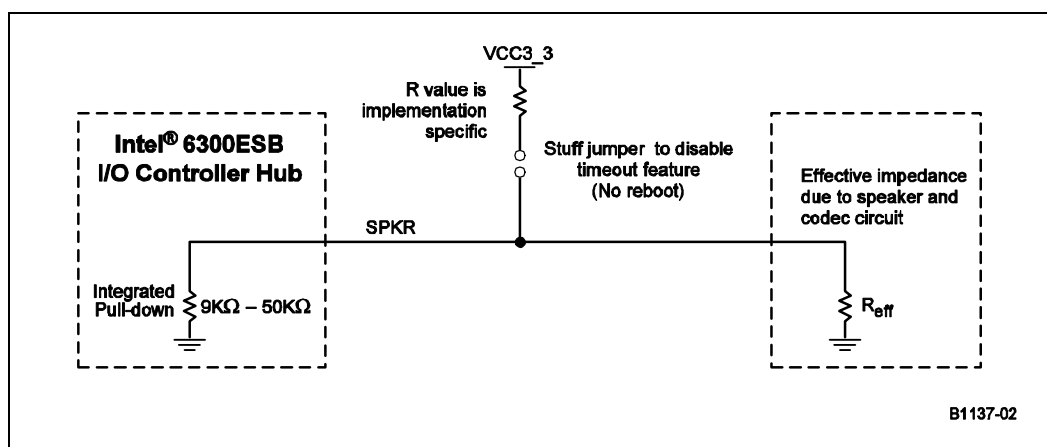
Option	Primary Codec	Secondary Codec	Tertiary Codec
1	Audio	Audio	Audio
2	Audio	Audio	Modem
3	Audio	Audio	Audio/Modem
4	Audio	Modem	Audio
5	Audio	Audio/Modem	Audio
6	Audio/Modem	Audio	Audio
7	Modem	-	-

**NOTE:** For power management reasons, codec power management registers are in audio space. As a result, when there is an audio codec in the system it must be Primary. In addition, there cannot be two modems in a system since there is only one set of modem DMA channels.

### 9.8.3 SPKR Pin Consideration

SPKR is used as both the output signal to the system speaker and as a functional strap. The strap function enables or disables the TCO Timer Reboot function based on the state of the SPKR pin on the rising edge of PWROK. When enabled, the 6300ESB ICH sends an SMI# to the processor upon a TCO timer time out. The status of this strap is readable through the NO\_REBOOT bit (bit 1, D31: F0, Offset D4h). The SPKR signal has a weak integrated pull-down resistor (the resistor is only enabled during boot/reset). Therefore, its default state is a logical zero or set to reboot. To disable the feature, a jumper may be populated to pull the signal line high (see Figure 92). The value of the pull-up must be such that the voltage divider output caused by the pull-up, the effective pull-down ( $R_{eff}$ ), and the 6300ESB ICH's integrated pull-down resistor will be read as logic high ( $0.5 V_{CC3.3}$  to  $V_{CC3.3} + 0.5 V$ ).

Figure 92. Example Speaker Circuit



### 9.8.4 AC\_SDOUT Pin Consideration

AC\_SDOUT is used as both the output signal to the system speaker and as a functional strap. The strap function enables or disables the Safe Mode function based on the state of the AC\_SDOUT pin on the rising edge of PWROK. When enabled, the 6300ESB ICH will force the appropriate bits to engage Safe Mode. The status of this strap is readable through the SAFE\_MODE bit (bit 2, D31: F0, Offset D4h). The AC\_SDOUT signal has a weak integrated pull-down resistor (the resistor is only enabled during boot/reset). Therefore, its default state is a logical zero or set to reboot.

To disable the feature, a jumper may be populated to pull the signal line high (see Figure 93). The value of the pull-up must be such that the voltage divider output caused by the pull-up and the 6300ESB ICH's integrated pull-down resistor will be read as logic high ( $0.5 V_{CC3.3}$  to  $V_{CC3.3} + 0.5 V$ ).

### 9.8.5 SIU0\_DTR# Pin Consideration

SIU0\_DTR# is used as both the output signal to the system speaker and as a functional strap. The strap function enables or disables the Top Swap function based on the state of the SIU0\_DTR# pin on the rising edge of PWROK. When disabled, the 6300ESB ICH will not invert A16 for cycles targeting FWH BIOS space. The status of this strap is readable through the TOP\_SWAP bit (bit 5, D31: F0, Offset D5h). The SIU0\_DTR# signal has a weak integrated pull-up resistor (the resistor is only enabled during boot/reset). Therefore, its default state is a logical zero or set to reboot.

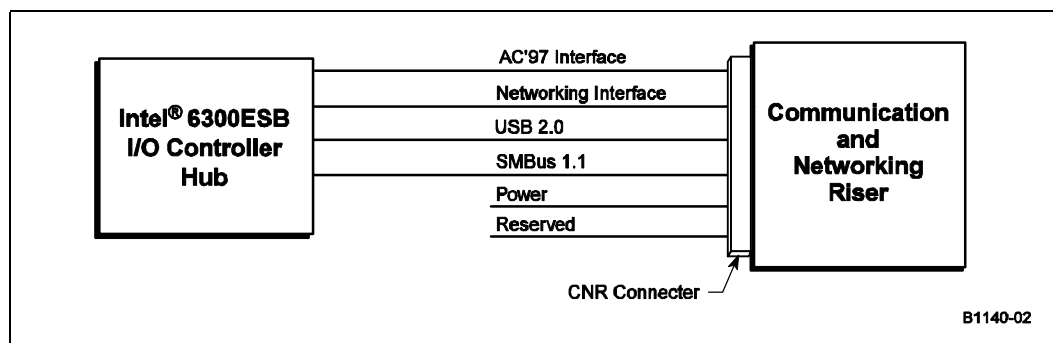
To disable the feature, a jumper may be populated to pull the signal line low (see Figure 94). The value of the pull-down must be such that the voltage divider output caused by the pull-down and the 6300ESB ICH's integrated pull-up resistor will be read as logic low.

## 9.9 Communication Network Riser

The *Communication and Networking Riser (CNR) Specification* defines a hardware-scalable Original Equipment Manufacturer (OEM) motherboard riser and interface. This interface supports AC '97 multi-channel audio, V.90 analog modem, phone-line based networking, SMBus Interface Power Management Rev 1.1, and USB 2.0. The CNR Specification defines the interface, which should be configured prior to shipment of the system. Standard I/O expansion slots, such as those supported by the PCI bus architecture, are intended to continue serving as the upgrade medium. The CNR mechanically shares a PCI slot, therefore, the system designer will not sacrifice a PCI slot if they decide not to include a CNR in a particular build.

Figure 93 shows the interface for the CNR connector. Refer to the appropriate section of this document for the corresponding design and layout guidelines. Refer to the *CNR Specification* for additional information.

Figure 93. CNR Interface



### 9.9.1 AC '97 Audio Codec Detect Circuit and Configuration Options

Table 74 provides general circuits to implement a number of different codec configurations. Please refer to the *Communication Network Riser Specification, Revision 1.2*, for Intel's recommended codec configurations

Table 74. Signal Descriptions

Signal	Description
CDC_DN_ENAB#	When low, indicates that the codec on the motherboard is enabled and primary on the AC97 Interface. When high, indicates that the motherboard codec(s) must be removed from the AC '97 Interface (held in reset), because the CNR codec(s) will be the primary device(s) on the AC '97 Interface.
AC97_RESET#	Reset signal from the AC '97 Digital Controller (6300ESB ICH).
SDATA_INn	AC '97 serial data from an AC '97-compliant codec to an AC '97-compliant controller (i.e., the 6300ESB ICH).

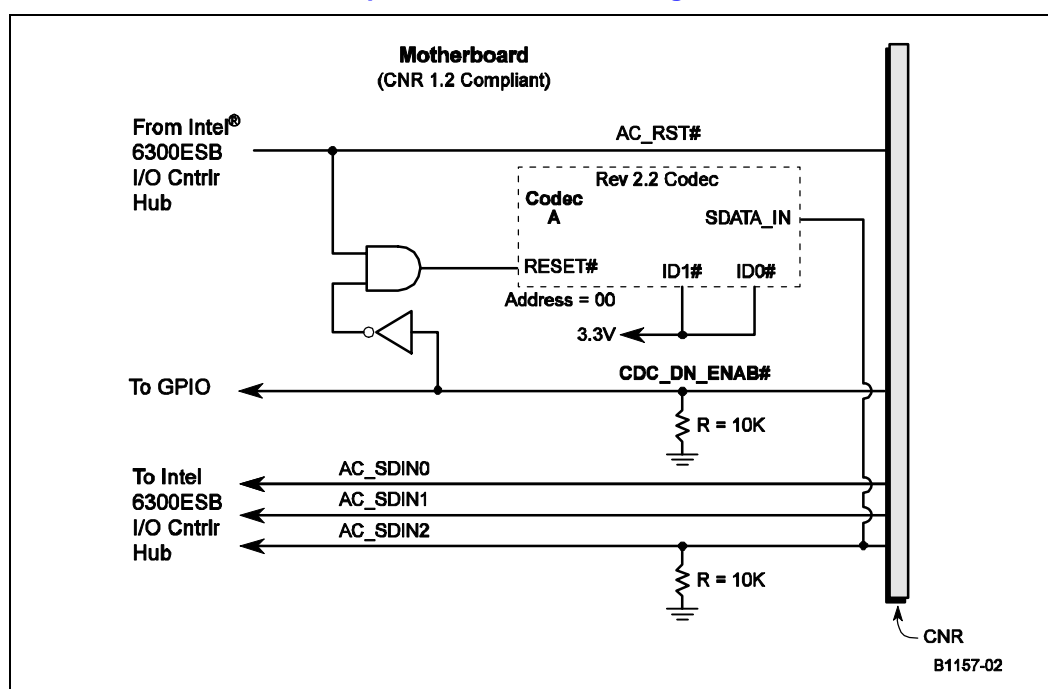
#### 9.9.1.1 CNR 1.2 AC '97 Disable and Demotion Rules for the Motherboard

The following are the CNR 1.1/1.2 AC '97 Disable and Demotion Rules for the motherboard.

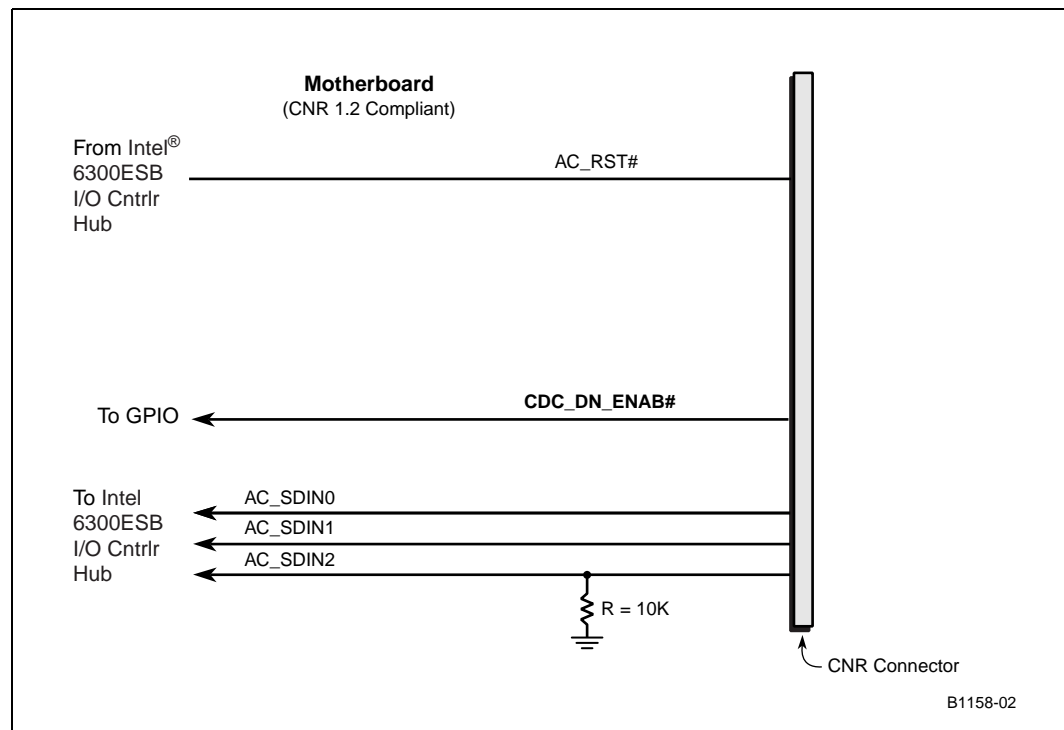
- All AC '97 Rev 2.2 codecs on the motherboard **must** always disable themselves when the CDC\_DN\_ENAB# signal is in a high state.
- A motherboard AC '97 codec **must** never change its address or SDATA\_IN line used, regardless of the state of the CDC\_DN\_ENAB# signal.
- On a motherboard containing an AC '97 Controller supporting three AC '97 Codecs, the AC '97 Rev. 2.2 codec on the motherboard **must** be connected to the SDATA\_IN2 signal of the CNR connector.

The above rules allow for forward and backward compatibility between CNR Version 1.1/1.2 cards. For more information on chaining consult the *Communication Network Riser Specification, Revision 1.2*.

**Figure 94. Motherboard AC '97 CNR Implementation With a Single Codec Down On Board**



**Figure 95. Motherboard AC '97 CNR Implementation Without Codec Down On Board**



## 9.9.2 CNR Routing Summary

Table 75 represents a summary of the various interfaces routing requirements to the CNR.

**Table 75. CNR Routing Summary**

Trace Impedance	CNR Routing Requirements	Maximum Trace Length to CNR connector	Signal Length Matching	Signal Referencing
90 $\Omega$ Differential	USB (7.5 on 7.5) (See <a href="#">Section 9.10.1.6</a> for more details)	10 inches	No more than 150 mils trace mismatch.	Ground
60 $\Omega \pm 15\%$	AC '97 (5 on 10)	AC_BIT_CLK (See <a href="#">Table 70</a> ) AC_SDOUT (See <a href="#">Table 71</a> ) AC_SDIN (See <a href="#">Table 72</a> )	N/A	Ground

## 9.10 USB 2.0

### 9.10.1 Layout Guidelines

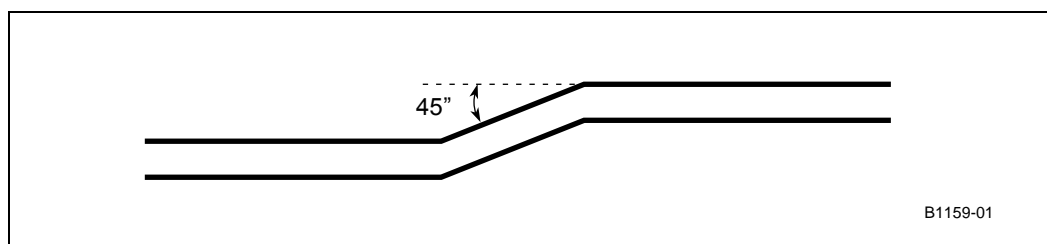
**Note:** These routing guidelines are created using the stack-ups described in [Section 3.2, “Board Stack-Up”](#) on page 34.

#### 9.10.1.1 General Routing and Placement

Use the following general routing and placement guidelines when laying out a new design. These guidelines will help to minimize signal quality and EMI problems.

1. Place the 6300ESB ICH and major components on the un-routed board first. With minimum trace lengths, route high-speed clock, periodic signals, and USB 2.0 differential pairs first. Maintain maximum possible distance between high-speed clocks/periodic signals to USB 2.0 differential pairs and any connector leaving the PCB (i.e., I/O connectors, control and signal headers, or power connectors).
2. USB 2.0 signals should be **ground referenced** (on the recommended stackup this would be the bottom signal layer).
3. Route USB 2.0 signals using a minimum of vias and corners. This reduces reflections and impedance changes.
4. When it becomes necessary to turn 90°, use two 45° turns or an arc instead of making a single 90° turn. This reduces reflections on the signal by minimizing impedance discontinuities (see [Figure 96](#)).

**Figure 96. Trace Routing**



5. Do not route USB 2.0 traces under crystals, oscillators, clock synthesizers, magnetic devices, or ICs that use and/or duplicate clocks.
6. Stubs on High-speed USB signals should be avoided, as stubs will cause signal reflections and affect signal quality. When a stub is unavoidable in the design, the total of all the stubs on a particular line should not be greater than 200 mils.
7. Route all traces over continuous planes (VCC or GND), with no interruptions. Avoid crossing over anti-etch (plane splits) when possible. Crossing over anti-etch increases inductance and radiation levels by forcing a greater loop area. Likewise, avoid changing layers with USB 2.0 traces as much as practical. It is preferable to change layers to avoid crossing a plane split. Refer to [Section 9.10.2, “Plane Splits, Voids, and Cut-Outs \(Anti-Etch\)”](#) on page 149.
8. Separate signal traces into similar categories and route similar signal traces together (such as routing differential pairs together).
9. Keep the USB 2.0 signals clear of the core logic set. High current transients are produced during internal state transitions and may be very difficult to filter out.

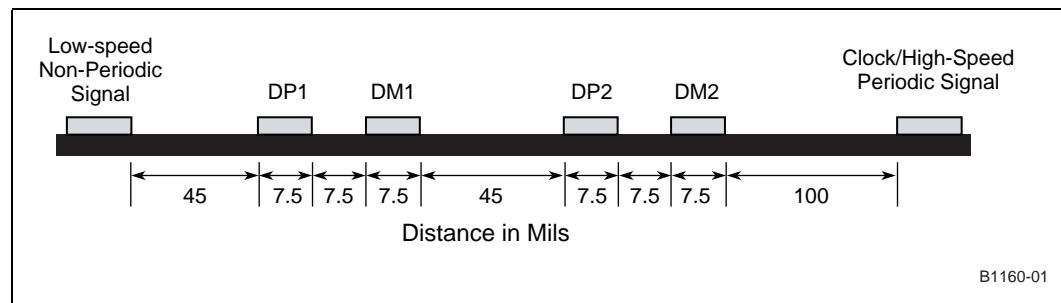
10. Follow the 20 x h thumb rule by keeping traces at least 20 x (height above the plane) away from the edge of the plane (VCC or GND, depending on the plane the trace is over). For the suggested stackup the height above the plane is 4.5 mils. This calculates to a 90 mils spacing requirement from the edge of the plane. This helps prevent the coupling of the signal onto adjacent wires and also helps prevent free radiation of the signal from the edge of the PCB.

### 9.10.1.2 USB 2.0 Trace Separation

Use the following separation guidelines. [Figure 97](#) provides an illustration of the recommended trace spacing.

1. Maintain parallelism between USB differential signals with the trace spacing needed to achieve the target differential impedance. Deviations will normally occur due to package breakout and routing to connector pins. Just ensure the amount and length of the deviations are kept to the minimum possible.
2. Use an impedance calculator to determine the trace width and spacing required for the specific board stackup being used; keeping in mind the target differential impedance.
3. Minimize the length of high-speed clock and periodic signal traces that run parallel to high-speed USB signal lines, to minimize crosstalk. Based on EMI testing experience, the minimum suggested spacing to clock signals is 100 mils.
4. Based on simulation data, use 45 mils minimum spacing between high-speed USB signal pairs and other signal traces for optimal signal quality. This helps to prevent crosstalk.

**Figure 97. Recommended General USB Trace Spacing ( $60\ \Omega \pm 15\%$ )**



### 9.10.1.3 USB BIAS Connections

The USBRBIAS pin and the USBRBIAS# pin may be shorted and routed 5 mils width, 5 mils spacing, to one end of a  $22.6\ \Omega \pm 1\%$  resistor to ground. Place the resistor within 500 mils of the 6300ESB ICH and avoid routing next to clock pins. (See [Figure 98](#) and [Table 76](#) for more information.)

Figure 98. USB BIAS Connections

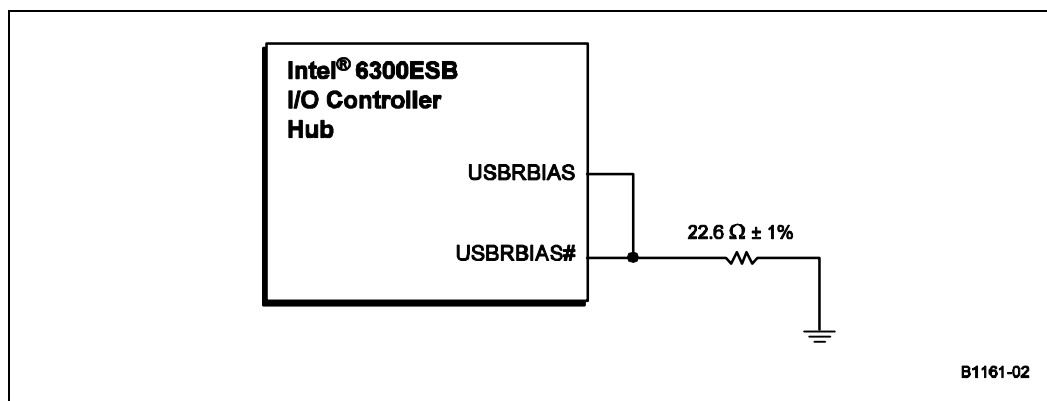


Table 76. USB BIAS Routing Summary

Trace Impedance	USBRBIAS/USBRBIAS# Routing Requirements	Maximum Trace Length	Signal Length Matching	Signal Referencing
60 $\Omega \pm 15\%$	5 mils width, 5 mils spacing	500 mils	N.A.	N.A.

#### 9.10.1.4 USB 2.0 Termination

A common-mode choke should be used to terminate the USB 2.0 bus. Place the common-mode choke as close as possible to the connector pins. See [Section 9.10.4, “EMI Considerations”](#) on [page 150](#) for details.

#### 9.10.1.5 USB 2.0 Trace Length Pair Matching

USB 2.0 signal pair traces should be trace length matched. Max trace length mismatch between USB 2.0 signal pair should not be greater than 60 mils.

#### 9.10.1.6 USB 2.0 Trace Length Guidelines

[Table 77](#) and [Table 78](#) provide trace length guidelines.

Table 77. USB 2.0 Back Panel Trace Length Guidelines (Common-Mode Choke, 60  $\Omega \pm 15\%$ )

Differential Impedance	Pair Spacing	Signal Referencing	Signal Matching	Maximum Motherboard Trace Length
90 $\pm 15\%$	45 mils	Ground	The max mismatch between data pairs should not be greater than 60 mils	7.75 inches
	80 mils			10.4 inches

**NOTE:** Two options are given for motherboard trace length; choose the parameters that best suit your system.



**Table 78. USB 2.0 CNR Trace Length Guidelines (Common-Mode Choke,  $60\ \Omega \pm 15\%$ )**

Differential Impedance	Pair Spacing	Maximum Motherboard Trace Length	Maximum CNR Card Length	Signal Matching
$90 \pm 15\%$	50 mils	1.0 inches	6 inches	The max mismatch between data pairs should not be greater than 60 mils
		2.4 inches	4 inches	
		3.6 inches	2 inches	
	80 mils	2.3 inches	6 inches	
		3.9 inches	4 inches	
		6.3 inches	2 inches	

**NOTE:** Many options are given for motherboard trace length and CNR card trace length, choose the parameters that best suit your system.

**Table 79. USB 2.0 Front Panel Trace Length Guidelines (Common-Mode Choke,  $60\ \Omega \pm 15\%$ )**

Differential Impedance	Pair Spacing	Maximum Cable Length	Motherboard Trace Length	Front Panel Length	Signal Matching
$90 \pm 15\%$	50 mils	9.1 inches	= 4.5 inches	= 1.5 inches	The max mismatch between data pairs should not be greater than 60 mils
		6.5 inches	= 6.0 inches	1.5 - 2.5 inches	

**NOTE:** Two options are given for motherboard trace length, cable length and front panel length; choose the parameters that best suit your system.

## 9.10.2 Plane Splits, Voids, and Cut-Outs (Anti-Etch)

The following guidelines apply to the use of plane splits voids and cut-outs.

### 9.10.2.1 V<sub>CC</sub> Plane Splits, Voids, and Cut-Outs (Anti-Etch)

Use the following guidelines for the V<sub>CC</sub> plane.

Traces should not cross anti-etch, for it greatly increases the return path for those signal traces. This applies to USB 2.0 signals, high-speed clocks, and signal traces as well as slower signal traces which might be coupling to them. USB signaling is not purely differential in all speeds (i.e., the Full-speed Single Ended Zero is common mode).

**Note:** Avoid routing of USB 2.0 signals 25 mils of any anti-etch to avoid coupling to the next split or radiating from the edge of the PCB.

When breaking signals out from packages it is sometimes very difficult to avoid crossing plane splits or changing signal layers, particularly in today's motherboard environment that uses several different voltage planes. Changing signal layers is preferable to crossing plane splits when a choice has to be made between one or the other.

When crossing a plane split is completely unavoidable, proper placement of stitching capacitors may minimize the adverse effects on EMI and signal quality performance caused by crossing the split. Stitching capacitors are small-valued capacitors (1  $\mu$ F or lower in value) that bridge voltage plane splits close to where high-speed signals or clocks cross the plane split. The capacitor ends

should tie to each plane separated by the split. They are also used to bridge, or bypass, power and ground planes close to where a high-speed signal changes layers. As an example of bridging plane splits, a plane split that separates  $V_{CC5}$  and  $V_{CC3.3}$  planes should have a stitching capacitor placed near any high-speed signal crossing. One side of the capacitor should tie to  $V_{CC5}$  and the other side should tie to  $V_{CC3.3}$ . Stitching capacitors provide a high frequency current return path across plane splits. They minimize the impedance discontinuity and current loop area that crossing a plane split creates.

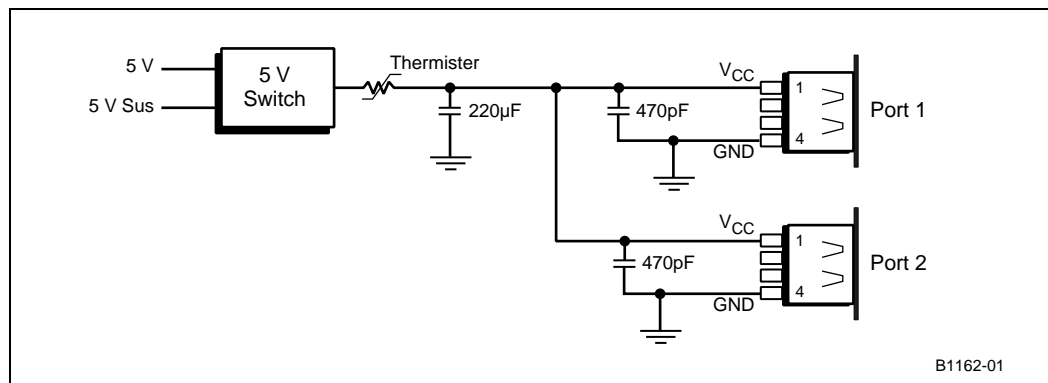
### 9.10.2.2 GND Plane Splits, Voids, and Cut-Outs (Anti-Etch)

Avoid anti-etch on the GND plane.

### 9.10.3 USB Power Line Layout Topology

The following is a suggested topology for power distribution of  $V_{BUS}$  to USB ports. Circuits of this type provide two types of protection during dynamic attach and detach situations on the bus: inrush current limiting (droop) and dynamic detach fly back protection. These two different situations require both bulk capacitance (droop) and filtering capacitance (for dynamic detach fly back voltage filtering). It is important to minimize the inductance and resistance between the coupling capacitors and the USB ports. That is, capacitors should be placed as close as possible to the port and the power-carrying traces should be as wide as possible, preferably, a plane. Make the power-carrying traces wide enough that the system fuse will blow on an over current event. When the system fuse is rated at 1 amps, the power-carrying traces should be wide enough to carry at least 1.5 amps.

Figure 99. Good Downstream Power Connection



### 9.10.4 EMI Considerations

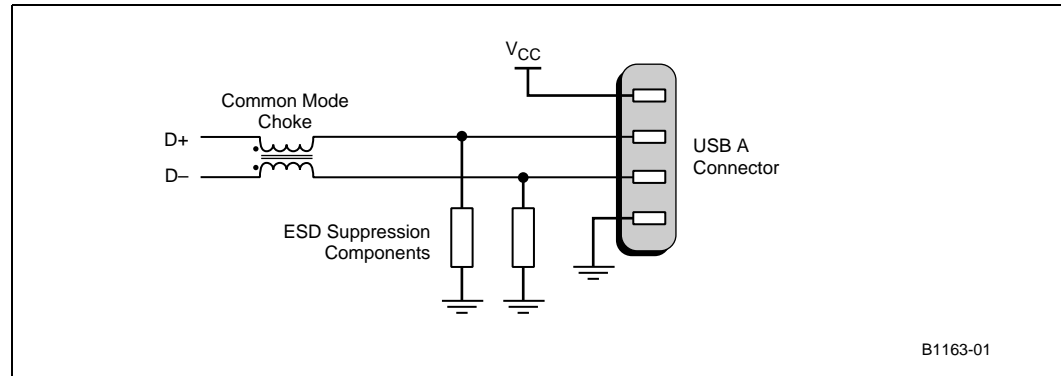
The following guidelines apply to the selection and placement of common mode chokes and ESD protection devices.

#### 9.10.4.1 Common-Mode Chokes

Testing has shown that common-mode chokes may provide required noise attenuation. A design should include a common-mode choke footprint to provide a stuffing option *in the event* the choke is needed to pass EMI testing. Figure 100 shows the schematic of a typical common-mode choke

and ESD suppression components. Place the choke as close as possible to the USB connector signal pins. In systems that route USB to a front panel header, place the choke on the front panel card. (See [Section 9.10.6.3, “Front Panel Connector Card”](#) on page 154 for more information.)

**Figure 100. A Common-Mode Choke**



Common mode chokes distort full-speed and high-speed signal quality. As the common mode impedance increases, the distortion will increase, so you should test the effects of the common mode choke on full speed and high-speed signal quality. Common-mode chokes with a target impedance of 80  $\Omega$  to 100  $\Omega$  at 100 MHz generally provide adequate noise attenuation.

Finding a common-mode choke that meets the designer’s needs is a two-step process.

1. A part must be chosen with the impedance value that provides the required noise attenuation. This is a function of the electrical and mechanical characteristics of the part chosen and the frequency and strength of the noise present on the USB traces that you are trying to suppress.
2. Once you have a part that gives passing EMI results the second step is to test the effect this part has on signal quality. Higher impedance common-mode chokes generally have a greater damaging effect on signal quality, so care must be used when increasing the impedance without doing thorough testing. Thorough testing includes checking the signal quality for low-speed, full-speed and high-speed USB operation.

## 9.10.5 ESD

Classic USB (1.0/1.1) provided ESD suppression using in-line ferrites and capacitors that formed a low pass filter. This technique does not work for USB 2.0 due to the much higher signal rate of high-speed data. A device that has been tested successfully is based on spark gap technology. Proper placement of any ESD protection device is on the data lines between the common-mode choke and the USB connector data pins as shown in [Figure 100](#). Other types of low-capacitance ESD protection devices may work as well but have not been investigated. As with the common mode choke solution, it is recommended to include footprints for some type of ESD protection device as a stuffing option in case it is needed to pass ESD testing.

## 9.10.6 Front Panel Solutions

### 9.10.6.1 Internal USB Cables

The front panel internal cable solution must meet all the requirements of Chapter 6 of the *Universal Serial Bus Specification, Revision 2.0*, for High-/Full-speed cabling for each port with the exceptions described in Cable Option 2. For more information refer to the *Front Panel I/O Connectivity Design Guide*.

#### 9.10.6.1.1 Internal Cable Option 1

Use standard High-speed/Full-speed compatible USB cables. These must meet all cabling requirements called out in Chapter 6 of the *Universal Serial Bus Specification, Revision 2.0*. Recommended motherboard mating connector pin-out is covered in detail in [Section 9.10.6.2](#).

#### 9.10.6.1.2 Internal Cable Option 2

Use custom cables that meet all of the requirements of Chapter 6 of the *Universal Serial Bus Specification, Revision 2.0*, with the following additions/exceptions.

1. They may share a common jacket, shield, and drain wire.
2. Two ports with signal pairs that share a common jacket may combine  $V_{BUS}$  and ground wires into a single wire provided the following conditions are met:
  - a. The bypass capacitance required by Section 7.2.4.1 of the *Universal Serial Bus Specification, Revision 2.0*, is physically located near the power and ground pins of the USB connectors. This is easiest to achieve by mounting the front panel USB connectors and the bypass capacitance on a small PCB (daughter card). Refer to the front panel daughter card referenced later for details.
  - b. Selecting proper wire size: A general rule for replacing two power or ground wires with a single wire is to choose a wire size from Table 6-6 in Section 6.6.3 of the *Universal Serial Bus Specification, Revision 2.0*, that has half the resistance of either of the two wires being combined. The data is provided for reference in [Table 80](#).

**Table 80. Conductor Resistance (Table 6-6 from the USB 2.0 Specification)**

American Wire Gauge (AWG)	Ohm ( $\Omega$ ) / 100 Meters Maximum
28	23.20
26	14.60
24	9.09
22	5.74
20	3.58

**Example:** Two 24 gauge (AWG) power or ground wires may be replaced with one 20 gauge wire.

Proper wire gauge selection is important to meet the voltage drop and droop requirements called out in the *Universal Serial Bus Specification, Revision 2.0*, at the USB connectors as well as at the stake pins on the PCB.

Placing the capacitance near the USB connectors for cables that share power and ground conductors is required to ensure the system passes droop requirements. Cables that provide individual power and ground conductors for each port may usually meet droop requirements by providing adequate capacitance near the motherboard mating connector, since droop is actually an effect felt by adjacent ports due to switching transients on the aggressor port. In the separate conductor case, all transients will be seen/dampened by the capacitance at the motherboard mating connector before they may cause problems with the adjacent port sharing the same cable. See sections 7.2.2 and 7.2.4.1 of the *Universal Serial Bus Specification, Revision 2.0*, for more details.

**Note:** Cables that contain more than two signal pairs are not recommended due to unpredictable impedance characteristics.

### 9.10.6.2 Motherboard/PCB Mating Connector

Proper selection of a motherboard mating connector for front panel USB support is important to ensure signal quality is not adversely affected due to a poor connector interface. The cable and PCB mating connector must also pass the TDR requirements listed in the *Universal Serial Bus Specification, Revision 2.0*.

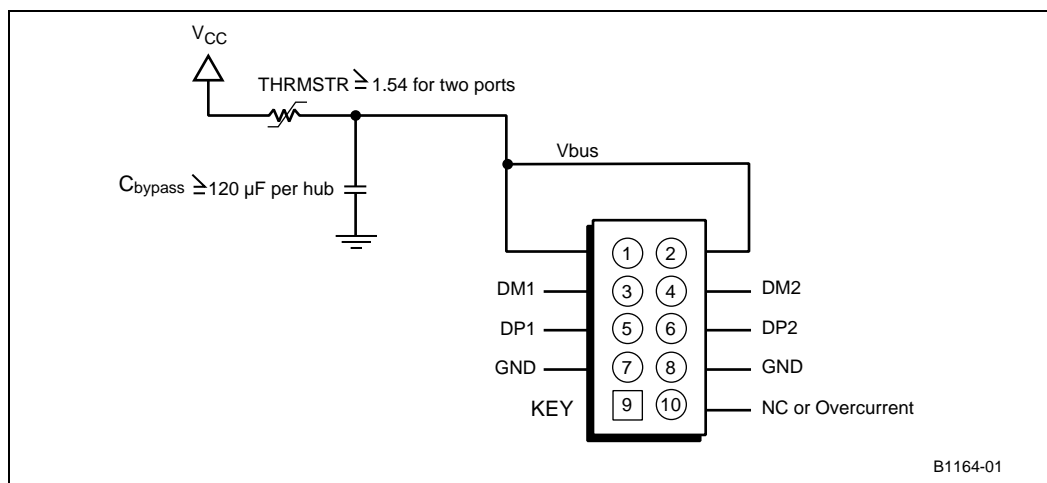
#### 9.10.6.2.1 Pin-Out

A ten pin, 0.1 inch pitch stake pin assembly is recommended with the pin-out listed in [Table 81](#) and schematic shown in [Figure 101](#).

**Table 81. Front Panel Header Pin-Out**

Pin	Description
1	Vcc
2	Vcc
3	Dm1
4	Dm2
5	Dp1
6	Dp2
7	GND
8	GND
9	Key
10	No connect or over-current sense

Figure 101. Front Panel Header Schematic



**Note:** It is **highly** recommended that the fuse element (thermistor) for the front panel header be included on the motherboard to protect the motherboard from damage in the following instances:

- If an un-fused front panel cable solution is used.
- If an un-keyed cable is inadvertently plugged onto the front panel USB connector.
- If the front panel cable is cut or damaged during assembly or manufacturing resulting in a short between  $V_{BUS}$  and ground.

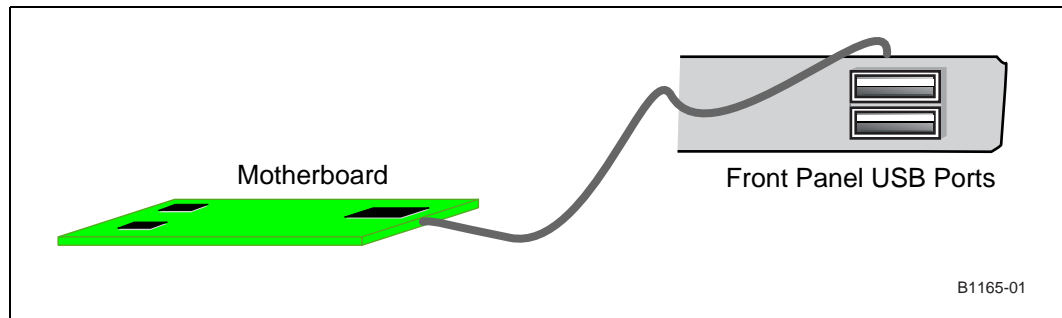
#### 9.10.6.2.2 Routing Considerations

Traces or surface shapes from  $V_{CC}$  to the thermistor, to  $C_{BYPASS}$  and to the connector power and ground pins should be at least 50 mils wide to ensure adequate current carrying capability. There should be double vias on power and ground nets, and the trace lengths should be kept as short as possible.

#### 9.10.6.3 Front Panel Connector Card

The best way to provide front or side panel support for USB is to use a daughter card and cable assembly. This allows the placement of the EMI/ESD suppression components right at the USB connector where they will be the most effective. Figure 102 shows the major components associated with a typical front/side panel USB solution that uses a front panel connector card. For more information refer to the *Front Panel I/O Connectivity Design Guide*.

**Figure 102. Motherboard Front Panel USB Support**



**Note:** When designing front panel I/O in a system where a connector card will be used ensure that there aren't duplicate EMI/ESD/thermistor components. Duplicate components will result in drop/droop and signal quality degradation or failure.

#### 9.10.6.3.1 Front Panel Daughter Card Design Guidelines

1. Place the  $V_{BUS}$  bypass capacitance, CMC, and ESD suppression components on the daughter card as close as possible to the connector pins.
2. Follow the same layout, routing and impedance control guidelines as specified for motherboards.
3. Minimize the trace length on the front panel connector card. Trace length less than two inches is recommended.
4. Use the same mating connector pin-out as outlined for the motherboard in [Section 9.10.6.2.1, "Pin-Out" on page 153](#).
5. Use the same routing guidelines as described in [Section 9.10.1, "Layout Guidelines" on page 146](#).
6. Trace length guidelines are given in [Table 77](#) and [Table 78](#).

## 9.11 Low Pin Count (LPC) Interface

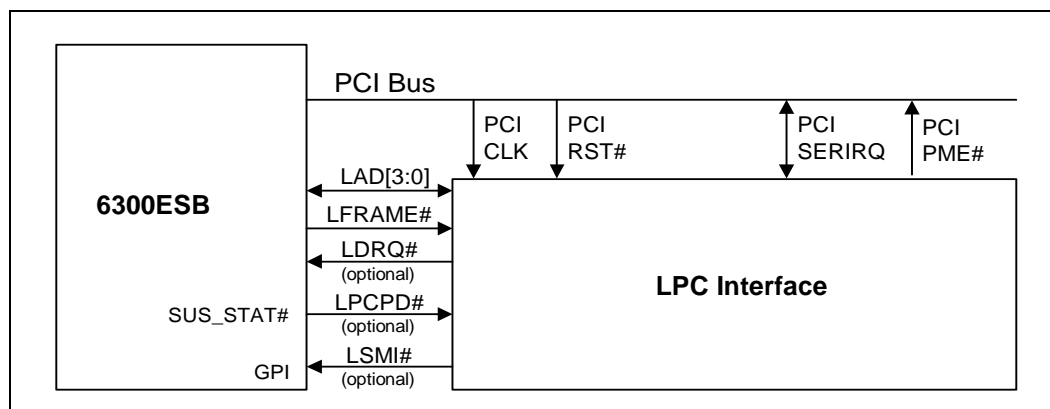
The 6300ESB ICH implements a Low Pin Count (LPC) Interface compliant with the *Low Pin Count Interface Specification Revision 1.0*. The following section provides design guidelines for proper interfacing with the LPC bus. These guidelines will help to minimize signal integrity issues and maintain conformance to LPC specifications.

The LPC Interface to the 6300ESB ICH is shown in [Figure 103](#). Note that the 6300ESB ICH implements all of the signals that are shown as optional, but peripherals are not required to do so. For the 6300ESB ICH:

- LSMI# may be connected to any of the 6300ESB ICH's GPIO signals, as they may be configured as inputs to generate an SMI#.
- The Super I/O's PME# may be connected to the PCI PME# signal. However, this may cause software problems. A better choice is to connect it to one of the 6300ESB ICH's GPIO signals, as they may be configured to generate an SCI.
- The 6300ESB ICH's SUS\_STAT# signal is connected directly to the LPCPD# signal.

All the other signals have the same name on the 6300ESB ICH and on the LPC Interface.

**Figure 103. LPC Interface Diagram**



### 9.11.1 General Routing and Placement

Use the following general routing and placement guidelines when laying out a new design.

1. LPC signals should be *ground referenced*.
2. Route all traces using microstrip or stripline over continuous planes (Vcc or GND), with no interruptions. Avoid crossing over anti-etch if at all possible. Any discontinuity or split in the ground plane may cause signal reflections and should be avoided.
3. Route LPC signals using a minimum of vias and corners. This reduces reflections and impedance changes.
4. No 90 degree bends or stubs.



### 9.11.2 LPC Trace Length Matching

LPC clock traces should be trace length matched. Max trace length mismatch between clocks coming from the clock driver should be no greater than 250 mils.

### 9.11.3 LPC Interface Routing Guidelines

Figure 104. LPC Interface Topology

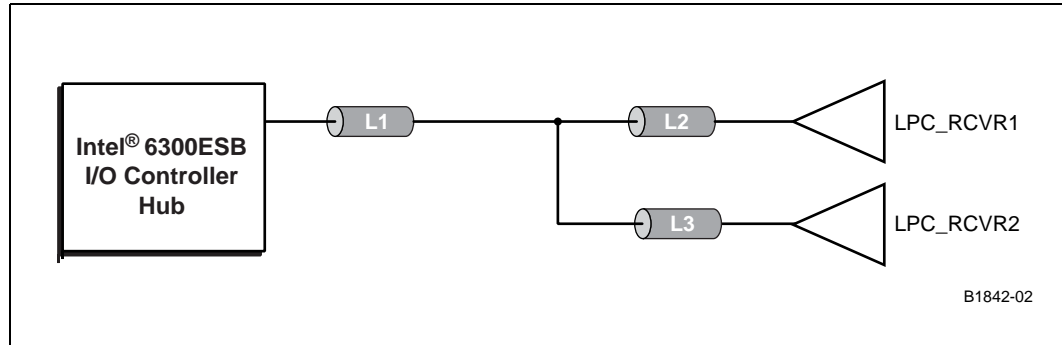


Table 82. LPC Interface Routing Summary

Trace Impedance	LPC Routing Requirements	Trace Lengths	LPC Clock Length Matching
60 $\Omega$ $\pm$ 15%	5 mil width, 12 mil spacing (based on stackup assumptions in <a href="#">Section 3.2</a> )	L1 = 2 to 8 inches L2 = 0 to 6 inches L3 = 0 to 6 inches	No more than 0.25 inches (250 mils) difference between clock signals.

## 9.12 SMBus 2.0/SMLink Interface

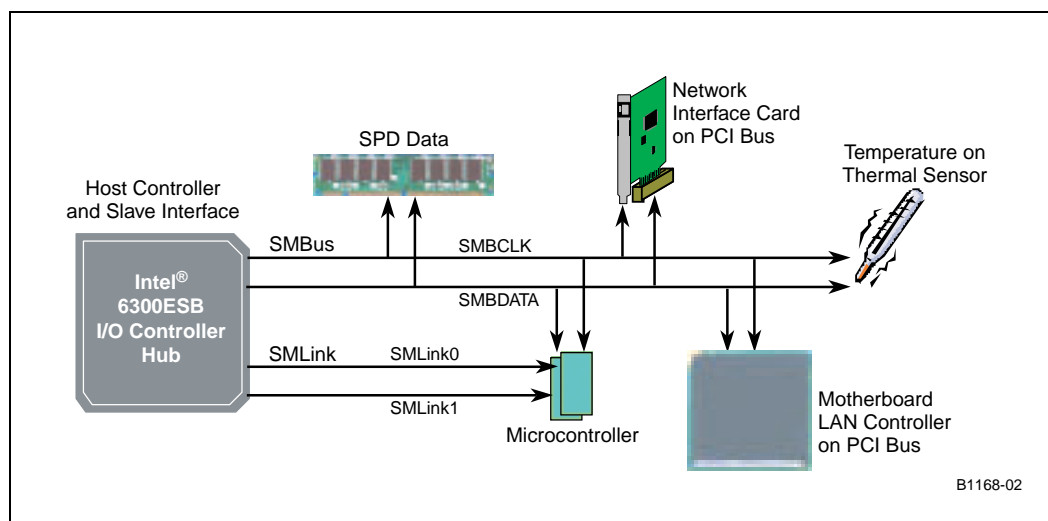
The SMBus interface on the 6300ESB ICH uses two signals SMBCLK and SMBDATA to send and receive data from components residing on the bus (see Figure 105). These signals are used exclusively by the SMBus Host Controller. The SMBus Host Controller resides inside the 6300ESB ICH.

The 6300ESB ICH incorporates a SMLink interface supporting Alert on LAN\*, Alert on LAN2\* and a slave functionality. It uses two signals SMLINK [1:0]. SMLINK[0] corresponds to an SMBus clock signal and SMLINK[1] corresponds to an SMBus data signal. These signals are part of the SMB Slave Interface.

For Alert on LAN\* functionality, the 6300ESB ICH transmits heartbeat and event messages over the interface. When using the 82562EM/82562EX Platform LAN Connect Component, it will claim the SMLink heartbeat and event messages and send them out over the network. An external, Alert on LAN2\*-enabled LAN Controller (e.g., the 82562EM/82562EX 10/100 Mbps Platform LAN Connect) will connect to the SMLink signals to receive heartbeat and event messages, as well as access the SMBus Slave Interface. The slave interface function allows an external microcontroller to perform various functions. For example, the slave write interface may reset or wake a system, generate SMI# or interrupts, and send a message. The slave read interface may read the system power state, read the watchdog timer status, and read system status bits.

Both the SMBus Host Controller and the SMBus Slave Interface obey the SMBus 1.0 protocol, so the two interfaces may be externally wire-ORed together to allow an external management ASIC (such as the 82562EM/82562EX 10/100 Mbps Platform LAN Connect) to access targets on the SMBus as well as the 6300ESB ICH Slave interface. Additionally, the 6300ESB ICH supports slave functionality, including the Host Notify protocol, on the SMLink pins.

**Figure 105. SMBUS 2.0/SMLink Interface**



**Note:** Intel does not support access of the 6300ESB ICH SMBus Slave Interface by the 6300ESB ICH SMBus Host Controller. Refer to the *Intel 6300ESB ICH External Design Specification* for full functionality descriptions of the SMLink and SMBus interface.

## 9.12.1 SMBus Architecture & Design Considerations

### 9.12.1.1 SMBus Design Considerations

There is not a single SMBus design solution that will work for all platforms. One must consider the total bus capacitance and device capabilities when designing SMBus segments. Routing SMBus to the PCI slots makes the design process even more challenging since they add so much capacitance to the bus. This extra capacitance has a large affect on the bus time constant which in turn affects the bus rise and fall times.

Primary considerations in the design process are:

- Device class (High/Low power). Most designs use primarily High Power Devices.
- Mixed Power Architecture. If there are devices that must run in S3, special considerations must be made (see [Section 9.12.1.3](#)).
- Amount of  $V_{CC-SUSPEND}$  current available (i.e., minimizing load of  $V_{CC-SUSPEND}$ ).

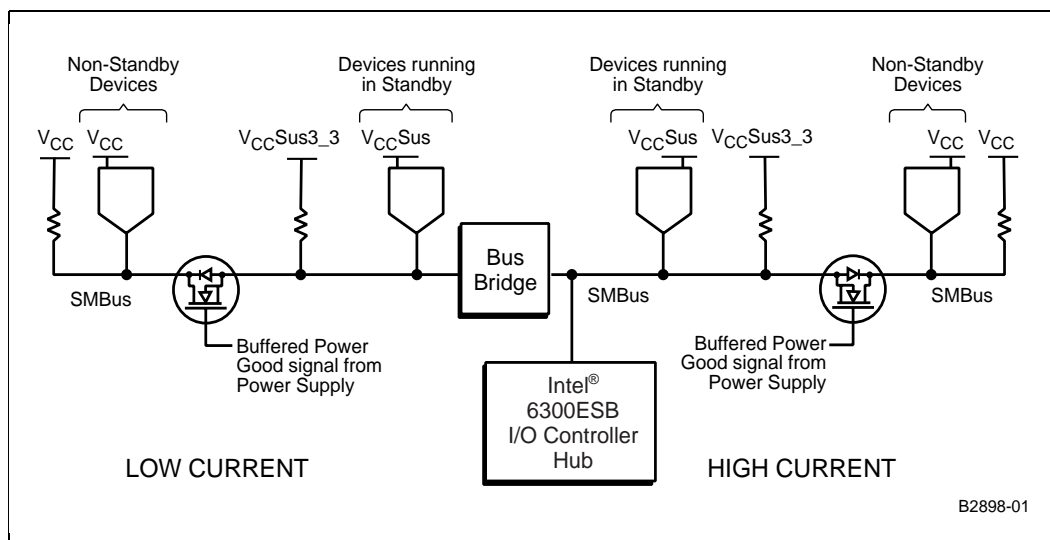
### 9.12.1.2 General Design Issues / Notes

Regardless of the architecture used, there are some general considerations.

- The pull-up resistor size for the SMBus data and clock signals is dependent on the bus load (this includes all device leakage currents). Generally, the SMBus device that may sink the least amount of current is the limiting agent on how small the resistor may be. The pull-up resistor may not be made so large that the bus time constant (Resistance X Capacitance) does not meet the SMBus rise and time specification.
- The maximum bus capacitance that a physical segment may reach is 400 pF.
- The 6300ESB ICH does not run SMBus cycles while in S3.
- SMBus devices that may operate in STR must be powered by the  $V_{CC-SUSPEND}$  supply.
- When the SMBus is connected to the PCI Bus, it must be connected to all PCI slots in the system.

### 9.12.1.3 High Power/Low Power Mixed Architecture

This design allows for current isolation of high and low current devices while also allowing SMBus devices to communicate while in S3.  $V_{CC-SUSPEND}$  leakage is minimized by keeping non-essential devices on the core supply. This is accomplished by the use of a FET to isolate the devices powered by the core and suspend supplies. See [Figure 106](#).

**Figure 106. High Power/Low Power Mixed  $V_{CC\_SUSPEND}/V_{CC\_CORE}$  Architecture****NOTES:**

1. Added considerations for mixed architecture.
2. The bus switch must be powered by  $V_{CC\_SUSPEND}$ .
3. Devices powered by the  $V_{CC\_SUSPEND}$  well must not drive into other devices that are powered off. This is accomplished with the bus switch.
4. The bus bridge can be a device like the Philips\* PCA9515.

**9.12.1.4 Calculating the Physical Segment Pull-Up Resistor**

The following tables are provided as a reference for calculating the value of the pull-up resistor that may be used for a physical bus segment. When any physical bus segment exceeds 400 pF, then a bus bridge device such as the Philips PCA9515 must be used to separate the physical segment into two segments that individually have a bus capacitance less than 400 pF.

**Table 83. Bus Capacitance Reference Chart (Sheet 1 of 2)**

Device	# of Devices/ Trace Length	Capacitance Includes	Capacitor (pF)
6300ESB ICH	1	Pin capacitance	12
CK409	1	Pin capacitance	10
DIMMS/RIMMS	2	Pin capacitance (10 pF) + 1 inch worth of trace capacitance (2 pF/inch) per DIMM/RIMM and 2 pF connector capacitance per DIMM/RIMM.	28
	3		42
PCI	2	Each PCI add-in card is allowed up to 40 pF + 3 pF per each connector.	86
	3		129
	4		172
	5		215
SMBus Trace Length in inches	= 24	2 pF per inch of trace length	48

**Table 83. Bus Capacitance Reference Chart (Sheet 2 of 2)**

Device	# of Devices/ Trace Length	Capacitance Includes	Capacitor (pF)
	= 36		72
	= 48		96
CNR	1	Pin capacitance (10 pF) + 6 inch worth of trace capacitance (2 pF/inch) and 2 pF connector capacitance.	24

**Table 84. Bus Capacitance/Pull-Up Resistor Relationship**

Physical Bus Segment Capacitance	Pull-Up Range (For Vcc = 3.3 V)
0 to 100 pF	8.2K $\Omega$ to 1.2 K $\Omega$
100 to 200 pF	4.7K $\Omega$ to 1.2 K $\Omega$
200 to 300 pF	3.3K $\Omega$ to 1.2 K $\Omega$
300 to 400 pF	2.2K $\Omega$ to 1.2 K $\Omega$

## 9.13 PCI

The 6300ESB ICH provides a PCI Bus interface that is compliant with the *PCI Local Bus Specification, Revision 2.2*. The implementation is optimized for high-performance data streaming when the 6300ESB ICH is acting as either the target or the initiator on the PCI bus. For more information on the PCI Bus interface, please refer to the *PCI Local Bus Specification*.

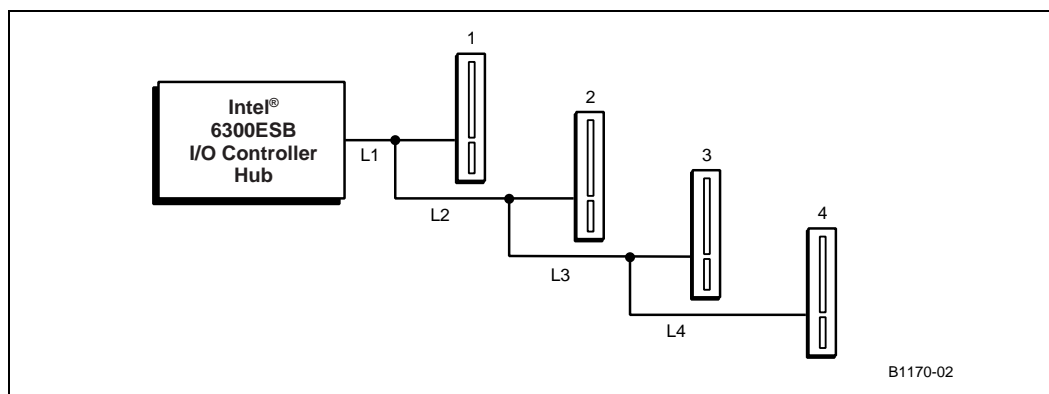
### 9.13.1 PCI Routing Summary

The following represents a summary of the routing guidelines for the PCI devices. The 6300ESB ICH supports four PCI devices. Simulations assume that PCI cards follow the *PCI Local Bus Specification* trace length guidelines.

**Note:** These routing guidelines are created using the stack-up described in [Section 3.2, “Board Stack-Up”](#) on page 34.

**Note:** The following guidelines apply to platforms with nominal impedances of  $60\ \Omega \pm 15\%$ .

**Figure 107. PCI Bus Layout Example**



**Note:** When a CNR connector is placed on the platform, it will share a slot space with one of the PCI slots. However, it will not take away from the slot functionality unless the CNR slot is occupied by a CNR card.

**Figure 108. PCI Bus Layout Example with IDSEL**

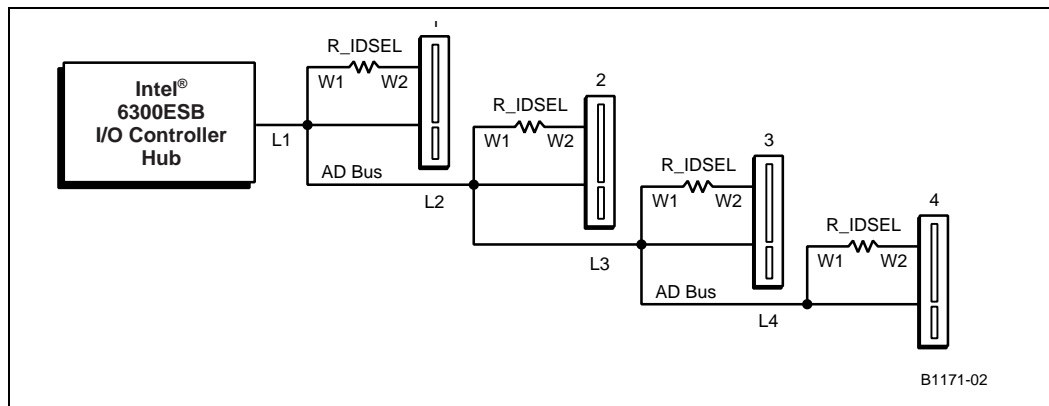


Table 85. PCI Data Signals Routing Summary

Trace Impedance	PCI Routing Requirements	Topology	Maximum Trace Length L1 L2 L3 L4			
60 $\Omega$ $\pm$ 15%	5 mils width, 7 mils spacing (based on stackup assumptions in <a href="#">Section 3</a> )	2 Slots W1 = W2 = 0.5 inches, R_IDSEL = 300 to 900 $\Omega$	10 inches	1.0 inch		
		3 Slots W1 = W2 = 0.5 inches, R_IDSEL = 300 to 900 $\Omega$	10 inches	1.0 inch	1.0 inch	
		4 Slots W1 = W2 = 0.5 inches, R_IDSEL = 300 to 900 $\Omega$	10 inches	1.0 inch	1.0 inch	1.0 inch

Figure 109. PCI 33 MHz Clock Layout Example

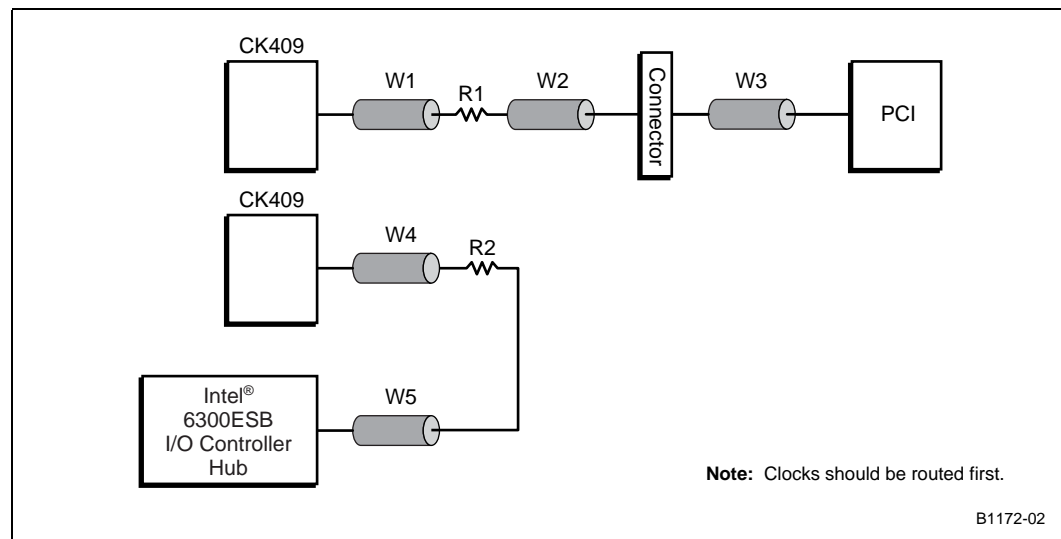


Table 86. PCI 33 MHz Clock Signals Routing Summary

Trace Impedance	PCI Routing Requirements	Topology	Maximum Trace Length	Resistor Values
60 $\Omega$ $\pm$ 15%	5 mils width, 50mils spacing (based on stackup assumptions in <a href="#">Section 3.2</a> )	2 -4 Devices	W1 = 0.5 inches W2 = W5 – 4.5" W3 = 2.5 inches (shown as a reference only) W4 = 0.5 inches W5 = May be as long as needed as long as W2 is scaled accordingly	R1 = 33 $\Omega$ R2 = 33 $\Omega$

### 9.13.2 PIRQ Routing Example

Table 87 shows how the 6300ESB ICH uses the PCI IRQ when the IOAPIC is active.

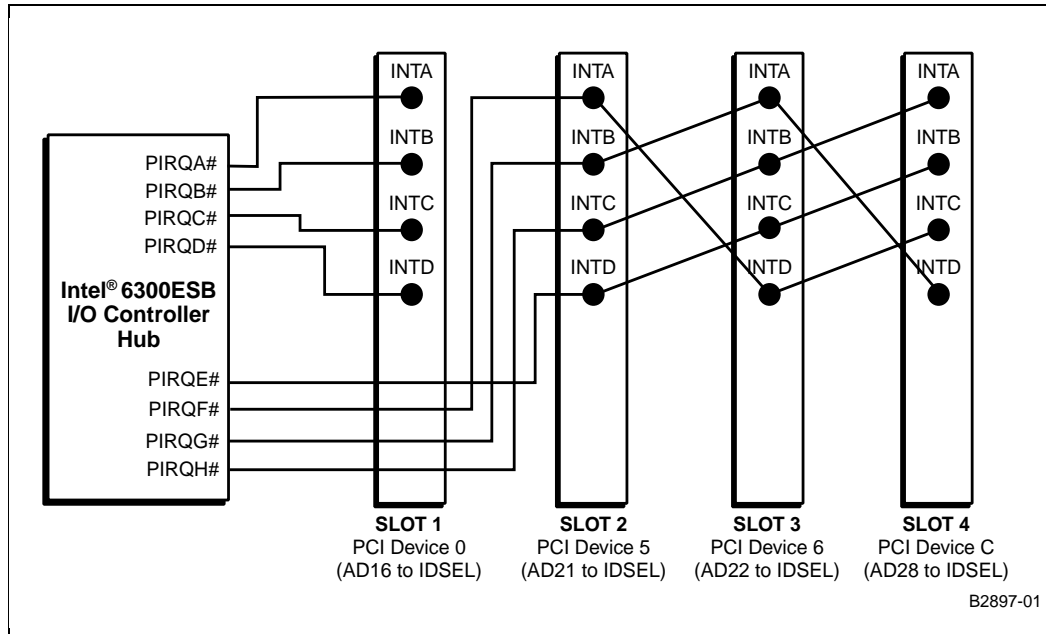
**Table 87. IOAPIC Interrupt Inputs 16 Through 23 Usage**

No	IOAPIC INTIN PIN	Function in 6300ESB ICH using the PCI IRQ in IOAPIC
1	IOAPIC INTIN PIN 16 (PIRQA)	USB UHCI Controller #1
2	IOAPIC INTIN PIN 17 (PIRQB)	AC '97 Audio and Modem; option for SMBus
3	IOAPIC INTIN PIN 18 (PIRQC)	USB UHCI Controller #3; Native mode SATA/IDE
4	IOAPIC INTIN PIN 19 (PIRQD)	USB UHCI Controller #2
5	IOAPIC INTIN PIN 20 (PIRQE)	Option for SCI, TCO, MMT #0,1,2
6	IOAPIC INTIN PIN 21 (PIRQF)	Option for SCI, TCO, MMT #0,1,2
7	IOAPIC INTIN PIN 22 (PIRQG)	Option for SCI, TCO, MMT #0,1,2
8	IOAPIC INTIN PIN 23 (PIRQH)	USB EHCI Controller, Option for SCI, TCO, MMT #0,1,2

Due to different system configurations, IRQ line routing to the PCI slots (swizzling) should be made to minimize the sharing of interrupts between both internal 6300ESB ICH functions and PCI functions. The figure below shows an example of IRQ line routing to the PCI slots

It is not necessarily an optimal routing scheme; an optimal scheme depends on individual system PCI IRQ usage.

**Figure 110. Example PIRQ Routing**



**NOTE:** This figure is an example; it is up to the board designer to route these signals in the most efficient manner for their particular system. A PCI slot can be routed to share interrupts with any of the 6300ESB ICH's internal devices/functions, but at a higher latency cost.



## 9.14 PCI-X Design Guidelines

**Note:** The following guidelines apply to platforms with nominal impedances of  $60\ \Omega \pm 15\%$ .

This section contains guidelines for connecting and routing the 6300ESB ICH PCI-X interface. The 6300ESB ICH supports up to four PCI-X devices. This section provides guidelines for PCI-X connector and motherboard design, including component and resistor placement. When considering PCI-X device configurations refer to [Table 88](#) which shows all the slot/device-down options possible with the 6300ESB ICH PCI-X Interface.

**Table 88. PCI-X Slot/Device Configurations**

PCI-X 1.0 Segment Configurations	# of Slots	# of Devices Down
6 loads, 3 pairs REQ/GNT	3	0
5 loads, 3 pairs REQ/GNT	2	1
6 loads, 4 pairs REQ/GNT	2	2
5 loads, 4 pairs REQ/GNT	1	3
4 loads, 4 pairs REQ/GNT	0	4

**Note:** Bounded by six electrical loads and four REQ/GNT pairs (1 slot = 2 electrical loads)

**Note:** These routing guidelines are created using the stack-up described in [Section 3.2, “Board Stack-Up”](#) on page 34.

The PCI-X interface may be routed with 5 mils traces on 12 mils spaces (dependent upon stackup parameters), and must be less than eight inches long (from 6300ESB ICH to PCI-X connector). Trace spacing of 5 mils is only acceptable when necessary to route through pin fields. For more information, refer to the *PCI-X Specification, Rev 1.0*.

**Table 89. PCI-X Routing Summary**

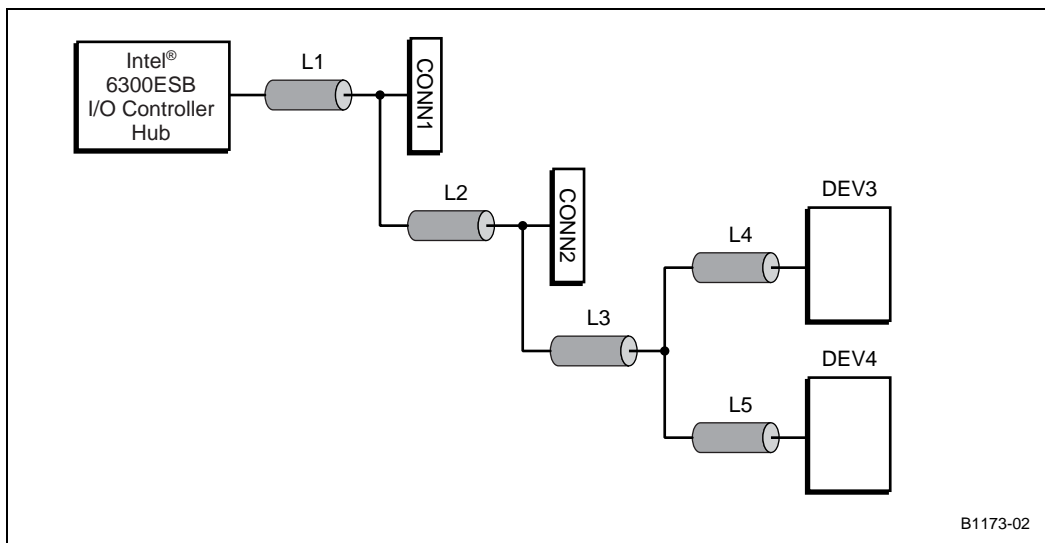
Trace Impedance	PCI-X Routing Requirements	Maximum Trace Length (To First Connector)	Maximum Trace Length Between Connectors	Clock Signal Spacing	PCI-X Signal Length Matching
$60\ \Omega \pm 15\%$	5 mils width, 12 mils spacing (based on stackup assumptions in <a href="#">Section 3.2</a> )	8 inches	1.5 inches	50 mils	Clocks coming from the clock driver must be length matched.

**Table 90. PCI-X Frequencies**

Frequency	Max Slots	Voltage
66 MHz	3	3.3 V

### 9.14.1 66 MHz Topologies and Trace Length

Figure 111. 66 MHz PCI-X, Two Slots, Two Down Devices Configuration

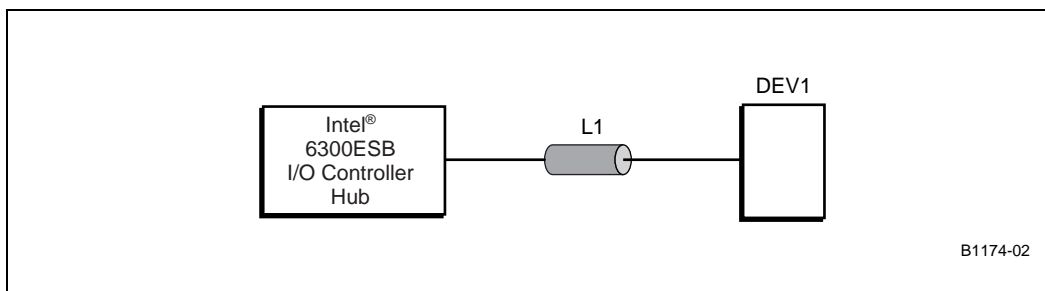


**Note:** For this configuration the recommended pull-up value for the PXPCICAP signal is 8.2 k $\Omega$ .

Table 91. 66 MHz PCI-X, Two Slots, Two Down Devices Routing Length Parameters

Segment	Length [inches]	Total Routing Length
L1	2 – 8.0	33 inches (Including cards 0.75 - 2.75 inches)
L2	1.5 Maximum	
L3	6 Maximum	
L4, L5	8 Maximum	

Figure 112. 66 MHz PCI-X, One Down Device Configuration

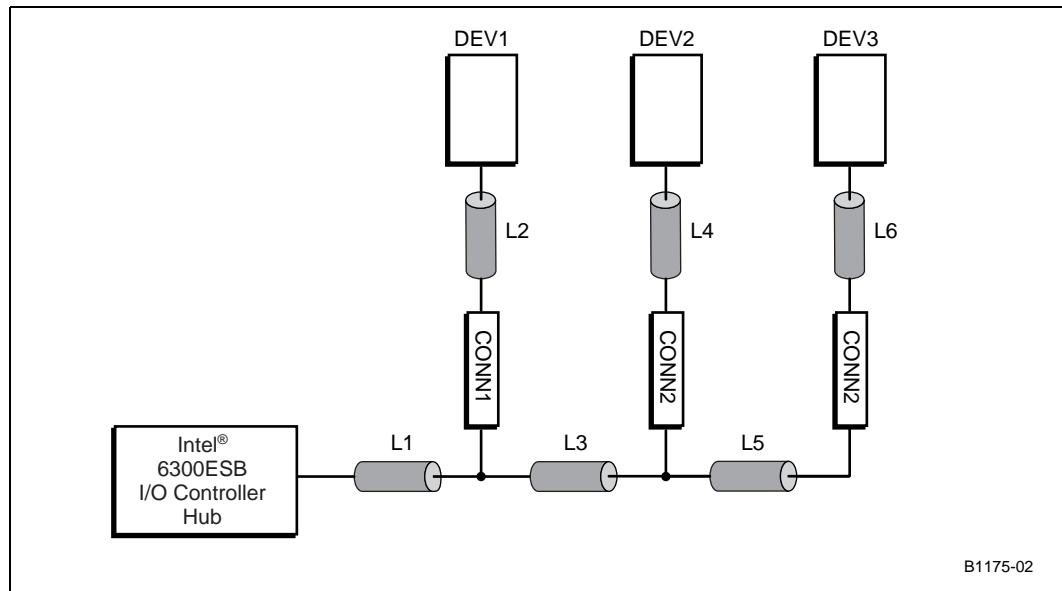


**Note:** For this configuration the recommended pull-up value for the PXPCICAP signal is 8.2 k $\Omega$ .

Table 92. 66 MHz PCI-X, One Down Device Routing Length Parameters

Segment	Length [inches]
L1	2 – 8.0

**Figure 113. 66 MHz PCI-X, Three Slot Configuration**

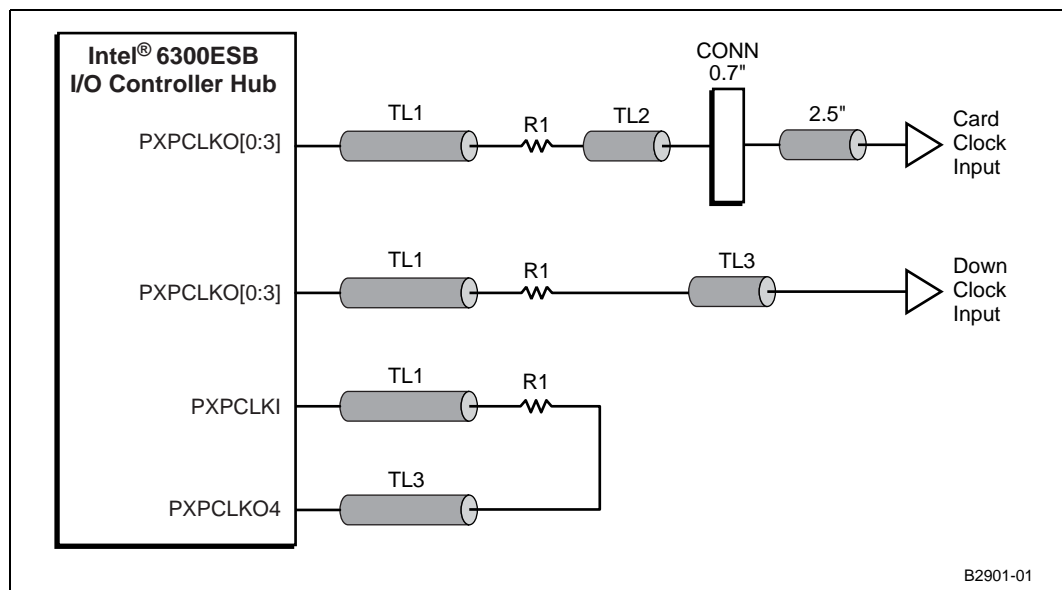


**Note:** For this configuration the recommended pull-up value for the PXPCICAP signal is 4.7 K $\Omega$ .

**Table 93. 66 MHz PCI-X, Three Slot Configuration Routing Length Parameters**

Segment	Length [inches]
L1	2 – 8.0
L3, L5	1.5 Maximum
L2, L4, L6	0.75 – 2.75

**Figure 114. 66 MHz Clock Signal Configuration**



### 9.14.1.1 PCI-X Clock Length Matching Guidelines

The total path length of each clock signal must be matched to all of the other clock lines to ensure that all of the clock edges arrive at the clock inputs of the devices at the same time. [Figure 114](#) above diagrams the general clock layout and the following formulas give the clock matching requirements.

**Note:** Maximum path length of any clock should be kept below 30 inches.

These guidelines account for the fact that there is some delay through the PCI-X mated connector, and through the 2.5 inches of specified trace length for the daughter cards. The PXPCLKI signal is a clock that is fed back to the 6300ESB ICH chip as a timing reference and must be matched to the other clocks.

- The length of the sum of (TL1 + TL2) must be matched to within  $\pm 0.1$  inch between all clocks passing to PCI-X connectors.
- For down devices and the PXPCLKI feedback clock:  $TL1 + TL3 = TL1 + TL2$  (for slots) + 3.2 inches  $\pm 0.1$  inch (the extra 3.2 inches account for the extra delay through the connector and traces of daughter cards).

### 9.14.2 IDSEL Series Resistor

The value for the series resistor on the IDSEL signal should be 100  $\Omega$ . No device is permitted to connect IDSEL to PXAD[16] (device number 0), since this device number is reserved for the source bridge. For systems that have add-in board connectors and connect IDSEL to the PXAD bus, the first two add-in board connectors are recommended to be connected according to [Table 94](#) to minimize the length of the IDSEL trace.

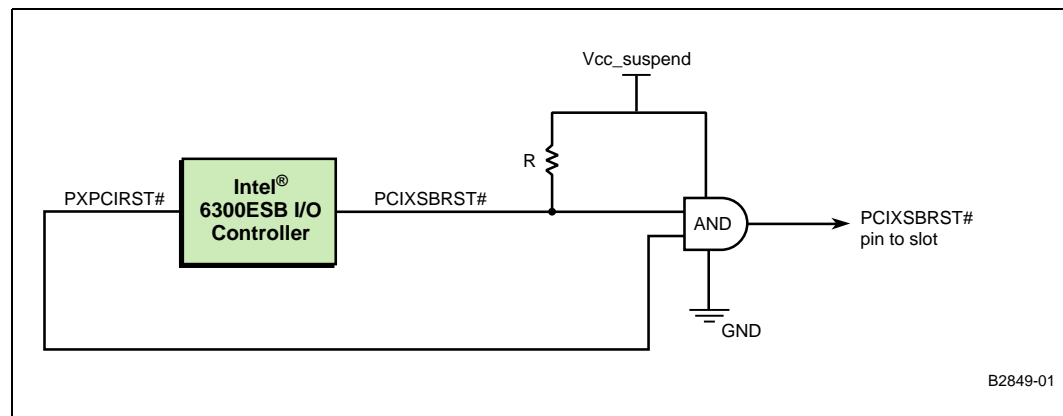
**Table 94. IDSEL to PXAD Bit Assignment**

Slot #	PXAD Bit	Device Number
1	17	1
2	18	2

### 9.14.3 PCI-X Secondary Bus Reset

The Secondary Bus Reset (SBR) function on the 6300ESB ICH enables the user to change the mode and frequency of the PCI-X Bus without resetting the entire system. If this function is not needed in the system design refer to [Section 9.14.3.1](#). When utilizing the SBR function an external circuit is required. Refer to [Figure 115](#) for proper implementation:

**Figure 115. Usage Model for SBR Functionality**



**NOTE:** Recommended pull-up resistor value (R) is 100 K $\Omega$  –200 K $\Omega$

### 9.14.3.1 Secondary Bus Reset Not Utilized

When the SBR function on the 6300ESB ICH is not utilized the following should be considered:

- The SBR pin PCIXSBRST# (Ball AA7) may be left as a No Connect.
- The PCI-X slots should be tied to the system reset logic (PXPCIRST#).

## 9.14.4 PME# Signal Sharing

In many cases the system designer will choose to share the PME# signal between the PCI-X bus and the PCI bus. While this option has been tested, certain considerations must be made when using this configuration.

### 9.14.4.1 Issues with Sharing PME#

Many operating systems recommend that the PME# signal is not shared when designing an optimal system. Refer to your specific operating system for issues that may occur when routing a shared PME# signal.

More information on General Purpose Event (GPE) Register recommendations for Microsoft® Windows® operating systems are available in *GPE Routing for Microsoft Windows* (see [Table 1](#), “Reference Documentation” on page 19).

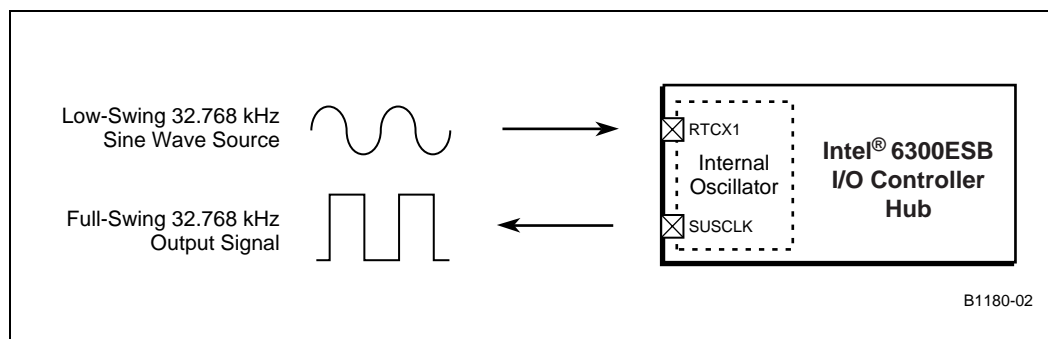
## 9.15 RTC

**Note:** The following guidelines apply to platforms with nominal impedances of 60  $\Omega \pm 15\%$ .

The 6300ESB ICH contains a real time clock (RTC) with 256 bytes of battery backed SRAM. The internal RTC module provides two key functions: keeping date and time and storing system data in its RAM when the system is powered down.

The 6300ESB ICH uses a crystal circuit to generate a low-swing 32 KHz input sine wave. This input is amplified and driven back to the crystal circuit through the RTCX2 signal. Internal to the 6300ESB ICH, the RTCX1 signal is amplified to drive internal logic as well as generate a free-running full-swing clock output for system use. This output ball of the 6300ESB ICH is called SUSCLK. This is illustrated in Figure 116.

**Figure 116. RTCX1 and SUSCLK Relationship in the ICH**

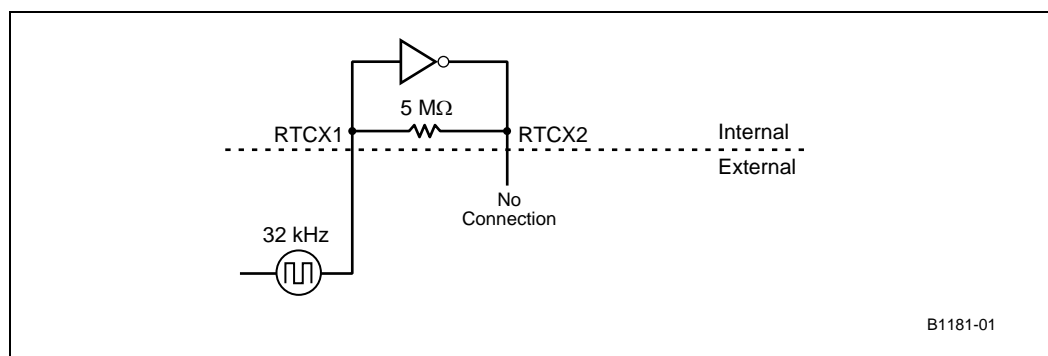


For further information on the RTC, consult the *ICH Family Real Time Clock (RTC) Accuracy and Considerations Under Test Conditions Application Note* (see Table 1, “Reference Documentation” on page 19). This application note is valid for the 6300ESB ICH.

Even when the 6300ESB ICH internal RTC is not used, it is still necessary to supply a clock input to RTCX1 of the platform because other signals are gated off that clock in suspend modes. However, in this case, the frequency accuracy (32.768 KHz) of the clock inputs is not critical; a crystal may be used or a single clock input may be driven into RTCX1 with RTCX2 left as no connect, as shown in Figure 117.

**Note:** This is not a validated feature on 6300ESB ICH. Please note that the peak-to-peak swing on RTCX1 may not exceed 2.0 V.

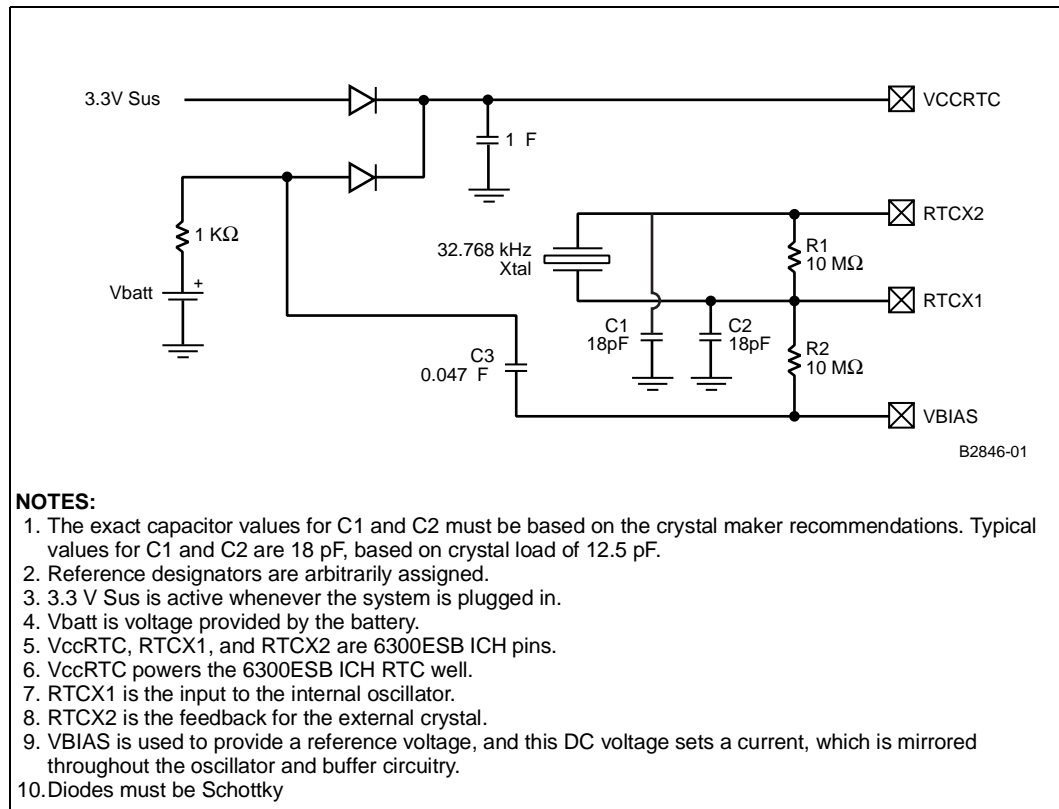
**Figure 117. External Circuitry in the ICH Without Use of Internal RTC**



### 9.15.1 RTC Crystal

The 6300ESB ICH RTC module requires an external oscillating source of 32.768 kHz connected on the RTCX1 and RTCX2 balls. Figure 118 shows the external circuitry that comprises the oscillator of the 6300ESB ICH RTC.

**Figure 118. External Circuitry for the ICH RTC**



**Table 95. RTC Routing Summary**

Trace Impedance	RTC Routing Requirements	Maximum Trace Length To Crystal	Signal Length Matching	R1, R2, C1, and C2 tolerances	Signal Referencing
60 Ω ± 15%	5 mil trace width (results in ~2 pF per inch)	1 inch	NA	R1 = 10M Ω ± 5% C1 = C2 = (NPO class) See <a href="#">Section 9.15.2</a> for calculating a specific capacitance value for C1 and C2.	Ground

## 9.15.2 External Capacitors

To maintain the RTC accuracy, the external capacitor  $C_3$  needs to be 0.047 μF and capacitor values  $C_1$  and  $C_2$  should be chosen to provide the manufacturer's specified load capacitance ( $C_{load}$ ) for the crystal when combined with the parasitic capacitance of the trace, socket (if used), and package. The following equation may be used to choose the external capacitance values:

$$C_{load} = [(C_1 + C_{in1} + C_{trace1}) * (C_2 + C_{in2} + C_{trace2})] / [(C_1 + C_{in1} + C_{trace1} + C_2 + C_{in2} + C_{trace2})] + C_{parasitic}$$

Where:

- $C_{load}$  = Crystal's load capacitance. This value may be obtained from crystal's specification.
- $C_{in1}$ ,  $C_{in2}$  = input capacitances at RTCX1, RTCX2 balls of the 6300ESB ICH. These values may be obtained in the ICH's data sheet.
- $C_{trace1}$ ,  $C_{trace2}$  = Trace length capacitances measured from crystal terminals to RTCX1, RTCX2 balls. These values depend on the characteristics of board material, the width of signal traces and the length of the traces. A typical value, based on a 5 mil wide trace and a 0.5 ounce copper pour, is approximately equal to:
- $C_{trace} = \text{trace length} * 2 \text{ pF/inch}$
- $C_{parasitic}$  = Crystal's parasitic capacitance. This capacitance is created by the exist of two electrode plates and the dielectric constant of the crystal blank inside the crystal part. Refer to the crystal's specification to obtain this value.

Ideally,  $C_1$ ,  $C_2$  may be chosen such that  $C_1 = C_2$ . Using the equation of  $C_{load}$  above, the value of  $C_1$ ,  $C_2$  may be calculated to give the best accuracy (closest to 32.768 kHz) of the RTC circuit at room temperature. However,  $C_2$  may be chosen so that  $C_2 > C_1$ . Then  $C_1$  may be trimmed to obtain the 32.768 kHz.

In certain conditions, both  $C_1$ ,  $C_2$  values may be shifted away from the **theoretical values** (calculated values from the above equation) to obtain the closest oscillation frequency to 32.768 kHz. When  $C_1$ ,  $C_2$  value are smaller than the theoretical values, the RTC oscillation frequency is higher.

The following example illustrates the use of the practical values  $C_1$ ,  $C_2$  in the case that theoretical values may not ensure the accuracy of the RTC in low temperature condition:

#### Example:

According to a required 12 pF load capacitance of a typical crystal that is used with the ICH, the calculated values of  $C_1 = C_2$  is 10 pF at room temperature (25 °C) to yield an 32.768 kHz oscillation.

At 0° C the frequency stability of crystal gives -23 ppm (assumed that the circuit has 0 ppm at 25° C). This makes the RTC circuit oscillate at 32.767246 kHz instead of 32.768 kHz.

When the values of  $C_1$ ,  $C_2$  are chosen to be 6.8 pF instead of 10 pF, the RTC oscillates at higher frequency at room temperature (+23 ppm), but this configuration of  $C_1 / C_2$  makes the circuit oscillate closer to 32.768 kHz at 0° C. The 6.8 pF value of  $C_1$  and 2 is the **practical value**.

**Note:** The temperature dependency of a crystal frequency is a parabolic relationship (ppm/degree square). The effect of changing crystal's frequency when operating at 0 °C (25° below room temperature) is the same when operating at 50° C (25° C above room temperature).

### 9.15.3 RTC Layout Considerations

Since the RTC circuit is very sensitive and requires a highly accurate oscillation, reasonable care must be taken during layout and routing of the RTC circuit. Some recommendations are:

- Reduce trace capacitance by minimizing the RTC trace length. The 6300ESB ICH requires a trace length less than one inch on each branch (from crystal's terminal to RTCXn ball). Routing of the RTC circuit should be kept simple to simplify the trace length measurement and increase accuracy on calculating trace capacitances. Trace capacitance depends on the trace



width and dielectric constant of board's material. On FR406, a 5 mil trace has approximately 2 pF per inch.

- Trace signal coupling must be importantly reduced, by avoiding routing of adjacent PCI signals close to RTCX1 and RTCX2, and VBIAS.
- Ground guard plane is highly recommended.
- The oscillator  $V_{CC}$  should be clean; use a filter, such as an RC low-pass, or a ferrite inductor.

## 9.15.4 RTC External Battery Connection

The RTC requires an external battery connection to maintain its functionality and its RAM while the 6300ESB ICH is not powered by the system.

Example batteries are: Duracell® 2032, 2025, or 2016 (or equivalent). Batteries are rated by storage capacity. The battery life, measured in years, may be calculated by dividing the capacity by the average current required. For example, when the battery storage capacity is 220 mAh (assumed usable) and the average current required is 8.5  $\mu$ A, the battery life will be at least:

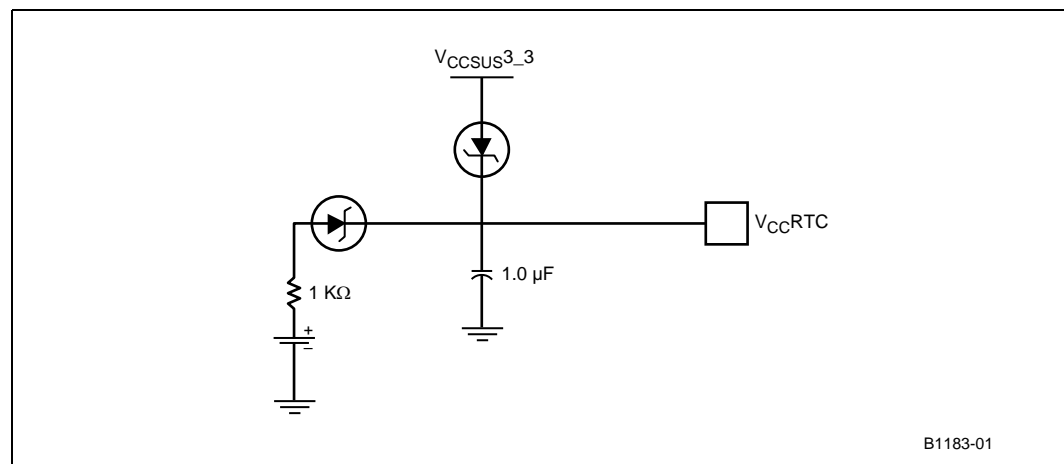
$$\sim 220,000 \mu\text{Ah} / 8.5 \mu\text{A} \cong 26,000\text{h} \cong 3 \text{ years}$$

**Note:** Refer to the *Intel 6300ESB ICH Datasheet* (see [Table 1, “Reference Documentation” on page 19](#)) for actual DC Current Characteristics.

The voltage of the battery may affect the RTC accuracy. In general, when the battery voltage decays, the RTC accuracy also decreases. High accuracy may be obtained when the RTC voltage is in the range of 3.0 V to 3.3 V.

The battery must be connected to the 6300ESB ICH through an isolation Schottky diode circuit. The Schottky diode circuit allows the 6300ESB ICH RTC-well to be powered by the battery when the system power is not available, but by the system power when it is available. To do this, the diodes are set to be reverse biased when the system power is not available. [Figure 119](#) is an example of a diode circuit that is used.

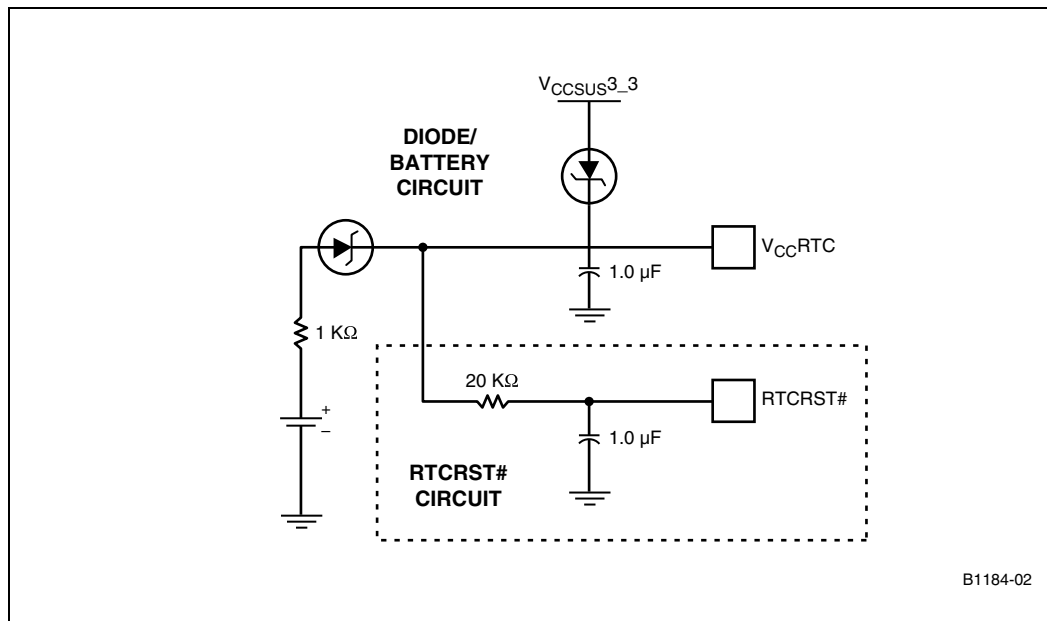
**Figure 119. Diode Circuit to Connect RTC External Battery**



A standby power supply should be used in a desktop system to provide continuous power to the RTC when available, which increases the RTC battery life and thereby the RTC accuracy.

### 9.15.5 RTC External RTCRST# Circuit

Figure 120. RTCRST# External Circuit for the ICH RTC



The 6300ESB ICH RTC requires some additional external circuitry. The RTCRST# signal is used to reset the RTC well. The external capacitor and the external resistor between RTCRST# and the RTC battery (VBAT) were selected to create an RC time delay, such that RTCRST# will go high some time after the battery voltage is valid. The RC time delay should be in the range of 18-25 ms. When RTCRST# is asserted, bit 2 (RTC\_PWR\_STS) in the GEN\_PMCON\_3 (General PM Configuration 3) register is set to 1, and remains set until software clears it. As a result of this, when the system boots, the BIOS knows that the RTC battery has been removed.

The RTCRST# signal may also be used to detect a low battery voltage. RTCRST# will be asserted during a power up from G3 state if the battery voltage is below 2 V. This sets the RTC\_PWR\_STS bit as described above. When desired, BIOS may request that the user replace the battery.

This RTCRST# circuit is combined with the diode circuit (shown in Figure 119) to allow the RTC well to be powered by the battery when the system power is not available. Figure 120 is an example of this circuitry that is used in conjunction with the external diode circuit.

### 9.15.6 V<sub>BIAS</sub> DC Voltage and Noise Measurements

V<sub>BIAS</sub> is a DC voltage level necessary for biasing the RTC oscillator circuit. This DC voltage level is filtered out from the RTC oscillation signal by the RC Network of R2 and C3 (see Figure 118); therefore, it is a self-adjusted voltage. Board designers should not manually bias the voltage level on V<sub>BIAS</sub>. Checking V<sub>BIAS</sub> level is used for testing purposes only to determine the right bias condition of the RTC circuit.

V<sub>BIAS</sub> should be at least 200 mV DC. The RC network of R2 and C3 will filter out most of AC signal that exist on this ball. However, the noise on this ball should be kept minimal in order to ensure the stability of the RTC oscillation.

Probing  $V_{BIAS}$  requires the same technique as probing the RTCX1, RTCX2 signals (using Op-Amp). Refer to the *Intel ICH Family Real Time Clock (RTC) Accuracy and Considerations under Test Conditions Application Note* for further details on measuring techniques.

**Note:**  $V_{BIAS}$  is also very sensitive to environmental conditions.

## 9.15.7 SUSCLK

SUSCLK is a square waveform signal output from the RTC oscillation circuit. Depending on the quality of the oscillation signal on RTCX1 (largest voltage swing), the SUSCLK duty cycle may be between 30-70%. When the SUSCLK duty cycle is beyond 30-70% range, it indicates a poor oscillation signal on RTCX1 and RTCX2.

SUSCLK may be probed directly using normal probe (50  $\Omega$  input impedance probe). It is an appropriated signal you may use to check the RTC frequency to determine the accuracy of the 6300ESB ICH's RTC Clock (see *Intel ICH Family Real Time Clock (RTC) Accuracy and Considerations under Test Conditions Application Note* for further details).

## 9.15.8 RTC-Well Input Strap Requirements

All RTC-well inputs (RSMRST#, RTCRST#, INTRUDER#) must be either pulled up to  $V_{CCRTC}$  or pulled down to ground while in G3 state. RTCRST# when configured as shown in [Figure 120](#) meets this requirement. RSMRST# should have a weak external pull-down to ground and INTRUDER# should have a weak external pull-up to  $V_{CCRTC}$ . This prevents these nodes from floating in G3, and correspondingly prevents  $I_{CCRTC}$  leakage that may cause excessive coin-cell drain. The PWROK input signal should also be configured with an external weak pull-down.

## 9.16 Serial I/O

The 6300ESB ICH supports two serial I/O ports. For proper functionality of the serial I/O ports ensure the clock input (UART\_CLK) has the correct value.

System designers have two options for the input clock:

- 48 MHz (recommended)
- 14.745 MHz

**Warning:** If using the 14.745 MHz option, ensure it is 14.745 MHz. Any deviation from this value, such as using a common system clock (14.318 MHz), will cause improper functioning of the serial I/O.

**Note:** A 48 MHz clock input is the recommended value to ease system design. A CK409 has an 48 MHz clock available so no other clock source for the serial I/O would be necessary.

### 9.16.1 Serial I/O Interface Not Utilized

When the serial I/O is not utilized in the system, all associated pins may be left as No Connect.

**Note:** SIU\_DTR# is a strap pin. To utilize the strap feature (TOP Swap) a pull-down to ground is necessary. Refer to the *Intel 6300ESB ICH Datasheet* for more details.

# General Purpose I/O

# 10

## 10.1 GPIO Summary

The 6300ESB ICH platform has 12 general purpose inputs, 9 general purpose outputs, and 16 general purpose inputs/outputs.

**Table 96. GPIO Summary (Sheet 1 of 2)**

GPIO Number	Power Well	Input-Output	Tolerance	If Not Used
0	Core	Input	3.3 V	Recommend an 8.2 K $\Omega$ pull-up resistor to V <sub>CC</sub> 3.3.
1	Core	Input	3.3 V	
2	Core	Input	5 V	Recommend an 8.2 K $\Omega$ pull-up resistor to V <sub>CC</sub> 3.3 or a 2.7 K $\Omega$ pull-up resistor to V <sub>CC</sub> 5.
3	Core	Input	5 V	
4	Core	Input	5 V	
5	Core	Input	5 V	
6	Core	Input	3.3 V	Recommend an 8.2 K $\Omega$ pull-up resistor to V <sub>CC</sub> 3.3.
7	Core	Input	3.3 V	
8	Resume	Input	3.3 V	Recommend an 8.2 K $\Omega$ pull-up resistor to V <sub>CC</sub> Sus3.3.
11	Resume	Input	3.3 V	
12	Resume	Input	3.3 V	
13	Resume	Input	3.3 V	
16	Core	Output	3.3 V	May leave as no connect.
17	Core	Output	3.3 V	
18	Core	Output	5 V	
19	Core	Output	5 V	
20	Core	Output	5 V	
21	Core	Output	5 V	
23	Core	Output	5 V	
24	Resume	Input-Output <sup>†</sup>	3.3 V	
25	Resume	Input-Output <sup>†</sup>	3.3 V	
27	Resume	Input-Output <sup>†</sup>	3.3 V	
28	Resume	Input-Output <sup>†</sup>	3.3 V	
32	Core	Input-Output <sup>†</sup>	3.3 V	
33	Core	Input-Output <sup>†</sup>	3.3 V	
34	Core	Input-Output <sup>†</sup>	3.3 V	
35	Core	Input-Output <sup>†</sup>	3.3 V	
36	Core	Input-Output <sup>†</sup>	3.3 V	

**Table 96. GPIO Summary (Sheet 2 of 2)**

GPIO Number	Power Well	Input-Output	Tolerance	If Not Used
37	Core	Input-Output <sup>†</sup>	3.3 V	May leave as no connect.
38	Core	Input-Output <sup>†</sup>	3.3 V	
39	Core	Input-Output <sup>†</sup>	3.3 V	
40	Core	Input-Output <sup>†</sup>	3.3 V	
41	Core	Input-Output <sup>†</sup>	3.3 V	
42	Core	Input-Output <sup>†</sup>	3.3 V	
43	Core	Input-Output <sup>†</sup>	3.3 V	
56	RTC	Output	3.3 V	
57	RTC	Output	3.3 V	

<sup>†</sup> Defaults as an Output to the 6300ESB ICH.

# Intel® 6300ESB ICH Power Management

11

## 11.1 SYS\_RESET# Usage Model

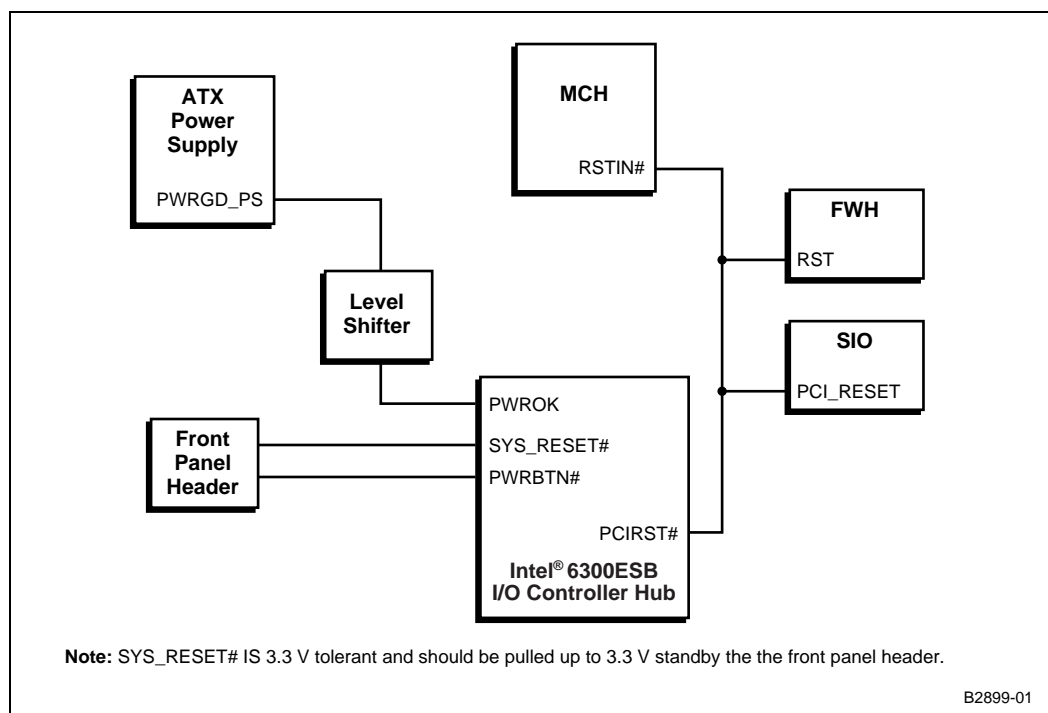
The System Reset ball (SYS\_RESET#) on the 6300ESB ICH may be connected directly to the reset button on the system front panel, provided that the front panel header pulls this signal up to 3.3 V standby through a weak pull-up resistor. The 6300ESB ICH will debounce signals on this pin (16 ms) and allow the SMBus to go idle before resetting the system. This helps to prevent a slave device on the SMBus from hanging by resetting in the middle of a cycle.

**Note:** The PWORK signal should not be used to implement front panel reset.

## 11.2 PWRBTN# Usage Model

The Power Button ball (PWRBTN#) on the 6300ESB ICH may be connected directly to the power button on the system front panel. This signal is internally pulled-up in the 6300ESB ICH to 3.3 V standby through a pull-up resistor (24 K $\Omega$  nominal). The 6300ESB ICH has 16 ms of internal debounce logic on this pin.

**Figure 121. SYS\_RESET# and PWRBTN# Connection**

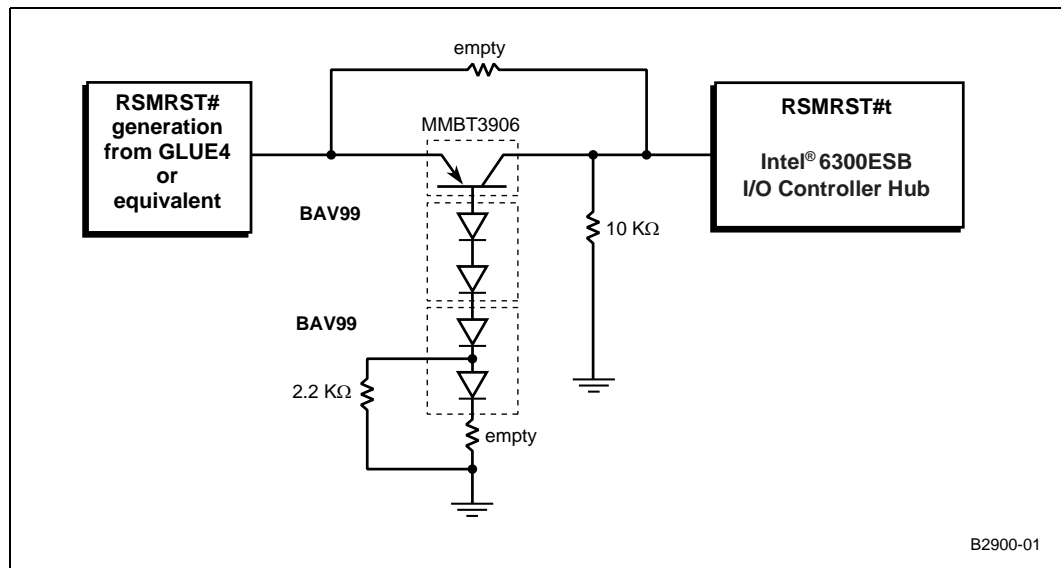


## 11.3 Power-Well Isolation Control Strap Requirements

**Note:** The RSMRST# signal of the 6300ESB ICH must transition from 20% signal level to 80% signal level and vice-versa within 50 uS.

The circuit shown in Figure 122 may be implemented to control well isolation between the VccSUS3.3 and RTC power-wells in the event that RSMRST# is not being actively asserted during the discharge of the standby rail. Failure to implement this circuit or a circuit that functions similar to this may result in excessive droop on the VCCRTC node during Sx-to-G3 power state transitions (removal of AC power). Droop on this node may potentially cause the CMOS to be cleared or corrupted, the RTC to lose time after several AC power cycles, or the intruder bit might assert erroneously.

**Figure 122. RTC Power Well Isolation Control**



# FWH Guidelines

# 12

The following provides general guidelines for compatibility and design recommendations for supporting the firmware hub (FWH) device. Refer to the *FWH BIOS Specification* or equivalent.

## 12.1 FWH Vendors

The following vendors manufacture firmware hubs that conform to the *Intel FWH Specification*. Contact the vendor directly for information on packaging and density.

- SST\*: <http://www.sst.com>
- STMicroelectronics\*: <http://www.st.com>
- Atmel\*: <http://www.atmel.com>

## 12.2 FWH Decoupling

A 0.1  $\mu$ F capacitor should be placed between the  $V_{CC}$  supply pins and the  $V_{SS}$  ground pins to decouple high frequency noise, which may affect the programmability of the device. Additionally, a 4.7  $\mu$ F capacitor should be placed between the  $V_{CC}$  supply pins and the  $V_{SS}$  ground pins to decouple low frequency noise. The capacitors should be placed no further than 390 mils from the  $V_{CC}$  supply pins.

## 12.3 In-circuit FWH Programming

All cycles destined for the FWH appear on PCI. The 6300ESB ICH Hub Interface to PCI Bridge places all CPU boot cycles out on PCI (before sending them out on the FWH interface). When the 6300ESB ICH is set for subtractive decode, these boot cycles may be accepted by a positive decode agent on the PCI bus. This enables the ability to boot from a PCI card that positively decodes these memory cycles. In order to boot from a PCI card, it is necessary to keep the 6300ESB ICH in subtractive decode mode. When a PCI boot card is inserted and the 6300ESB ICH is programmed for positive decode, there are two devices positively decoding the same cycle.

## 12.4 FWH INIT# Voltage Compatibility

The FWH INIT# signal trip points need to be considered because they are NOT consistent among different FWH manufacturers. The INIT# signal is active low. Therefore, the inactive state of the 6300ESB ICH INIT# signal needs to be at a value slightly higher than the  $V_{IH}$  min FWH INIT# pin specification. The 6300ESB ICH inactive state of this signal is typically governed by the formula:

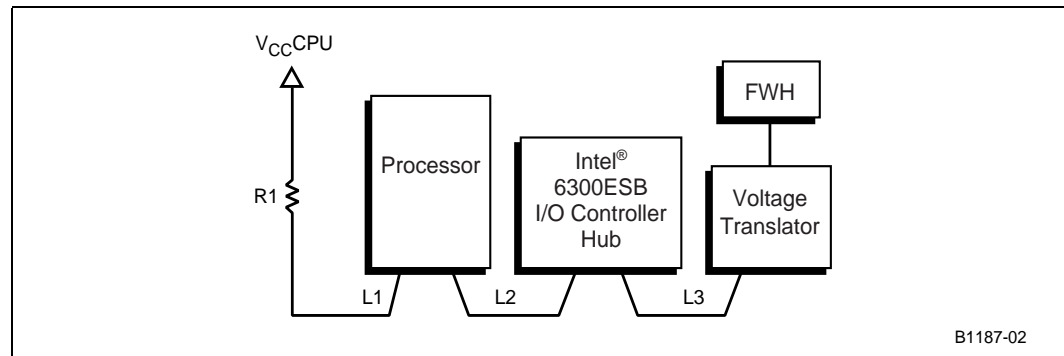
$$V_{CPU\_IO} \text{ min} - \text{noise margin} \geq V_{IH} \text{ min}$$



Therefore, if the  $V_{\text{CPU\_IO min}}$  of the processor is 1.6 V, the noise margin is 200 mV and the  $V_{\text{IH min}}$  spec of the FWH INIT# input signal is 1.35 V, there would be no compatibility issue because  $1.6 \text{ V} - 0.2 \text{ V} = 1.40 \text{ V}$  which is greater than the 1.35 V minimum of the FWH. If the  $V_{\text{IH min}}$  of the FWH was 1.45 V, then there would be an incompatibility and level translation would need to be used. These examples do not take into account actual noise that may be encountered on INIT#. Care must be taken to ensure that the  $V_{\text{IH min}}$  specification is met with ample noise margin.

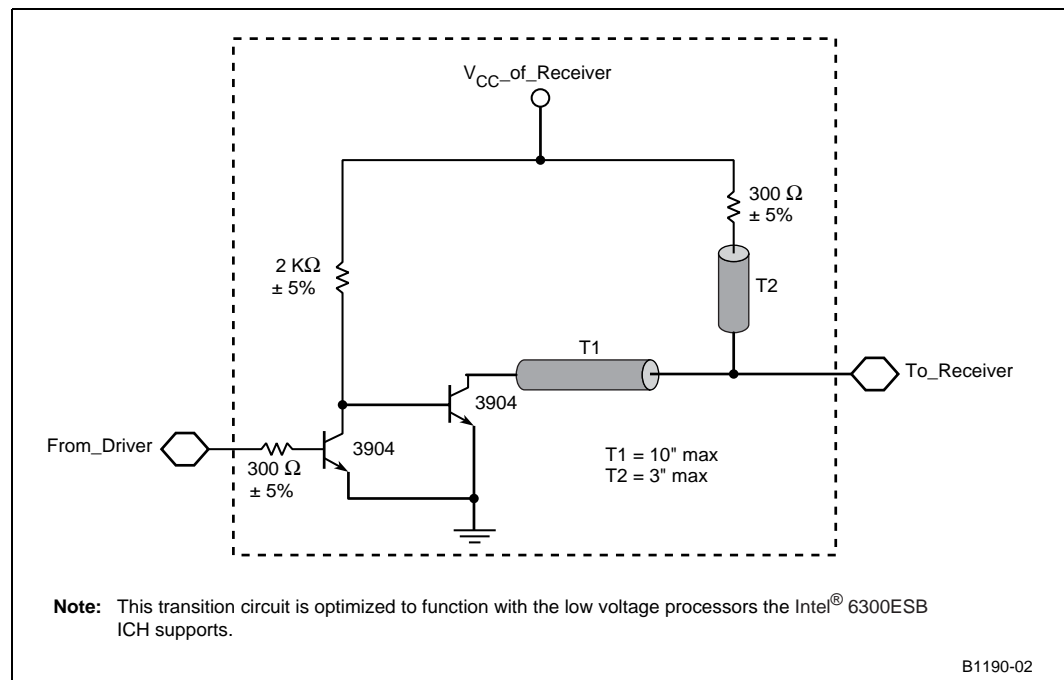
The following solutions assume that level translation is necessary. The figure below implements the INIT# signal UP (Figure 123) topology solution for the 6300ESB ICH, FWH and the CPU. The level translator circuitry is shown in Figure 124.

**Figure 123. FWH/CPU UP Signal Topology Solution**



**NOTE:** The recommended value for R1 depends on the processor used in the system. See the processor design guidelines for more info.

**Figure 124. FWH Level Translation Circuitry**

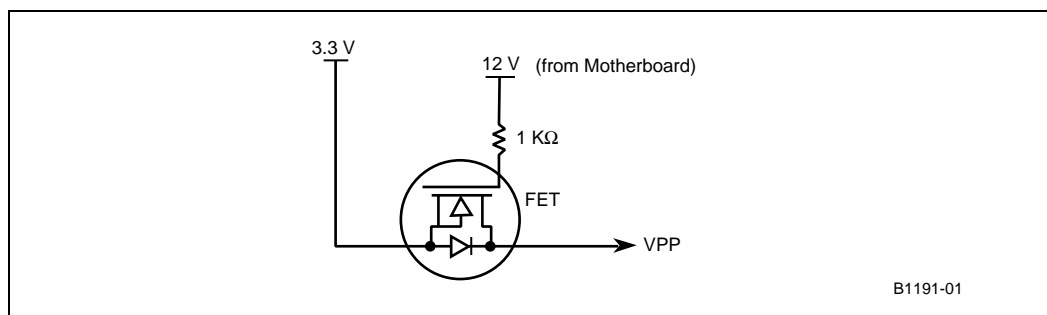


## 12.5 FWH $V_{PP}$ Design Guidelines

The  $V_{PP}$  pin on the FWH is used for programming the flash cells. The FWH supports  $V_{PP}$  of 3.3 V or 12 V. When  $V_{PP}$  is 12 V, the flash cells programs about 50% faster than at 3.3 V. However, the FWH only supports 12 V  $V_{PP}$  for 80 hours (3.3 V on  $V_{PP}$  does not affect the life of the device). The 12 V  $V_{PP}$  would be useful in a programmer environment, which is typically an event that occurs very infrequently (much less than 80 hours). The  $V_{PP}$  pin **MUST** be tied to 3.3 V on the motherboard. (See [Figure 125](#).)

In some instances, it is desirable to program the FWH during assembly with the device soldered down on the board. In order to decrease programming time it becomes necessary to apply 12 V to the  $V_{PP}$  pin. The following circuit will allow testers to put 12 V on the  $V_{PP}$  pin while keeping this voltage separated from the 3.3 V plane to which the rest of the power pins are connected. This circuit also allows the board to operate with 3.3 V on this pin during normal operation.

**Figure 125. FWH  $V_{PP}$  Isolation Circuitry**



# Power Distribution Guidelines

# 13

This section addresses power delivery recommendation for the 875P MCH/E7210 MCH/6300ESB ICH Customer Reference Board. These guidelines allow support for both the Pentium 4 and Pentium 4 with HT Technology<sup>†</sup> processors.

## 13.1 Terminology and Definitions

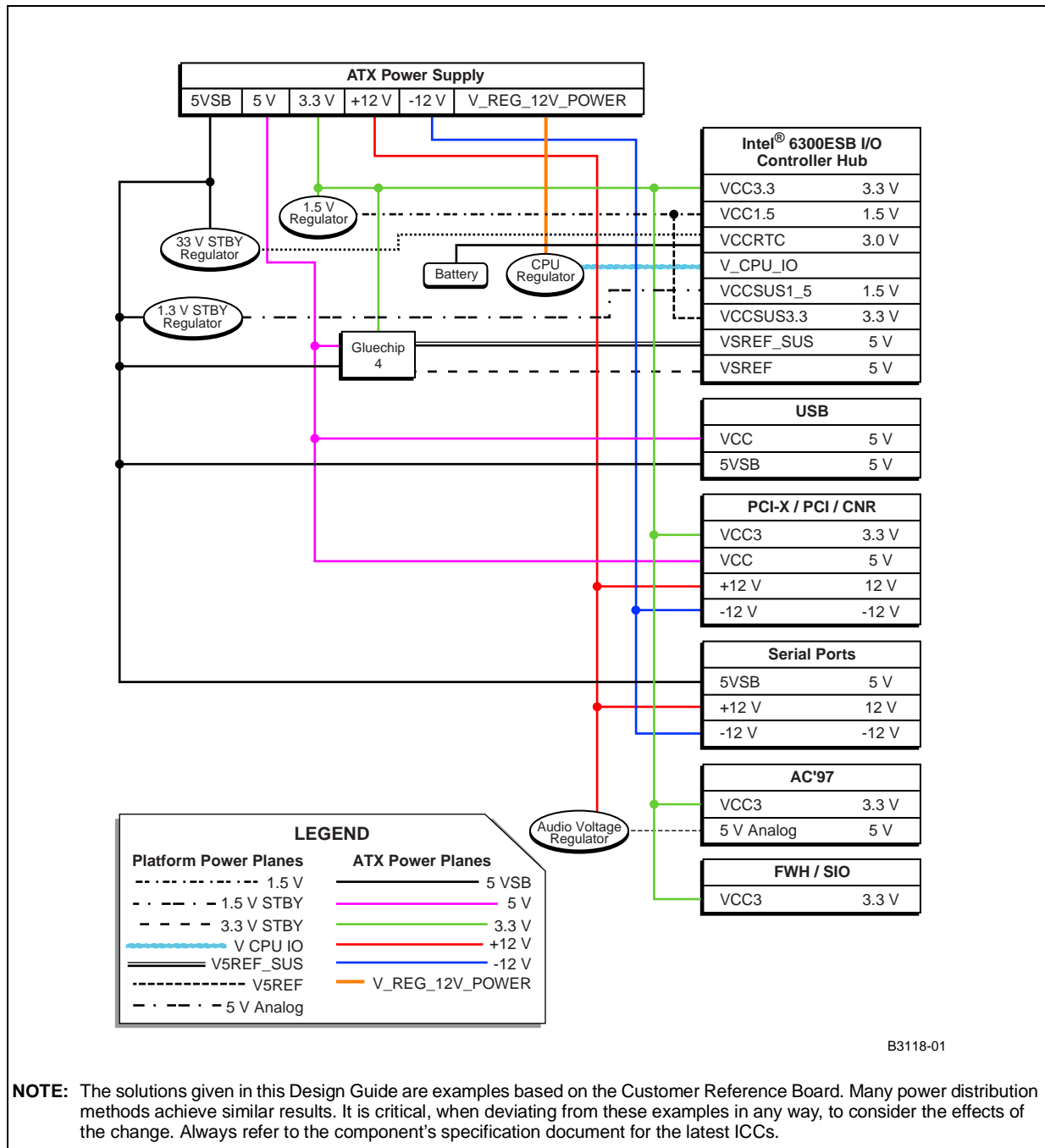
<b>Suspend-To-RAM (STR)</b>	In the STR state, the system state is stored in main memory and all unnecessary system logic is turned off. Only main memory and logic required to wake the system remain powered. This state is used in the Customer Reference Board to satisfy the S3 ACPI power management state.
<b>Full-Power</b>	During full-power operation, all components on the motherboard remain powered. Note that full-power operation includes both the full-on operating state and the S1 (CPU stop-grant state) state.
<b>Suspend Operation</b>	During suspend operation, power is removed from some components on the motherboard. The customer reference board supports two suspend states: Suspend-to-RAM (S3) and Soft-Off (S5).
<b>Power Rails</b>	An ATX power supply has six power rails: +12 V, -12 V, +5 V, +3.3 V, and +5 VSB. In addition to these power rails coming off the power supply, several other power rails are created by voltage regulators on the 875P MCH/E7210 MCH/6300ESB ICH Customer Reference Board.
<b>Core Power</b>	A power rail that is only on during full-power operation. These power rails are turned on when the PS_ON signal is asserted to the ATX power supply. The core power rails that are distributed directly from the ATX power supply are: $\pm 5$ V, $\pm 12$ V and +3.3 V.
<b>Standby Power Rail</b>	A power rail that is on during suspend operation (these rails are also on during full power operation) is a standby power rail. These rails are on at all times as soon as the power supply is plugged into AC power. The only standby power rail that is distributed directly from the ATX power supply is 5 V SB. The other standby rails on the motherboard are created by voltage regulators.
<b>Derived Power</b>	A derived power rail is any power rail that is generated from another power rail using an on-board voltage regulator. For example, +2.6 V may be derived from a +5 V power rail using a voltage regulator.
<b>Dual Power Rail</b>	A dual power rail is derived from different rails at different times (depending on the power state of the system). Usually, a dual power rail is derived from standby supply during suspend operation and derived from a core supply during full-power operation.
<b>VRM and VRD</b>	Voltage Regulator Module and Voltage Regulator Down. The VRD is what the 875P MCH/E7210 MCH/6300ESB ICH Customer Reference Board has implemented for the processor voltage regulator.

## 13.2 Customer Reference Board Power Delivery

Figure 126 shows the power delivery architecture for the 6300ESB ICH. This power delivery architecture supports the “Instantly Available PC Design Guidelines” via the suspend-to-RAM (STR) state.

During STR, only the necessary devices are powered. These devices include main memory, the 6300ESB ICH resume well, PCI wake devices (via 3.3 VAUX), and USB (USB may be powered only if sufficient standby power is available). To insure that enough power is available during STR, a thorough power budget should be completed. The power requirements should include each device’s power requirements, both in suspend and in full power modes. The power requirements should be compared with the power budget supplied by the power supply. Due to the requirements of main memory, the PCI 3.3 VAUX (and possibly other devices in the system), it is necessary to create a **dual** power rail.

Figure 126. ICH Power Delivery Map



B3118-01

### 13.2.1 VCC— Core Power to CPU

The VCC power plane to the CPU is used to power the processor core. The processor's voltage regulator must be compatible with either a VRM 10 or a VRD 10.0 design. Refer to the *VRM 9.0 DC-DC Converter Design Guidelines* or *Voltage Regulator-Down (VRD) 10.0 Design Guidelines* and the associated addendum for more information. This is required for all designs.

### 13.2.2 VTT— Power to MCH

The VTT power plane powers the MCH's FSB interface. It is important that the VTT plane be separate from the CPU's core power plane. When a Pentium 4 processor with HT Technology is inserted into the platform, the output of the MCH's VTT regulator should be set to 1.225 V, and if a Pentium 4 processor is inserted into the platform, the output of the MCH's VTT regulator should be set to 1.45 V. This regulator must be able to source 2 A and sink 600 mA in normal operation.

The power up/down timing requirements for the MCH's VTT regulator is that it must come up after or at the same time as the CPU core voltage and power down before or at the same time as the CPU core. The BOOTSELECT pin from the CPU socket is used to switch the output voltage on the regulator. At a minimum, the regulator should have tolerance of  $\pm 7\%$ , but  $\pm 5\%$  is preferred.

### 13.2.3 VCCVID— CPU VID

VCCVID is a 1.2 V power plane is used to power pins AF4 and AF3 on the processor. It is derived from 3.3 V and should be able to source 150 mA of current. This regulator is required for all designs.

### 13.2.4 2.55 V Dual— DDR CORE

The 2.55 V dual power plane is used to provide power to the DDR DRAM core, the MCH DDR I/O ring, reference voltage to the 1.275 V linear regulator, and the 2.55 V to 1.5 V linear regulator. The 2.55 V power plane is created using a switch between a switching regulator and a linear stand-by regulator. The switching regulator should be able to support up to 19.25 A of current while the stand-by regulator needs only to supply 500 mA of current. The switching regulator receives its input directly from the 5 V power rail of the power supply while the linear regulator receives its input from 5 VSB. The DDR DRAM VDD and VDDQ requires at most 13 A of current in the S1 state. This value is a worst-case current, and is based on DRAM vendor specific specification for maximum current. The power may be delivered a couple of different ways, one using two regulators, one for each channel, or one regulator for both channels. The current dedicated for the 875P MCH/E7210 MCH's VCCDDR is 4.9 A. This regulator is required in all designs.

### 13.2.5 1.275 V— DDR Termination Voltage

The 1.275 V voltage regulator is for the DDR termination voltage (DDR\_TERM). A linear regulator divides the 2.55 V power rail by 2 to drive a 1.275 V reference voltage. This provides some common mode noise rejection between the DDR termination and I/O voltages. The entire power plane requires 1.8 A of current, and may be delivered a couple of different ways. One way is to use two regulators, one for each channel or one regulator for both channels. This is required for all designs.

### 13.2.6 1.5 V— VCC for MCH Core, HI, AGP, ICH HI, and AGP Connector

The 1.5 V power plane is created using a dual linear regulator sourcing from the 2.55 V power rail. The 1.5 V plane powers the 6300ESB ICH core logic and HI, the MCH core, HI, CSA, AGP, and the AGP Connector. Sequencing on this rail should ensure that the 1.5 V power plane is shut off during S3. This voltage rail requires approximately 6.6 A maximum current. This regulator is required in all designs.

### 13.2.7 5 V Dual

This rail will be powered from the +5 V ATX rail from the power supply during full-power operation and from 5 VSB during S3 or *Suspend To Ram* (STR). There is a resistive drop through the 5 V dual Switch that must be considered. Therefore, **no components** should be connected directly to the 5 V dual plane. On the 875P MCH/E7210 MCH/6300ESB ICH Customer Reference Board, voltage regulators are the only devices on the 5 V dual rail.

**Note:** The voltage on the 5 V dual plane is not 5 V due to the resistive drop.

**Note:** This switch is not required in an 6300ESB ICH chipset-based system that does not support STR.

### 13.2.8 5 V SB (Standby)

The 5 V SB power plane comes directly off the 5 V SB power rail from the ATX power supply and has two functions. One is to provide power to resume functions via a 3.3 V SB regulator for I/O devices off of the 6300ESB ICH. The second is to provide 2.55 V power to the memory devices during the S3 state. The 6300ESB ICH requires 3.3 V SB only due to the integrated 1.275 V SB regulator. It is recommended that the ATX power supply be capable of handling 2 A of SB current.

### 13.2.9 3.3 V SB (Standby)

The 3.3 V SB power plane is the output of a 5 V SB-to-3.3 V SB voltage regulator. The 3.3 V SB plane powers the resume well of the 6300ESB ICH and the PCI 3.3 VAUX suspend power pins. The 3.3 VAUX requirements state that during suspend, the system must deliver 375 mA to each wake-enabled card and 20 mA to each non-wake enabled card. During full-power operation, the system must be able to supply 375 mA to **each** card. Therefore, the total current requirement is:

Full-power Operation:  $375 \text{ mA} * (\text{number of PCI slots})$   
Suspend Operation:  $375 \text{ mA} + 20 \text{ mA} * (\text{number of PCI slots} - 1)$

In addition to the PCI 3.3 VAUX, the 6300ESB ICH suspend well power requirements must be considered. This regulator is required for all designs.

The 1.5 V Standby regulator should be used to power the resume well of the 6300ESB ICH. The VCCSUS1\_5 pins are grouped into three sets of signals: VCCSUS1\_5\_A, VCCSUS1\_5\_B, and VCCSUS1\_5\_C. Each group needs to be independently connected to its corresponding decoupling capacitor for optimum noise isolation. Only one decoupling capacitor is needed per VCCSUS1\_5 signal pin.

**Note:** Do not connect the three sets of VCCSUS1\_5 signal groups together on the 6300ESB ICH.

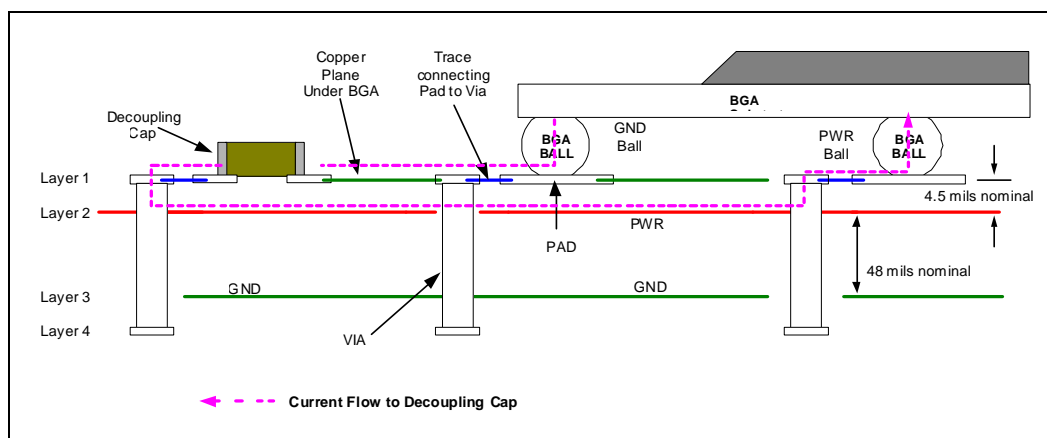
### 13.2.10 2.55 V SB (Standby)

The 2.55 V SB power plane is the output of the 5 V SB-to-2.55 V SB voltage regulator. The power plane is used solely for the DDR DIMMs during the S3 suspend state (some minimal 2.55 V rail current will also be supplied to the MCH). The suspend voltage regulator for system memory is controlled by the LATCHED\_BACKFEED\_CUT signal. This signal should be generated using the SLP\_S4# signal from the 6300ESB ICH, rather than the SLP\_S5# signal, even if the platform does not support the S4 Sleep state. The SLP\_S4# logic in the 6300ESB ICH ensures that system memory will be properly initialized when returning from S4 and S5 states (note that the LATCHED\_BACKFEED\_CUT signal is also derived from the SLP\_S3# and PS\_PWRGD signals, so as not to cause potential confusion). This regulator must be capable of sourcing 550 mA and is required for all designs. The 550 mA comes from 250 mA for the MCH; 107 for VREF, RCOMP, VOL, and VOH circuitry; and 192 mA for the DRAM devices (64 devices for a fully-loaded system at 3 mA each).

## 13.3 Component Power Delivery Guidelines

Large current swings cause the component voltage rails to drop below specified limits. To avoid this type of situation, ensure that the appropriate amount of bulk capacitance is added in parallel to the voltage input pins. The capacitors should be placed as close to the package as possible and rotated such that they sit over power planes. This orientation minimizes the loop inductance (see Figure 127). The basic theory for minimizing loop inductance is to consider which voltage is on layer two (power or ground) and spin the decoupling capacitor with the opposite voltage towards the BGA (ball grid array). This greatly minimizes the total loop inductance. It is recommended that for prototype board designs the designer include pads for extra power plane decoupling capacitors.

**Figure 127. Minimized Loop Inductance Example**





## 13.3.1 Processor Power Delivery Guidelines

### 13.3.1.1 Processor Power Requirements

For the processor system board design, Intel recommends using a regulator compliant with the *Voltage Regulator-Down (VRD) 10.0 Design Guidelines* and addendum. The system board designer should properly place high-frequency and bulk-decoupling capacitors as needed between the voltage regulator and processor to ensure the voltage fluctuations remain within the processor's datasheets. See [Table 97](#) for recommendations on the amount of decoupling needed.

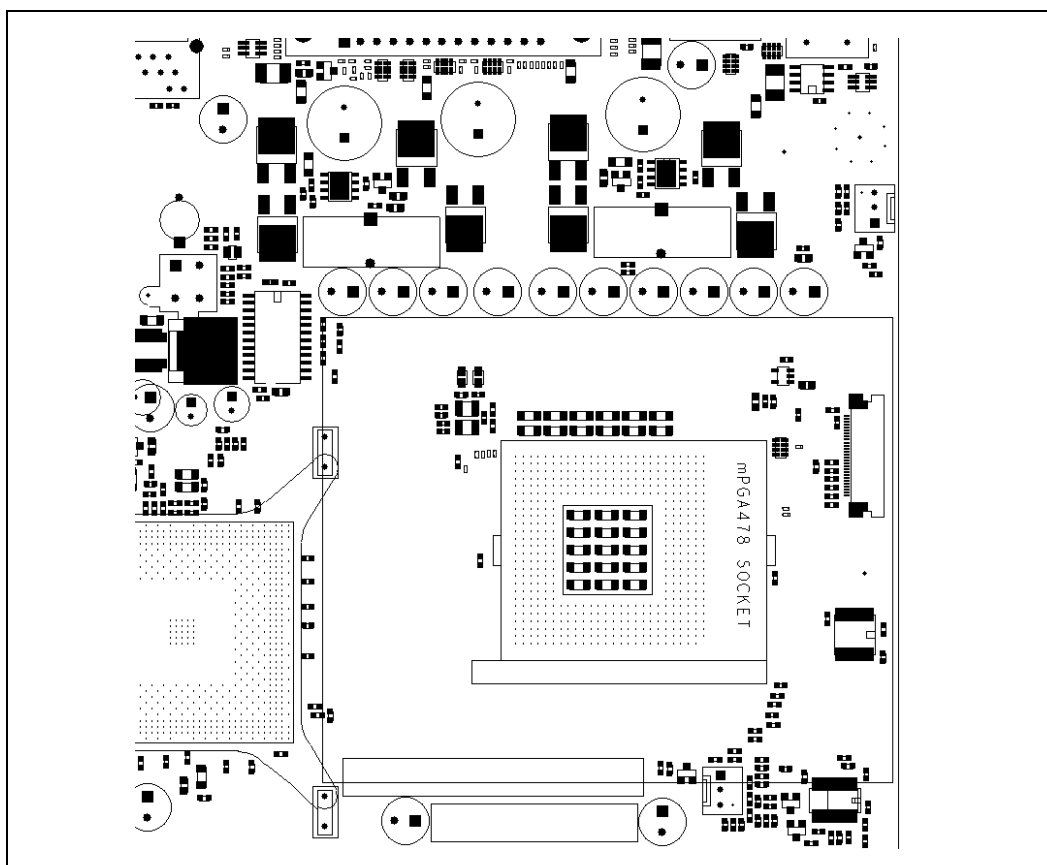
Specifications for the processor voltage are contained in the *Intel Pentium 4 Processor on 90 nm Process Datasheet* and the *Intel Pentium 4 Processor with 512 KB L2 Cache on 0.13 Micron Processor Datasheet* (refer to [Section 1.1, "Reference Documentation" on page 19](#)). These specifications are for the processor. For guidance on correlating the die specifications to socket level measurements, refer to the *Voltage Regulator-Down (VRD) 10.0 Design Guidelines* and addendum.

The voltage tolerance of the load lines contained in the documents mentioned above help the system designer to achieve a flexible motherboard design solution for all different frequencies of the processor. Failure to meet the load line requirements when modeling the system power delivery may result in a system that is not upgradeable.

The processor requires local regulation due to its higher current requirements while maintaining power supply tolerance. For example, an on-board DC-to-DC converter converts a higher DC voltage to a lower DC voltage using a switching regulator. Distributing lower current at a higher voltage to the converter minimizes unwanted losses ( $I \times R$ ). More importantly however, an on-board regulator regulates the voltage locally, which minimizes DC line losses by reducing motherboard resistance on the processor voltage. [Figure 128](#) shows an example of the placement of the local voltage regulation circuitry.

In this section, North and South are used to describe a specific side of the socket based on the placement of the customer reference board shown in [Figure 128](#). North refers to the side of the processor closest to the back panel and South refers to the side of the processor closest to the system memory.

Figure 128. Two Phase VR Component Placement Example



### 13.3.1.2 Decoupling Requirements

In order for the processor voltage regulatory circuitry to meet the transient specifications of the processor, proper bulk and high-frequency decoupling is required. The decoupling requirements for the processor power delivery in this case are shown in [Table 97](#).

Table 97. Decoupling Requirements

Capacitance	ESR (each)	ESL (each)	Filter	Notes
(10) AL Polymer 680 $\mu$ F	5 m $\Omega$	4 nH	Output	1
(40) 1206 pkg 22 $\mu$ F X5R	3.5 m $\Omega$	1.4 nH	Output	1, 2
(4) Al Electrolytic 1200 $\mu$ F 16 V 2.1 A Ripple	22 m $\Omega$	30 nH	Input	1
(4) 1206 pkg 4.7 $\mu$ F	6 m $\Omega$	1.1 nH	Input	1

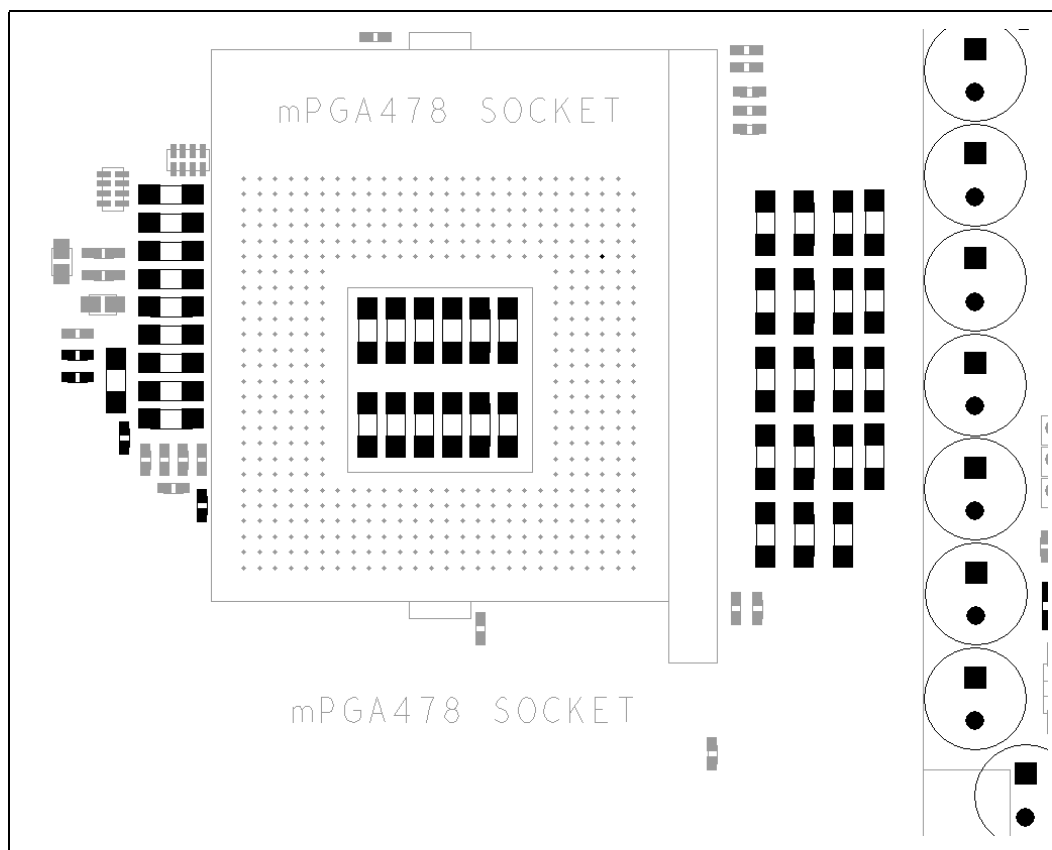
**NOTES:**

1. The ESR, ESL, and ripple current values in this table are based on the values used in power delivery simulations used by Intel and they are not vendor specifications.
2. The decoupling should be placed as close as possible to the processor power pins. [Table 97](#) details the recommended values and [Figure 129](#) illustrates the recommended placement. The placement drawings shows sites for 10 AL Polymer capacitors and 40 1206 package 22  $\mu$ F capacitors. The sites are populated as shown in [Table 98](#). The voltage regulator designer should ensure that an adequate amount of decoupling is present such that the circuit meets the processor specifications.

**Table 98. Decoupling Location**

Type	Number	Location
680 $\mu$ F AL Polymer	10	North side of processor, as close as possible to the keep-out area for the retention mechanism
22 $\mu$ F	12	Inside the processor socket cavity; all sites stuffed
22 $\mu$ F	9	West side of the processor, as close to the socket as possible; all sites stuffed
22 $\mu$ F	19	East of processor socket; six sites stuffed

**Figure 129. Decoupling Placement**



### 13.3.1.3 Layout

Processor VCC shapes on both the top and bottom layers should be maximized, within the constraints of the FSB and PLL routing and placement requirements. The copper plane areas on processor VCC (and also GND) directly impact the motherboard parasitics for CPU power delivery, which in turn impact the amount of bulk decoupling required to meet the Socket Load Line specification. Therefore, the most cost-effective design practice is to maximize processor VCC shapes in the CPU area on both top and bottom layers. [Figure 130](#) through [Figure 134](#) show examples of how to use shapes to deliver power to the processor.

**Figure 130. Top Layer Power Delivery Shape (VCC\_CPU)**

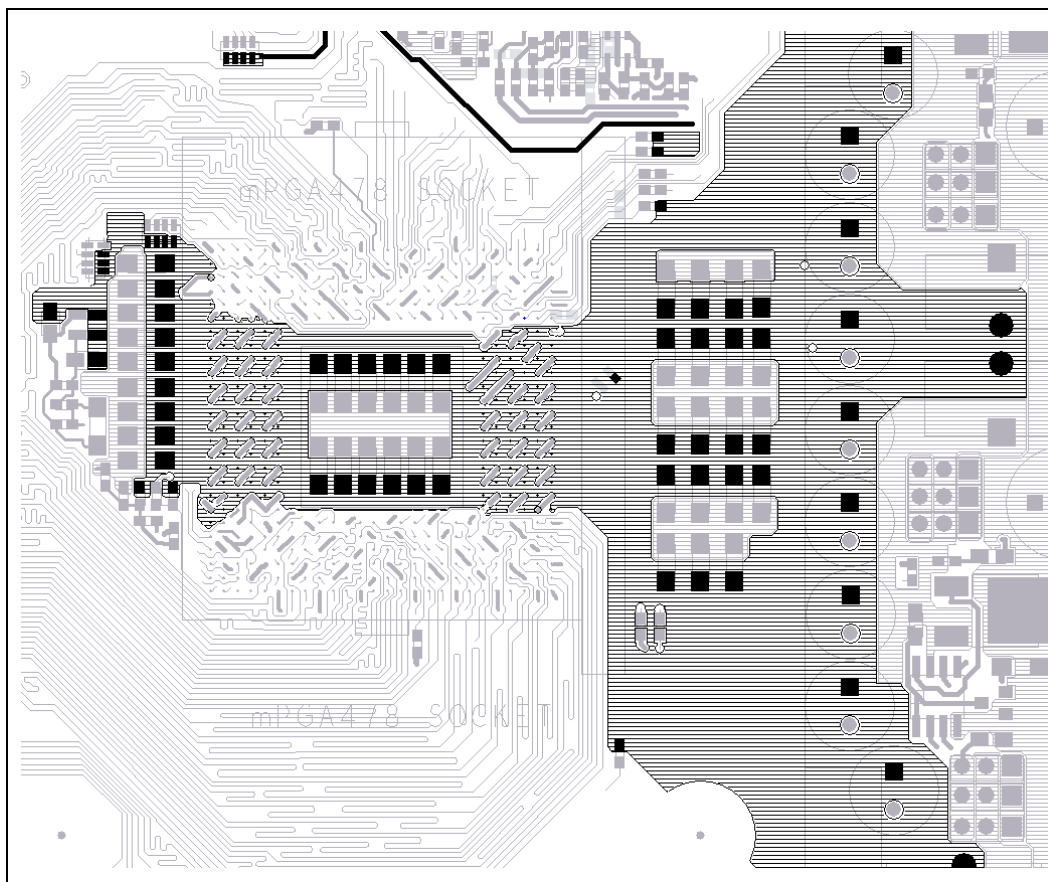
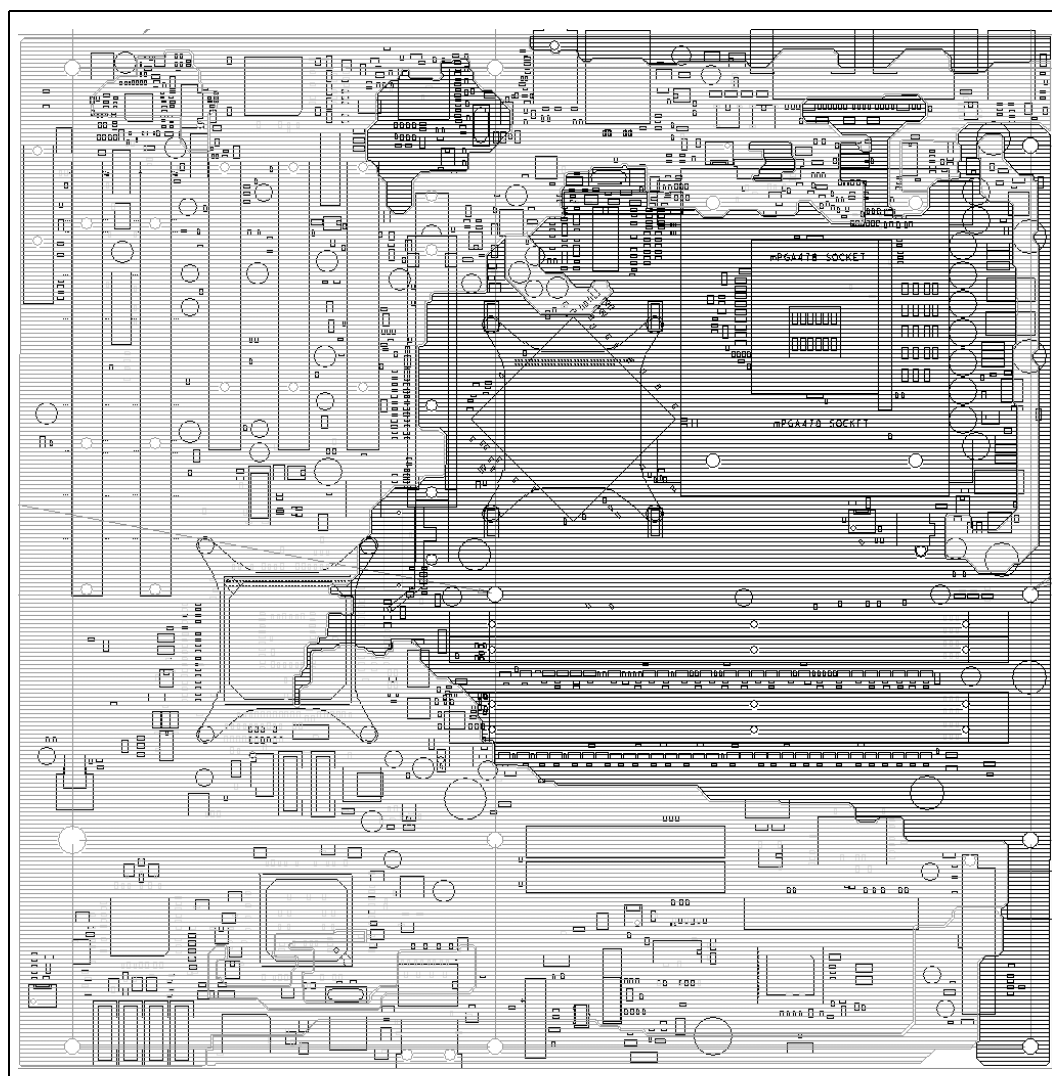
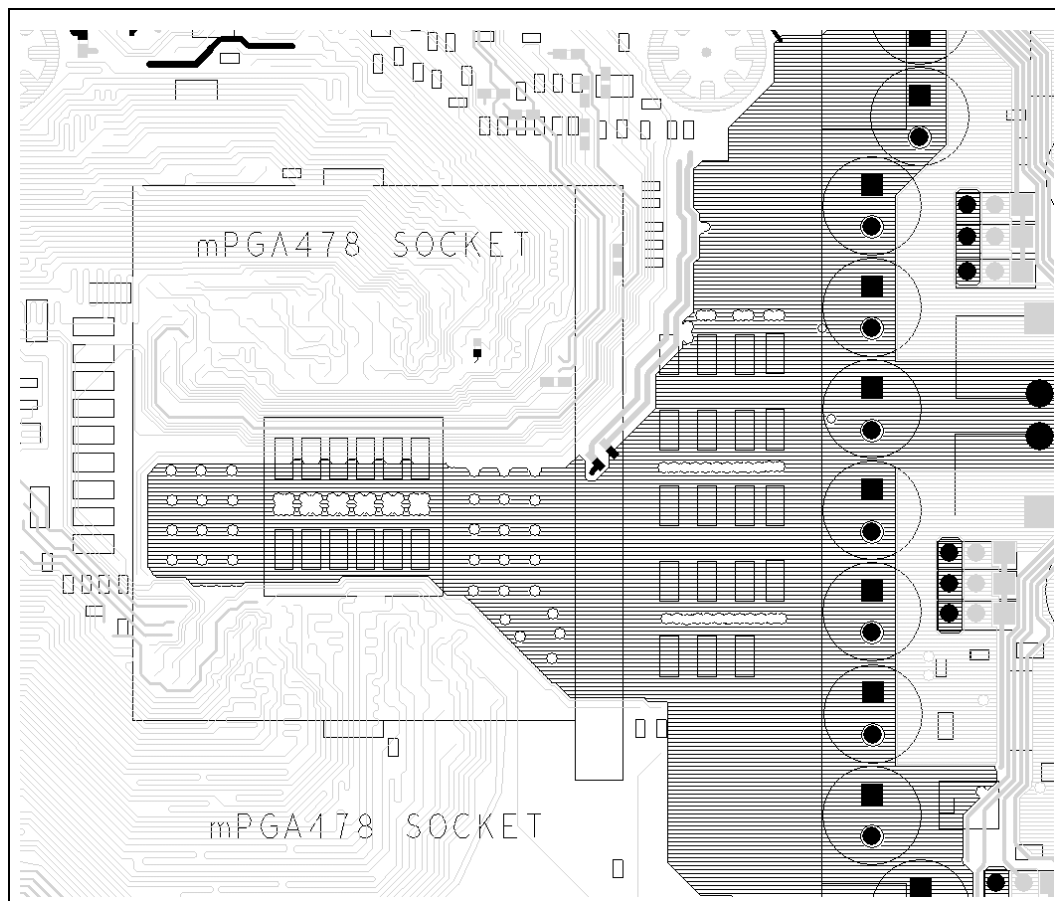


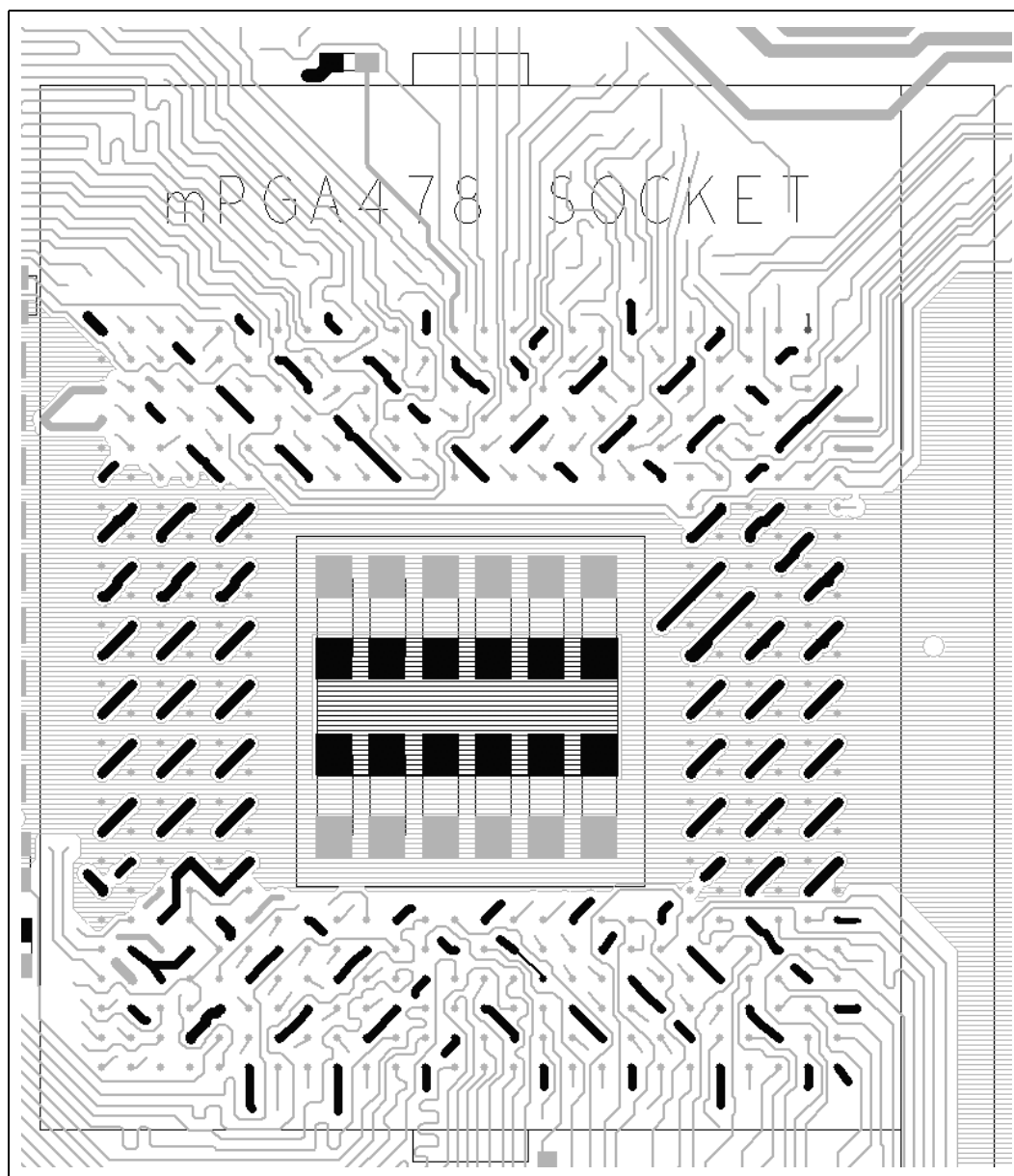
Figure 131. Layer 2 Power Delivery Shape (VSS)



**Figure 132. Bottom Layer Power Delivery Shape (VCC\_CPU)**

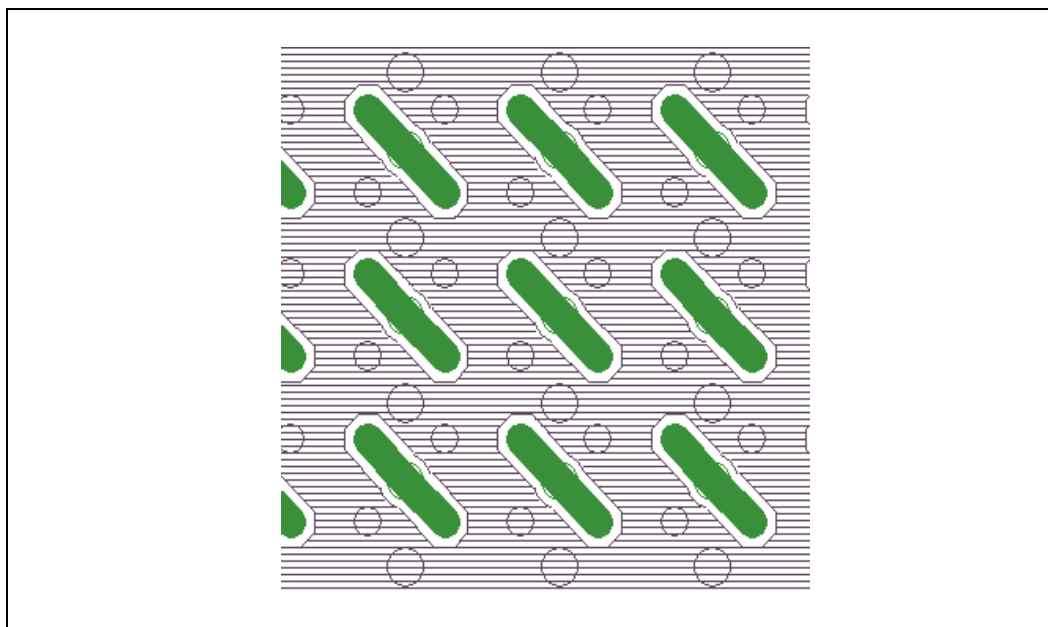
The 22  $\mu$ F 1206 capacitors inside of the socket cavity should be oriented such that the current flow through the capacitor field is maximized. This may be accomplished by orienting the capacitors in an east/west direction with the grounds on the inside, as shown in [Figure 133](#).

Figure 133. Capacitor Orientation



The processor socket has 478 pins with 50 mil pitch. The routing of the signals, power, and ground pins will require creation of many vias. These vias cut up the power and ground planes beneath the processor resulting in increased inductance in of these planes. In order to provide the best path through the via field, it is recommended that the vias are shared for every two processor ground pins and every two processor power pins. [Figure 134](#) illustrates this via sharing.

Figure 134. Shared Ground and Power Vias



The switching voltage regulators typically used for processor power delivery require the use of the feedback signal for output error correction. Previous socket 478 platforms required sensing the voltage regulator feedback from the socket or the system board voltage plane. For the 875P MCH/E7210 MCH/6300ESB ICH chipset using VRD10 controllers, Intel is evaluating whether die sense will provide a performance benefit over socket sense. In order to provide maximum flexibility for this design, Intel recommends that the system board be routed with an option for both socket feedback and die feedback. This design guide will be updated with the final recommendation for either socket or die sense once the analysis has been completed.

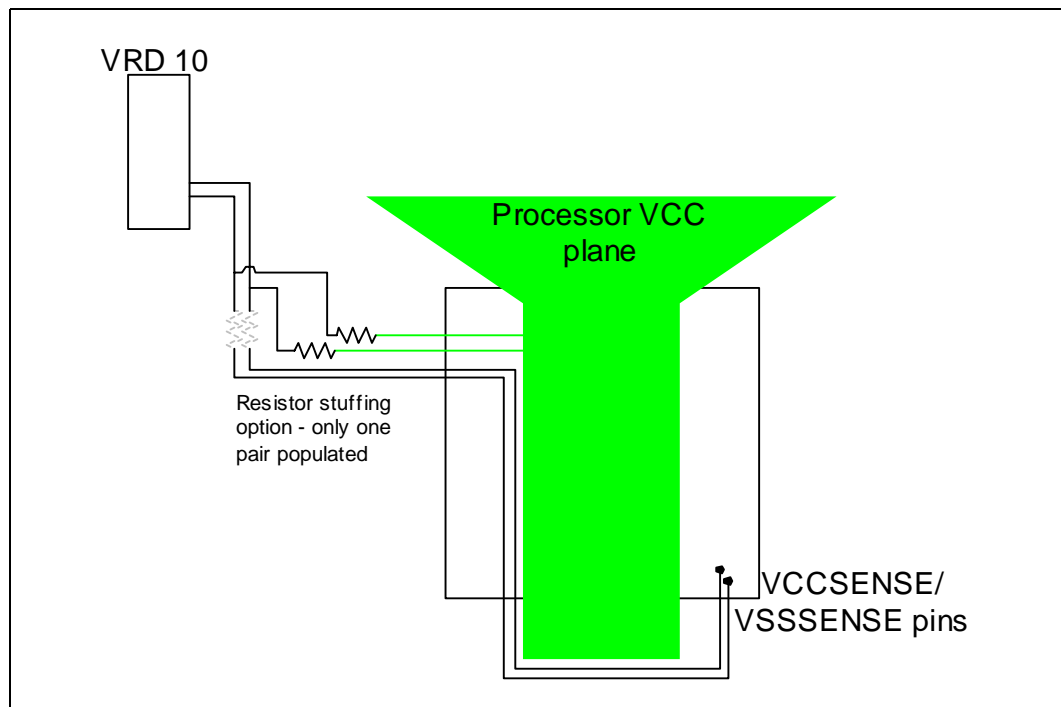
The socket load line defined in the *Voltage Regulator-Down (VRD)10.0 Design Guidelines* and addendum is defined at pins AC14 (VCC\_CPU) and AC15 (VSS) and should be validated from these pins as well. These pins are located approximately in the center of the pin field on the North side of the processor. Socket feedback for the voltage regulator controller should therefore be taken close to this area of the power delivery shape using wide, low inductive traces.

The die loadline is defined at the processor VCC\_SENSE and VSS\_SENSE pins. The die feedback should be taken from these pins using wide, low inductive traces.

Four, 0  $\Omega$  resistors may be used as shown in [Figure 135](#) to create a manufacturing stuffing option to implement either die or socket sense. Intel recommends populating the resistors for socket sense for initial board builds.



**Figure 135. Routing of Feedback Signal**



### 13.3.1.4 Thermal Considerations

For a power delivery solution to meet the Flexible Motherboard (FMB) requirements, it must be able to deliver a fairly high amount of current. This high amount of current also requires that the solution is able to dissipate the associated heat generated by the components and keep all of the components and the PCB within their thermal specifications. OEMs should evaluate their component configurations, system airflow, and layout to ensure adequate thermal performance of the processor power delivery solution.

Intel recommends that the 875P MCH/E7210 MCH/6300ESB ICH chipset system boards be designed to support the full Pentium 4 processor with HT Technology FMB1.5 guidelines. These guidelines include an ICC\_MAX electrically for brief time periods. The voltage regulator solution should also be designed to support a minimum of VR\_TDC indefinitely within the envelope of operation conditions of the system. The VR\_TDC limits of the system board are typically governed by the system board thermal limits. Intel recommends that system boards designed to the above guidelines implement a VR thermal monitor circuit. Refer to the *Voltage Regulator-Down (VRD) 10.0: for Desktop Socket 478 Design Guide* for more information (see [Table 1.1 on page 19](#)).

The voltage regulator shown is a two phase solution with four FETs per phase. The layout is optimized to provide adequate thermal relief for the motherboard and other components. The voltage regulator thermal performance was validated using the Intel reference heatsink and the boxed processor heatsink in a representative chassis running in a 25° C and 35° C external ambient environment.

The specifications for ICC\_MAX of the Pentium 4 processor with HT Technology are contained in the *Intel Pentium 4 Processor with HT Technology Electrical, Mechanical, and Thermal Specifications*.

### 13.3.1.5 Simulation

To completely model the system board, one must include the inductance and resistance that exists in the cables, connectors, PCB planes, pins and body of components (such as resistors and capacitors), processor socket, and the voltage regulator module. More detailed models showing these effects are shown in Figure 136.

Figure 136. Power Distribution Model for Processor with Voltage Regulator on System Board

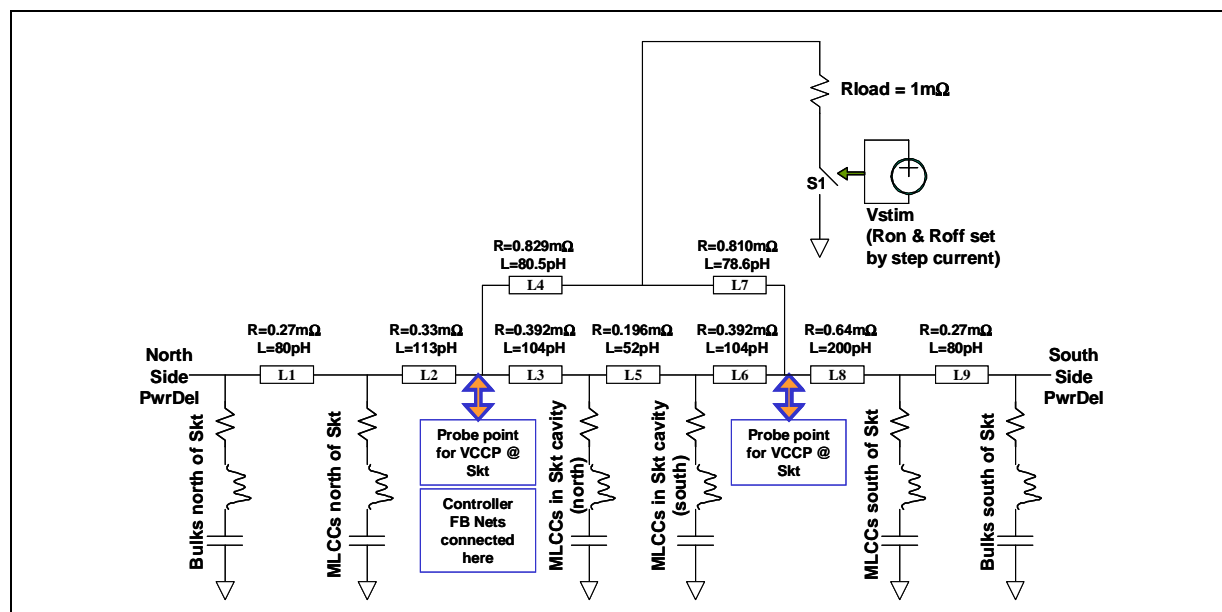


Table 99 lists the parameters for the system board shown in Table 136.

Table 99. Intel® Pentium® 4 Processor with HT Technology Power Delivery Model Parameters

Segment	Resistance	Inductance
L1	0.27 mΩ	80 pH
L2	0.33 mΩ	113 pH
L3	0.392 mΩ	104 pH
L4	0.829 mΩ	80.5 pH
L5	0.196 mΩ	52 pH
L6	0.329 mΩ	104 pH
L7	0.810 mΩ	78.6 pH
L8	0.64 mΩ	200 pH
L9	0.27 mΩ	80 pH

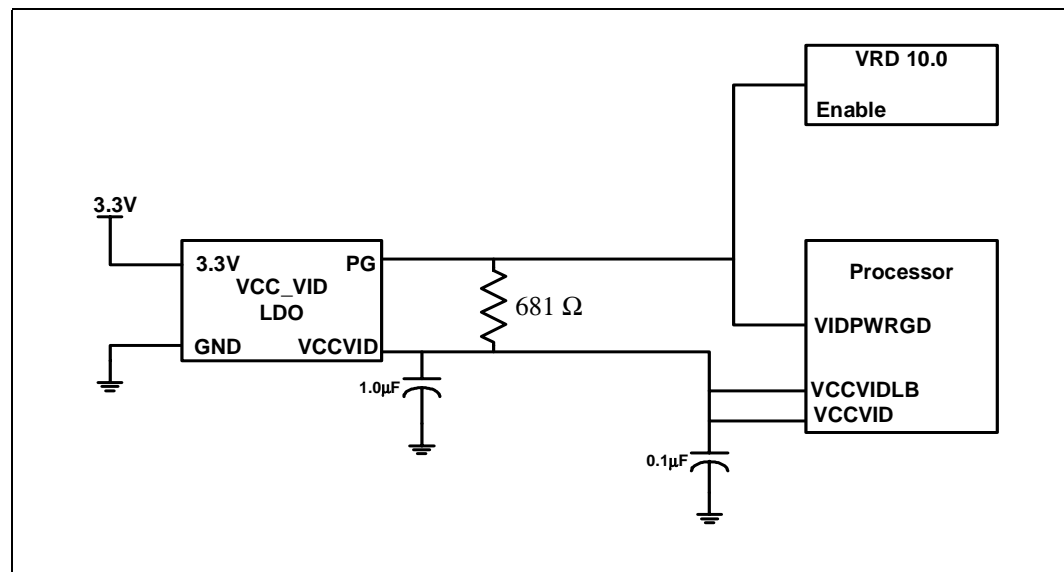
### 13.3.1.6 VCCVID Regulator Guidelines

The VCCVID power plane powers pins AF4 and AF3 of the processor and adheres to the following guidelines. For details on timing requirements for VCCVID refer to the *Intel Pentium 4 Processor with HT Technology Electrical, Mechanical, and Thermal Specifications*.

- The output of the voltage regulator used to generate VCCVID should be no more than 1.5 inches away from pins AF3 and AF4 on the processor.
- The trace connecting the voltage regulator output to pins AF3 and AF4 should be as wide as practical, but no less than 25 mils.
- The trace connecting the voltage regulator output to pin AF3 and AF4 should have both a 0.1  $\mu\text{F}$  and a 1.0  $\mu\text{F}$  capacitor for decoupling. The 1.0  $\mu\text{F}$  capacitor should be located as close as possible to output of the voltage regulator and the 0.1  $\mu\text{F}$  capacitor should be located as close as possible to pins AF3 and AF4 on the processor.
- The PG signal of the VCCVID regulator should be pulled up to VCCVID through a 681 K $\Omega$  resistor.

During power-on the rising edge of the VCCVID power supply needs to be monotonic.

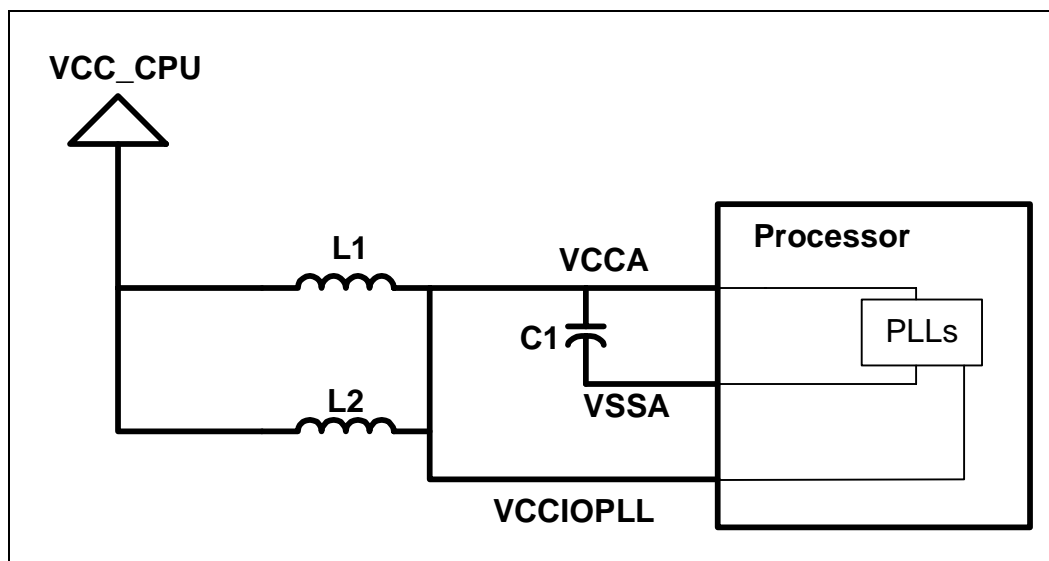
**Figure 137. VCC\_VID Regulator Topology**



### 13.3.1.7 CPU Filter Specifications for VCCA, VCCIOPLL, and VSSA

$V_{CCA}$  and VCCIOPLL are required by the PLL clock generators on the processor's silicon. Since these PLLs are analog in nature they require quiet power supplies for minimum jitter. Jitter is detrimental to a system; it degrades external I/O timings, as well as internal core timings (i.e., maximum frequency). To prevent this degradation these supplies must be low pass filtered from VCC\_CPU. The general desired filter topology is shown in [Figure 138](#). Not shown in the core is parasitic routing. Excluded from the external circuitry are parasitics associated with each component.

Figure 138. Typical VCCIOPLL, VCCA, and VSSA Power Distribution



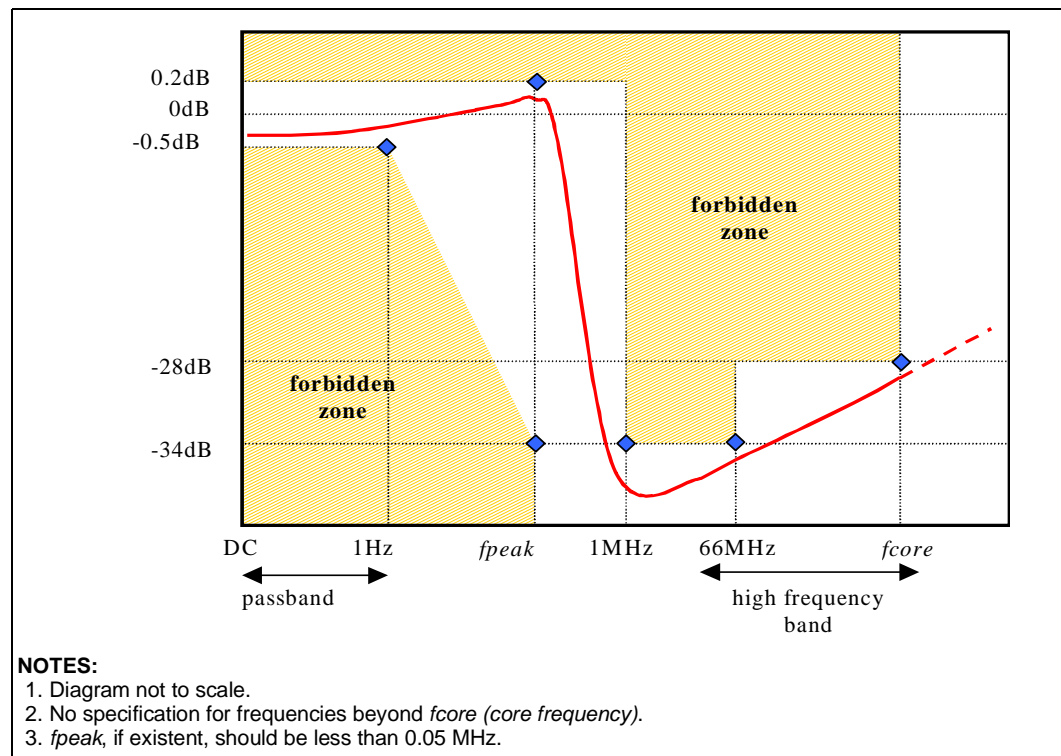
The function of the filter is twofold. It protects the PLL from external noise through low-pass attenuation; it also protects the PLL from internal noise through high-pass filtering. In general, [Figure 138](#) forms an adequate description for the low-pass filter. For simplicity, we are addressing the recommendation for VCCA filter design. The same characteristics and design approach are applicable for the PLL filter design.

The AC low-pass specification, with input at VCC\_CPU and output measured across the capacitor, is as follows:

- < 0.2 dB gain in pass band
- < 0.5 dB attenuation in pass band < 1 Hz (see DC drop in next set of requirements)
- 34 dB attenuation from 1 MHz to 66 MHz
- 28 dB attenuation from 66 MHz to core frequency

The filter specification (AC) is graphically shown in [Figure 139](#).

Figure 139. AC Filter Specification



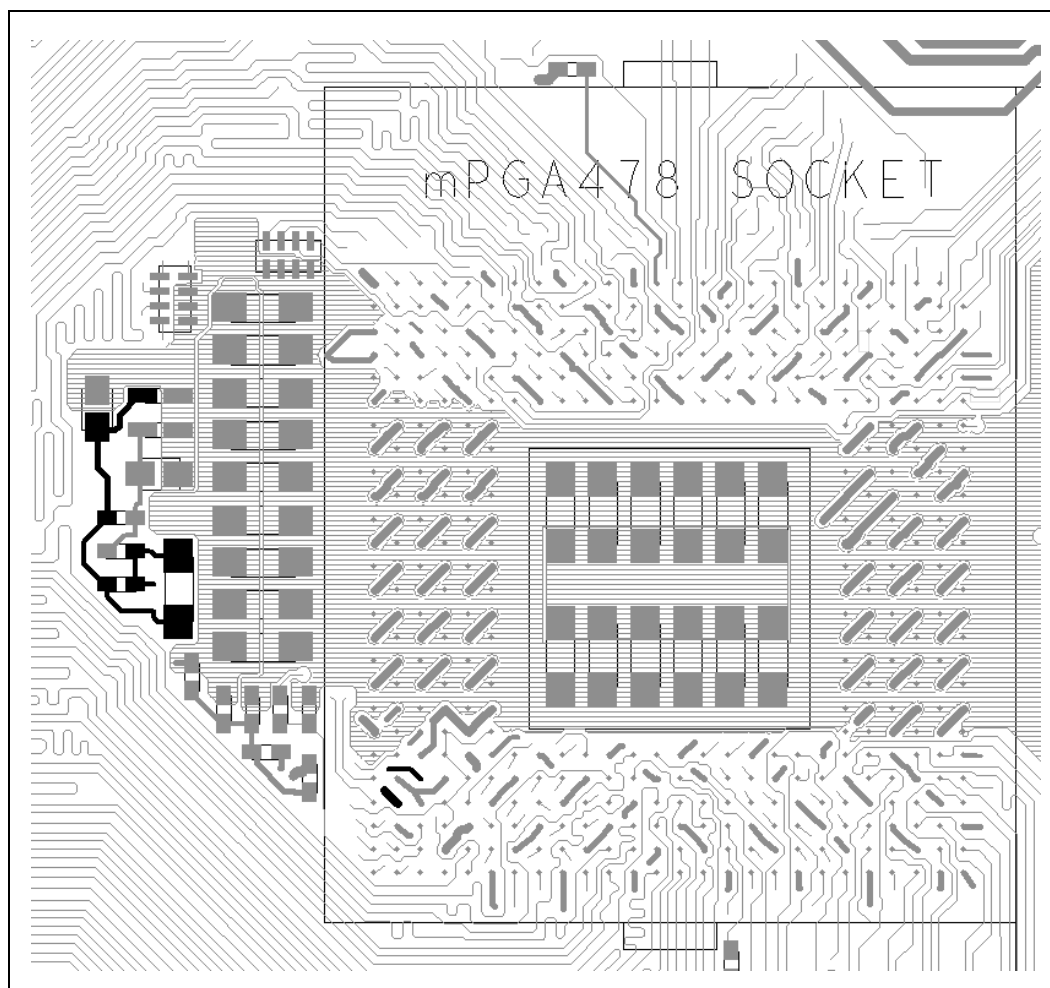
Other requirements:

- Use shielded type inductor to reduce crosstalk.
- Capacitor, C1: 22  $\mu$ F – 33  $\mu$ F with a 20% tolerance. The ESL is  $\leq 2.5$  nH and the ESR  $\leq 0.225 \Omega$ .
- Inductor: 10  $\mu$ H  $\pm 25\%$ . Rdc =  $0.4 \pm 30\%$ . Self Resonant Frequency  $\geq 30$  MHz. IDC = 60 mA
- Filter should support DC current of 100 mA.
- DC voltage drop from VCC\_CPU to VCCA should be  $< 70$  mV.
- In order to maintain a DC drop of less than 70 mV, the total DC resistance of the filter from processor VCC to the processor socket should be a maximum of  $0.7 \Omega$ .

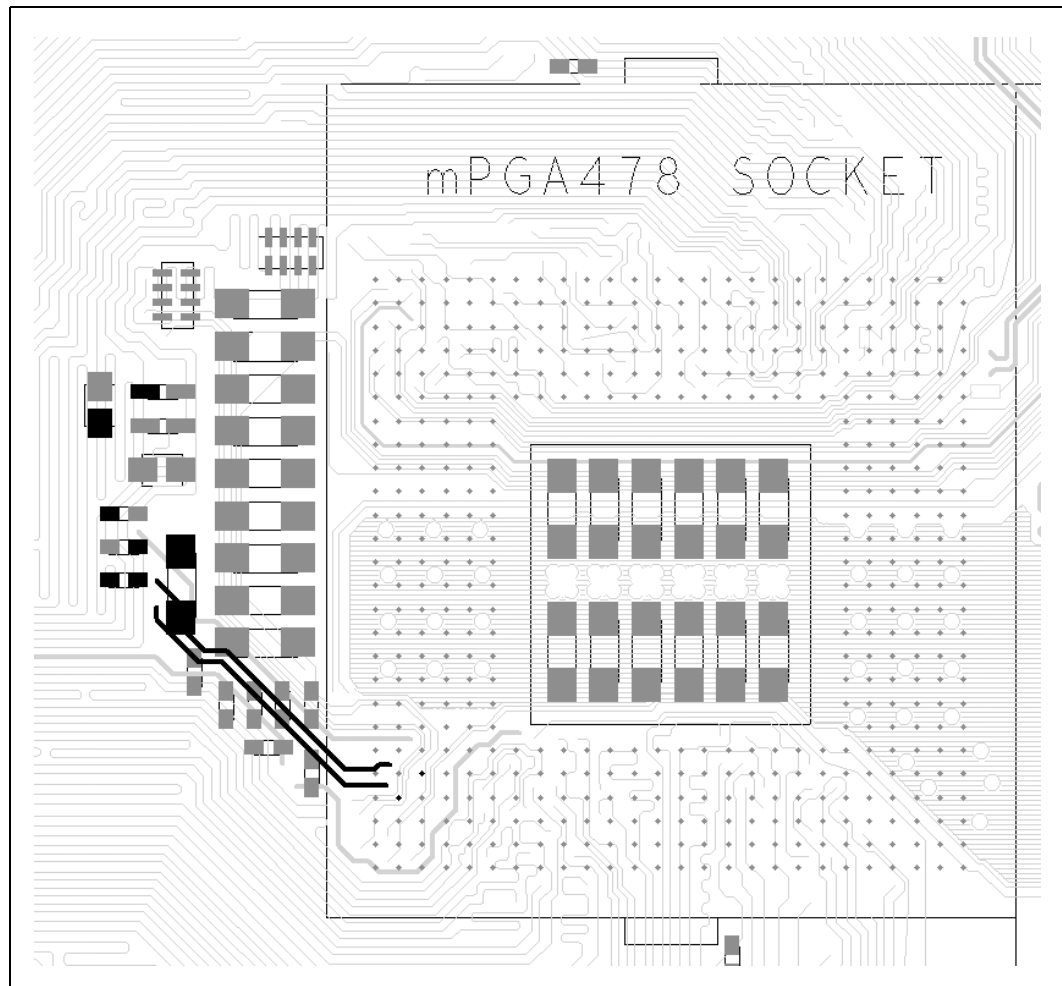
Other routing requirements:

- C1 should be within 600 mils of the VCCA and VSSA pins. An example of the component placement is shown in [Figure 140](#).
- VCCA route should be parallel and next to VSSA route (minimize loop area).
- A minimum of a 12 mil trace should be used to route the filter to the processor pins.
- The inductors (L1 and L2) should be close to the capacitor C1.
- It is recommended that the total resistance of DCR plus routing does not exceed  $0.36 \Omega$ . This results in a max drop of 36 mV for 100 mA maximum.

Figure 140. VCCA and VSSA Layer 1 Routing



**Figure 141. VCCA and VSSA Bottom Layer**



### 13.3.1.8 Processor Power Sequencing

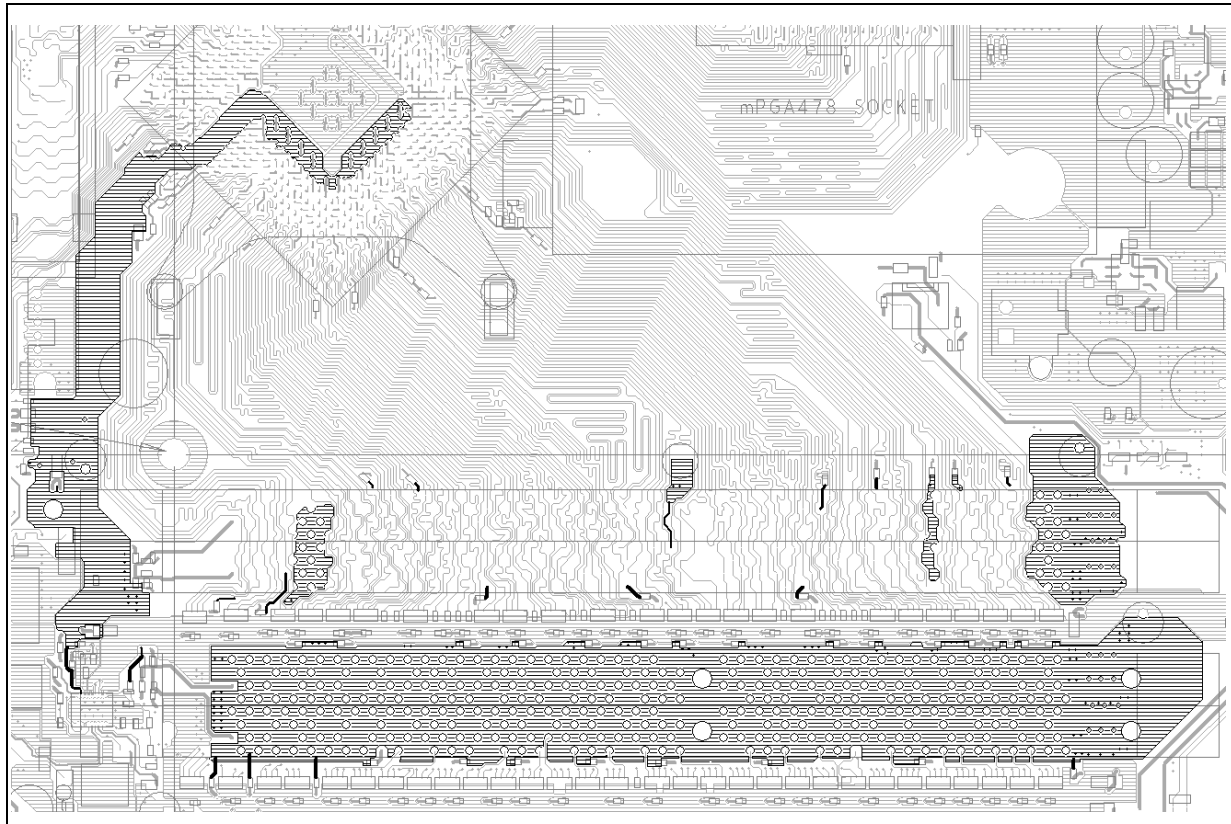
The Pentium 4 processor with HT Technology has specific power-up sequencing requirements. Please refer to the *Intel Pentium 4 Processor with HT Technology Electrical, Mechanical, and Thermal Specifications* for these requirements.

### 13.3.2 MCH Power Delivery Guidelines

Power is delivered to the 875P MCH/E7210 MCH on different layers. Layer 1 provides 1.5 V to the HI, CSA, and AGP interfaces, and 2.55 V to the DDR interface. Layers 2 and 5 provide ground, while layer 6 provides 1.5 V core power.

### 13.3.2.1 DDR (2.55 V Power Plane)

Figure 142. DDR Power Plane— Layer 1



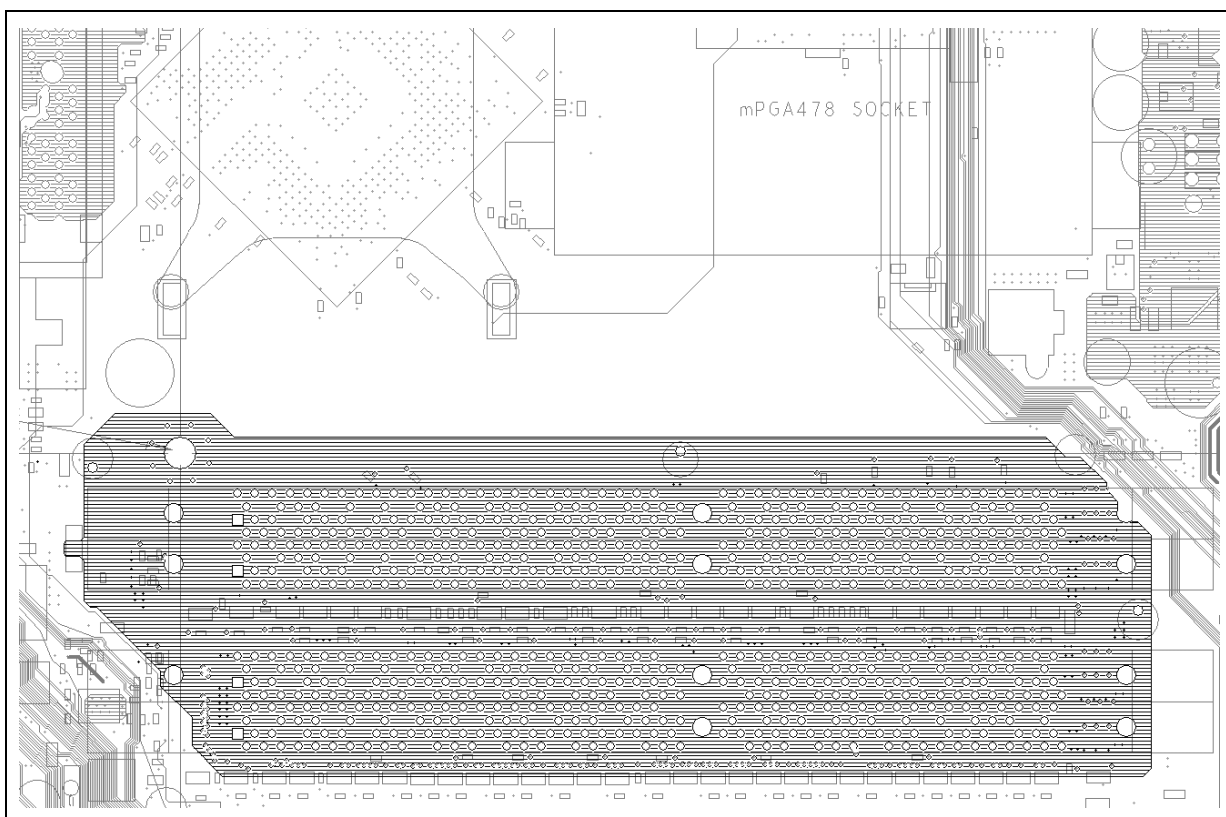
In order to meet the timings for DDR, it is imperative that the DDR power plane to the MCH have as low of DC impedance as possible. The voltage drop caused by the (ICC) delivered to the MCH DDR interface through the power plane resistance (R) plus the tolerance of the voltage regulator (VTOL) must be less than the voltage tolerance specified in the *Intel 875P External Design Specification Addendum* and the *Intel E7210 MCH External Design Specification Addendum*:

$$(I_{cc} * R) + V_{tol} \text{ of Regulator} \leq V_{tol} \text{ specified in the External Design Specification Addendum}$$

To accomplish this, it is very important to use wide, unobstructed planes with good current carrying capability. An example of this is shown above in [Figure 142](#) and below in [Figure 143](#).



Figure 143. 2.55 VDDR Power Plane— Layer 3



### 13.3.2.2 VTT (MCH FSB Power Plane)

Figure 144. VTT (MCH FSB Power Plane)—Layer 1

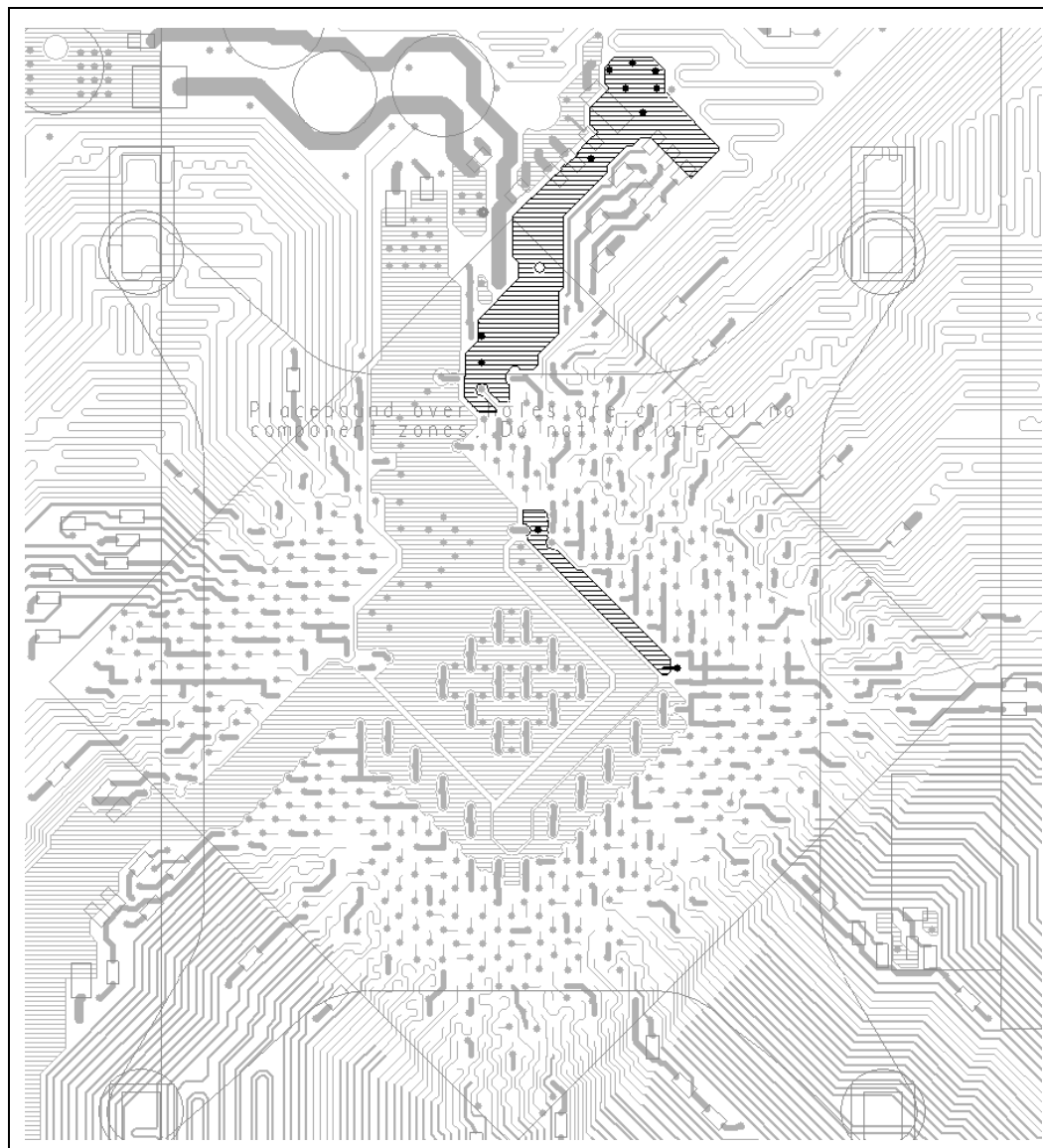
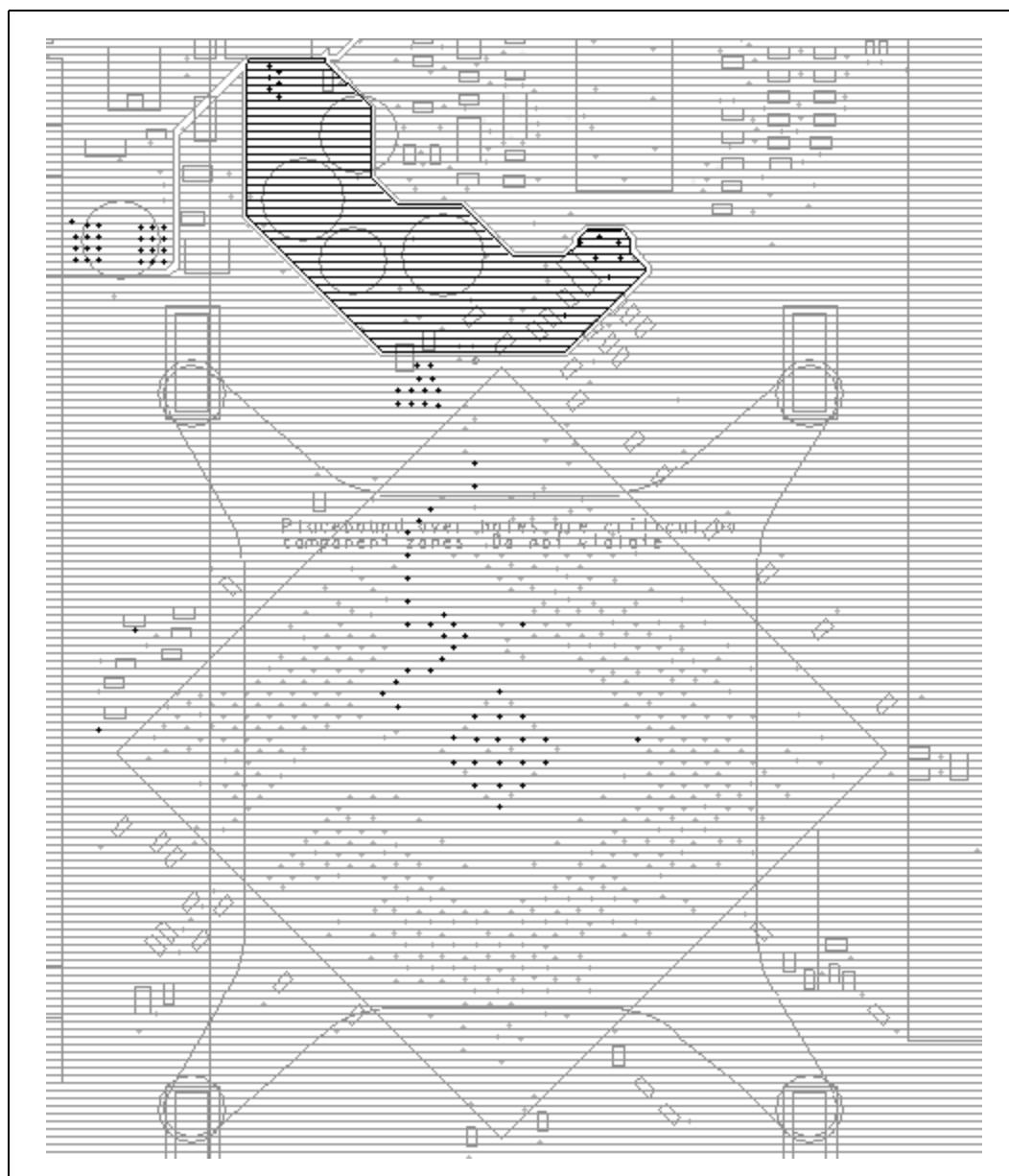


Figure 145. VTT (MCH FSB Power Plane)— Layer 2



### 13.3.2.3 Hub, CSA, AGP (Intel® 875P MCH Only) and Core Interface (1.5 V Power Plane)

Figure 146. 1.5 V Power Plane—Layer 1

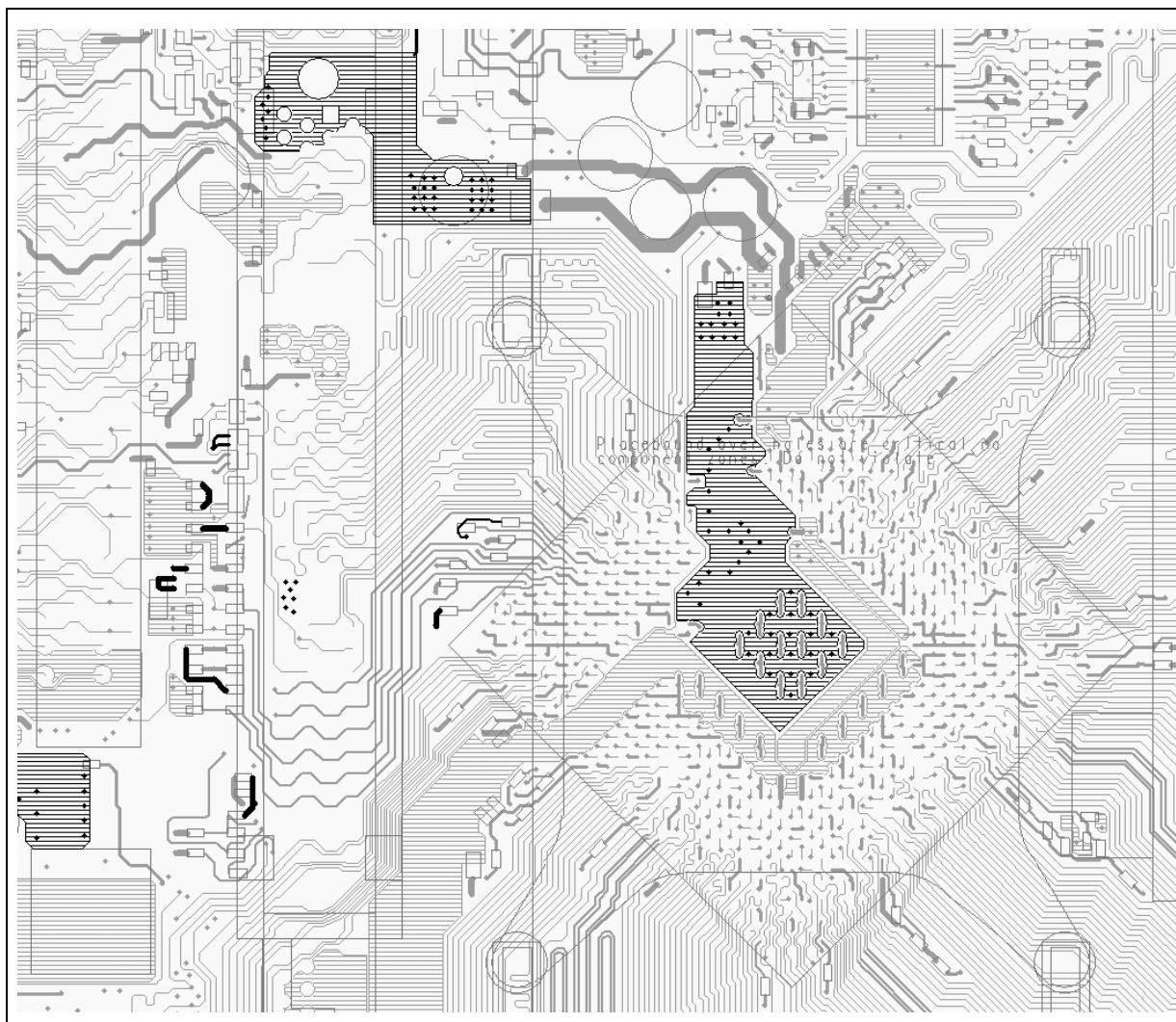
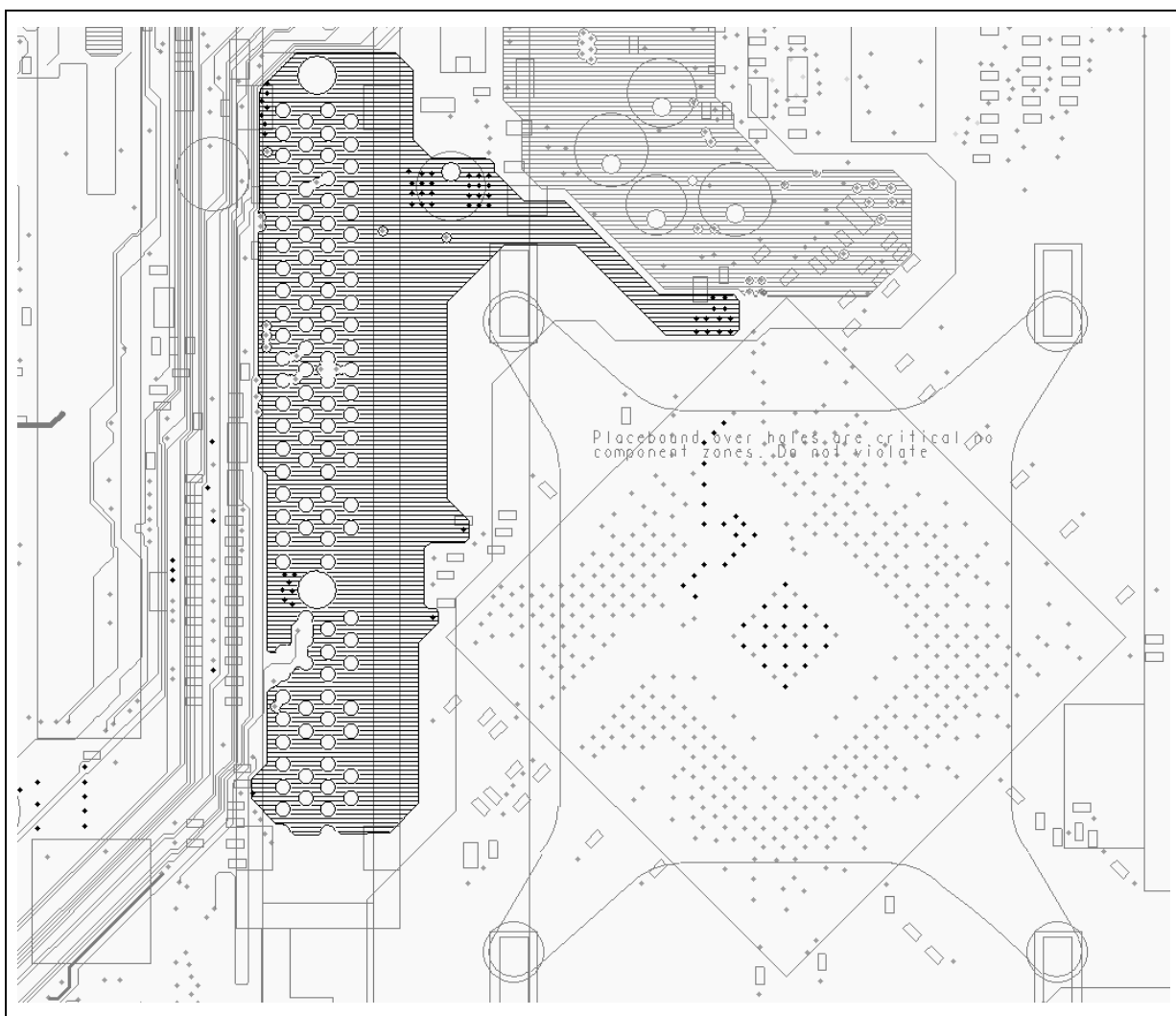
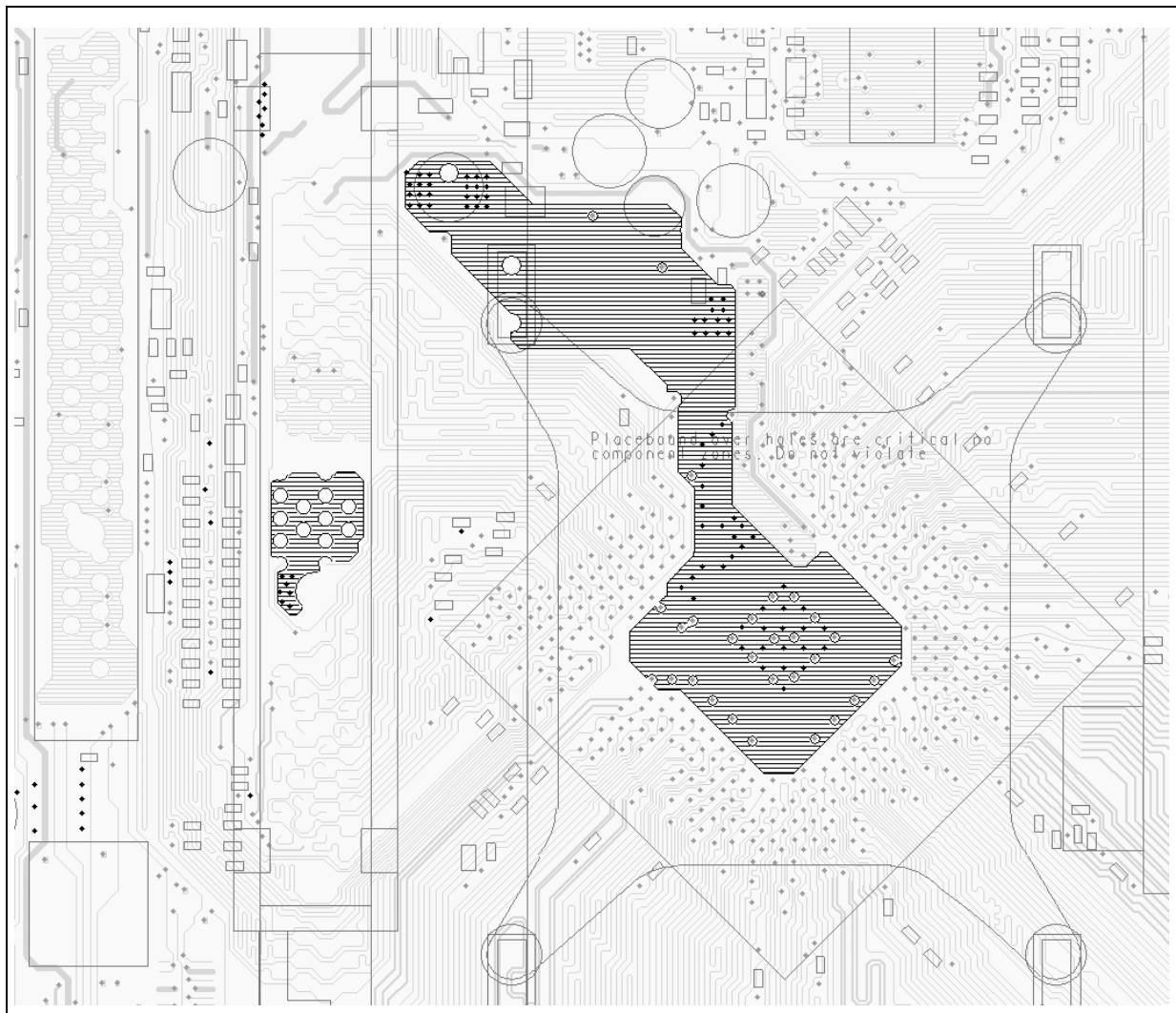


Figure 147. 1.5 V Power Plane— Layer 3



**Figure 148. 1.5 V Power Plane— Layer 6**

### 13.3.2.4 Decoupling Recommendations

The following guidelines are recommended for an optimal 875P MCH/E7210 MCH power delivery. These guidelines will minimize power noise and signal integrity issues.

The guidelines below are not intended to replace thorough system validation of 875P MCH/E7210 MCH/6300ESB ICH chipset-based products.



**Table 100. MCH High-Frequency Decoupling Requirements**

Power Rail	Decoupling Requirements	Decoupling Type (Pin Type)	Decoupling Placement
VTT (MCH FSB)	(1) 0.47 $\mu$ F (1) 0.47 $\mu$ F (1) 0.47 $\mu$ F (1) 0.22 $\mu$ F (1) 0.1 $\mu$ F	Edge capacitors <sup>2</sup> Edge capacitors <sup>2</sup> Edge capacitors <sup>2</sup> Edge capacitors <sup>2</sup> Power plane decoupling	As close to ball A24 as possible As close to ball A20 as possible As close to ball A15 as possible As close to ball A10 as possible As close to MCH as possible
VCC_AGP	(1) 0.47 $\mu$ F (1) 0.1 $\mu$ F (1) 0.1 $\mu$ F	Edge capacitor <sup>2</sup> Edge capacitor <sup>2</sup> Edge capacitor <sup>2</sup>	As close to ball AE1 as possible As close to ball AA1 as possible As close to ball T1 as possible
VCC_HI	(1) 0.1 $\mu$ F (1) 0.22 $\mu$ F	Edge capacitor <sup>2</sup> Edge capacitor <sup>2</sup>	As close to ball AN8 as possible As close to ball AN5as possible
VCCDDR	(1) 0.1 $\mu$ F (1) 0.47 $\mu$ F (1) 0.22 $\mu$ F (1) 0.1 $\mu$ F (1) 0.22 $\mu$ F (1) 0.47 $\mu$ F (1) 0.1 $\mu$ F	Edge capacitor <sup>2</sup> Edge capacitor <sup>2</sup> Edge capacitor <sup>2</sup> Edge capacitor <sup>2</sup> Edge capacitor <sup>2</sup> Edge capacitor <sup>2</sup> Power plane decoupling	As close to ball D33 as possible As close to ball AN30 as possible As close to ball AN22 as possible As close to ball AN18 as possible As close to ball AD33 as possible As close to ball P33 as possible As close to MCH as possible

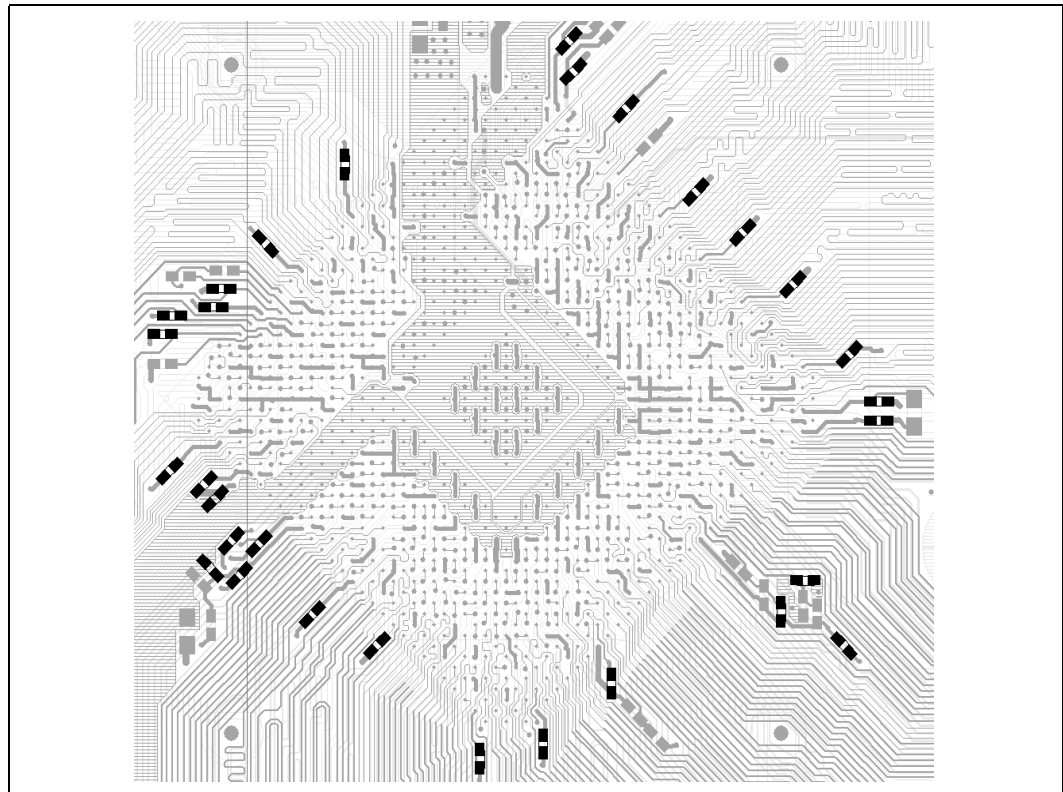
**Figure 149. MCH High-Frequency Decoupling Capacitor Placement**


Figure 150. MCH Bulk Decoupling Capacitor Placement

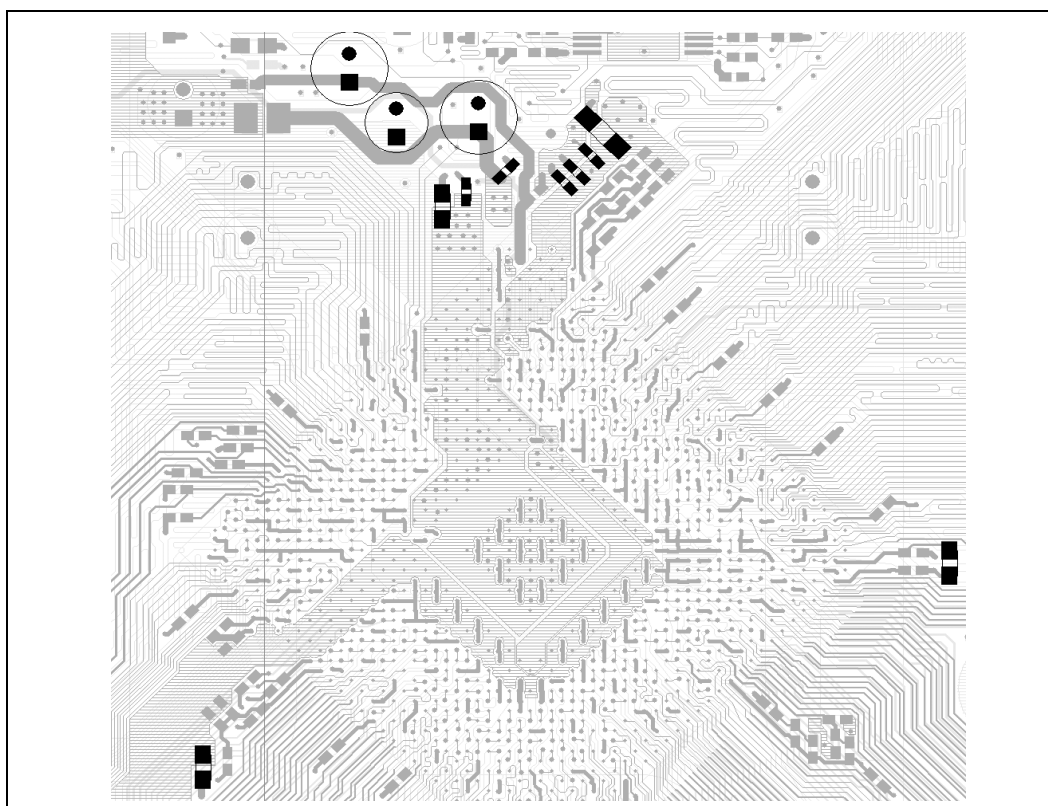


Table 101. MCH Bulk Decoupling Requirements

Plane	Decoupling Requirements	Decoupling Placement
VTT (MCH FSB)	(1) 0.1 $\mu$ F (1) 0.47 $\mu$ F (1) 1.0 $\mu$ F (2) 4.7 $\mu$ F (1) 470 $\mu$ F	Place on MCH VTT plane using good layout practices. Such as placing the smaller value capacitors closer to the MCH than the higher value capacitors.
VCCDDR	(1) 22 $\mu$ F (1) 4.7 $\mu$ F	Place at the 2.55 V power plane transitions to layer 1 at the MCH.
VCC (MCH Core)	10 $\mu$ F	Place as close to where the 1.5 V core and 1.5 V AGP/CSA planes diverge.

### 13.3.3 MCH Filter Specifications

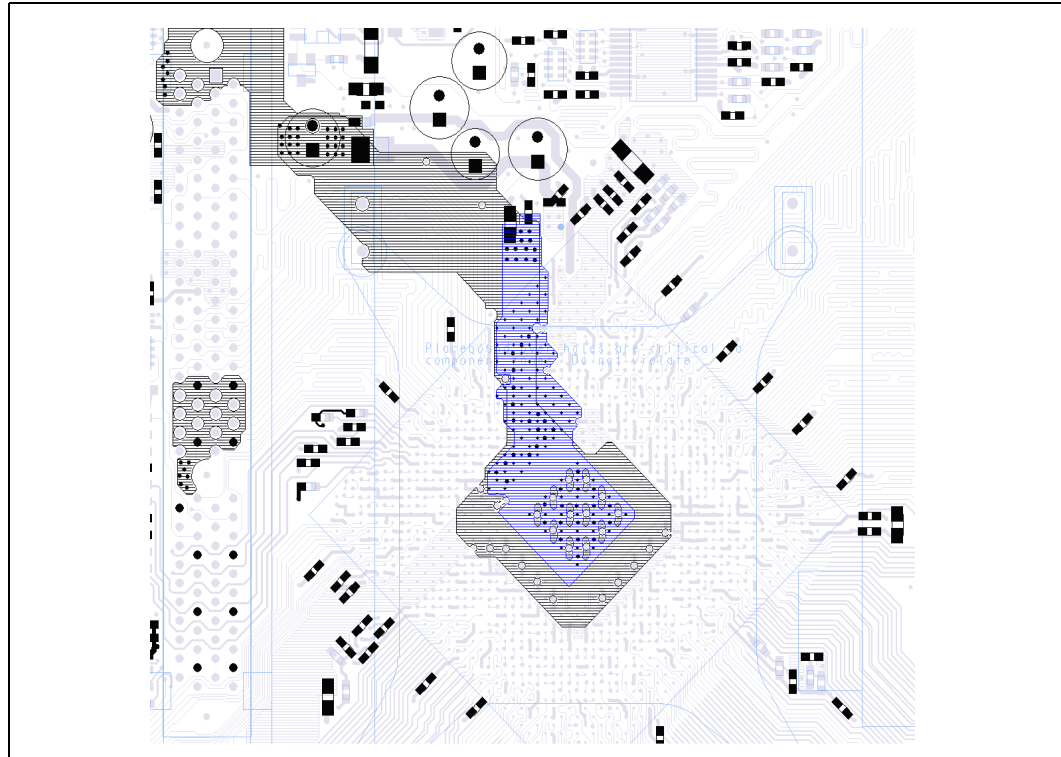
#### 13.3.3.1 Plane Filter

1.5 V core power needs to be filtered between pins to the 1.5 V AGP, HI, and CSA power pins. This is easily accomplished by having two separate power floods into the 875P MCH/E7210 MCH for 1.5 V power. One power flood will be on layer 4 which will supply 1.5 V power for the core,



while on layer 1 the 1.5 V power flood will supply power for AGP, HI, and CSA. To filter these planes, each flood will need to be referenced to ground and at the point where the two planes separate, there needs to be one (1) 0805 10  $\mu$ F Y5 V capacitor.

**Figure 151. MCH Filter Topology for 1.5 V Core**



### 13.3.3.2 Analog Filters

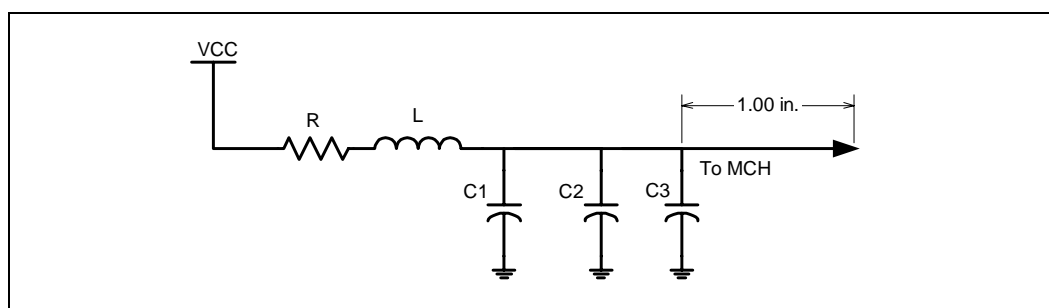
In addition to the plane filters, an additional four analog filter circuits are required for the MCH's VCCA\_DDR and VCCA\_FSB pins. All of the filters require an inductor.

**Table 102. MCH Analog Filter Requirements**

Required 875P MCH/ E7210 MCH Filters	Filter Current Capability (mA)	Filter DC Resistance ( $\Omega$ ) <sup>1</sup>	Max DC Drop (mV) <sup>2</sup>	Pass Band Gain (dB)	f1	f2	Attenuation from f1 to f2 (dB)
VCCA_FSB	30	2.3	70	<+0.2, >-0.5	50 MHz	800 MHz	-30
VCCA_DDR	1000	0.070	70	<+0.2, >-0.5	50 MHz	400 MHz	-30

**NOTES:**

1. Filter DC resistance is the inductor resistance + MB routing resistance.
2. DC drop across filter includes voltage drop across the inductor and across the MB trace.

**Figure 152. MCH Analog Filter Topologies**

The recommended component values for the filter are presented in [Table 103](#):

**Table 103. MCH Analog Filter Components**

Component	Value	Package Type
<b>VCCA_DDR Filter</b>		
VCC	1.5 V	
R	0 $\Omega$	NA
L <sup>1</sup>	1 $\mu$ H	1210
C1	NA	NA
C2	100 $\mu$ F	Aluminum
C3	0.1 $\mu$ F	0603
<b>VCCA_FSB Filter</b>		
VCC	1.5 V	
R	0 $\Omega$	NA
L <sup>2</sup>	82 $\mu$ H	1210
C1	NA	NA
C2	100 $\mu$ F	Aluminum
C3	0.1 $\mu$ F	0603

**NOTES:**

1. The DCR of the inductor must be < 50 m $\Omega$ .
2. The DCR of the inductor must be  $\leq$  2.1  $\Omega$

The VCCA\_AGP does not require a filter, but it does need to connect to the 1.5 V core power plane.

The VCCA\_DDR trace is carrying 1 A of current and DC resistance of this trace needs to be kept at or below 50 m $\Omega$ . To do this, it is recommended to route the VCCA\_DDR with a trace width of 50 mils whenever possible. When routing under the MCH ball field, it is acceptable to neck the trace down to 35 mils. [Figure 153](#) and [Figure 154](#) show an example of the recommended routing.

Figure 153. Layer 1 VCCA\_DDR

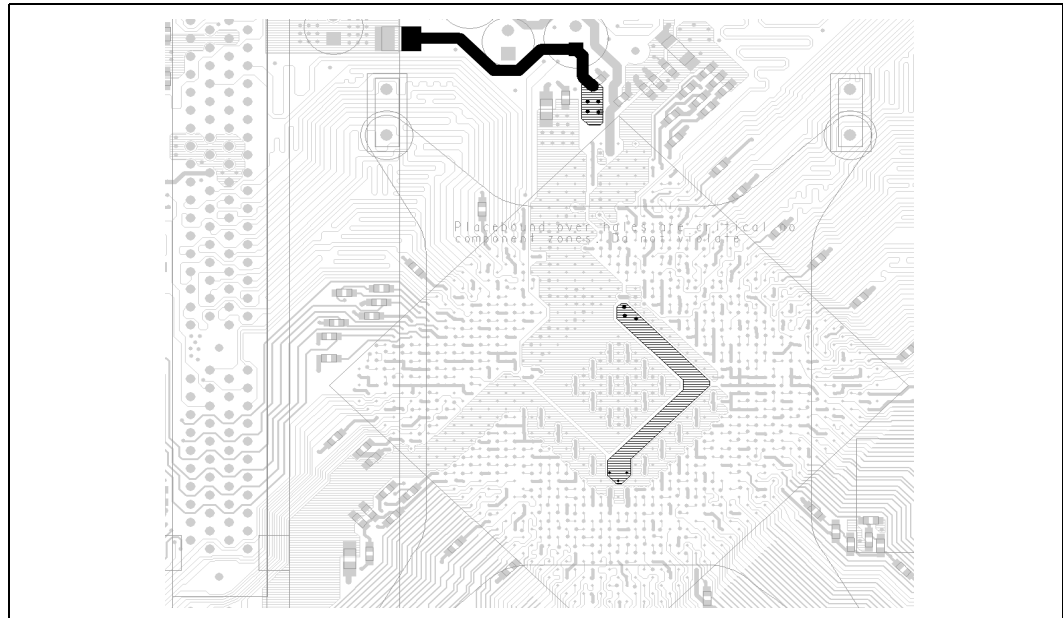
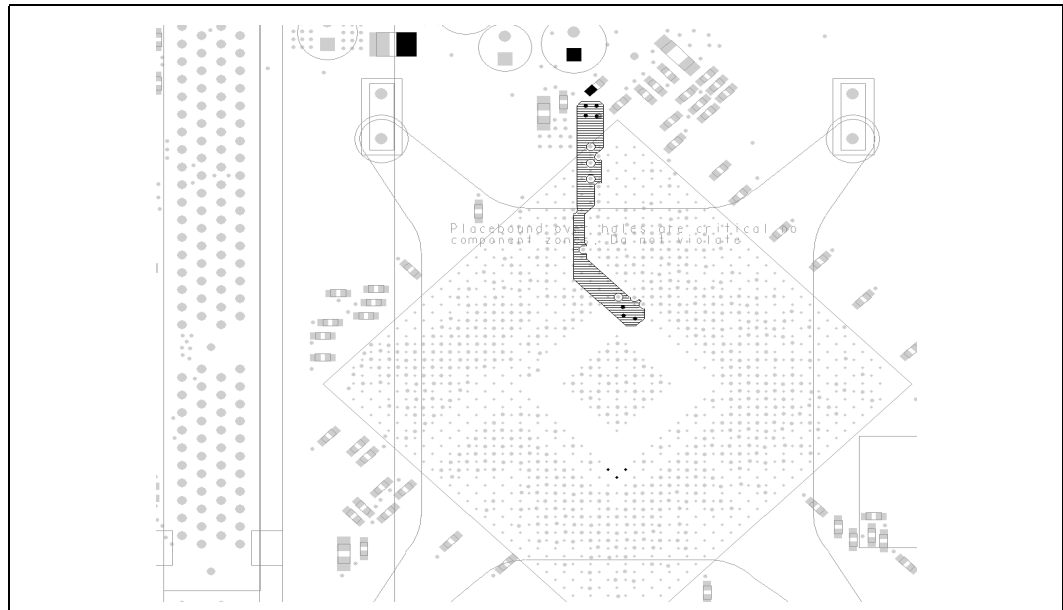


Figure 154. Layer 6 VCCA\_DDR



### 13.3.3.3 MCH Power Sequencing Requirements

There are no power sequencing requirements for the 875P MCH/E7210 MCH. However, the following timings must be met:

- GCLKIN must be valid at least 10  $\mu$ s prior to the rising edge of PWROK.
- HCLKN/HCLKP must be valid at least 10  $\mu$ s prior to the rising edge of RSTIN#.

## 13.3.4 ICH Power Delivery Guidelines

### 13.3.4.1 Power Supply PS\_ON Consideration

If a pulse on SLP\_S3# or SLP\_S5# is short enough (~10–100 ms) such that PS\_ON is driven active during the exponential decay of the power rails, a few power supply designs may not be designed to handle this short pulse condition. In this case, the power supply will not respond to this event and will never power back up. **These power supplies would need to be unplugged and re-plugged to bring the system back up.** Power supplies not designed to handle this condition must have their power rails decay to a certain voltage level before they may properly respond to PS\_ON. This level varies with affected power supply.

The ATX specification does not specify a minimum pulse width on PS\_ON de-assertion, which means power supplies must be able to handle any pulse width. This issue may affect any power supply (beyond ATX) with similar PS\_ON circuitry. Due to variance in the decay of the core power rails per platform, a single board or chipset silicon fix would be non-deterministic (may not solve the issues in all case).

The platform designer must ensure that the power supply used with the platform is not affected by this issue.

### 13.3.4.2 SLP\_S4# Assertion Width

When removing and reapplying power to the DRAM, the DRAMs need to see the power supply down for a minimum period of time before it may be treated as a “cold reset” and safely power up. All cases in which the DRAM power is removed could potentially be a problem if the minimum time requirement is not met. This potentially could occur during resume from S4/S5. To address this potential issue, the 6300ESB ICH has implemented timers to help ensure that this minimum period of time is met.

The aforementioned time is the assertion width of SLP\_S4#. If the assertion width is less than the minimum period of time set in SLP\_S4# Minimum Assertion Width register (D31:F0, offset A4h), the 6300ESB ICH has provided a means to help ensure that this minimum time is met. The amount of time required to safely power up is DRAM-specific.

This feature may be disabled using bit 3 of the same register.

### 13.3.4.3 3.3 V/1.5 V Power Sequencing

There are no power sequencing requirements for the associated 3.3 V/1.5 V rails or the rail of the 6300ESB ICH. However, it is generally good design practice to power up the core before or at the same time as the other rails.

#### 13.3.4.3.1 PCI-X Power Sequencing

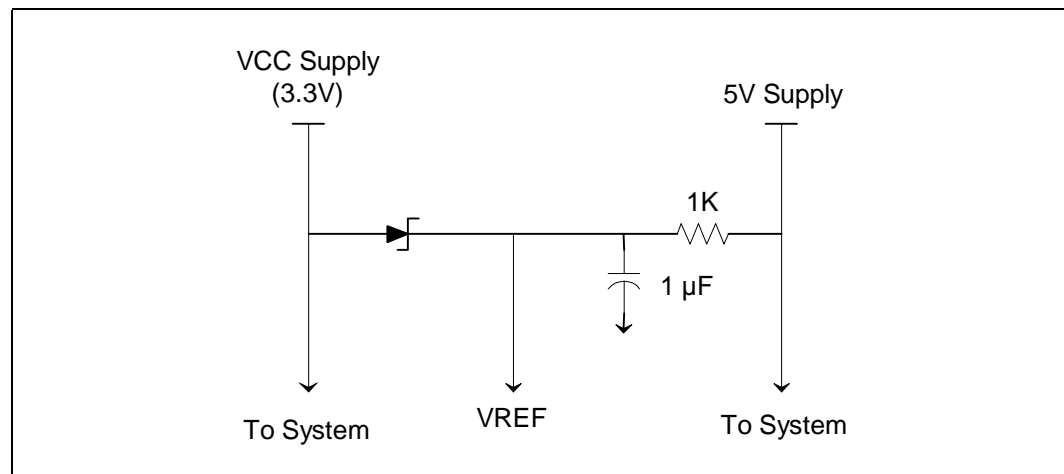
The 1.5 V voltage must be valid before the first CLK66 pulse is driven into the 6300ESB ICH. This may be ensured by gating the CK409 clocks using a power good signal from the 1.5 V regulator. When the first CLK66 pulse is driven before 1.5 V is valid, the PCI-X PLL may fail to correctly lock.

### 13.3.4.4 3.3 V/V5REF Sequencing

V5REF is the reference voltage for the 5 V tolerant input buffers on the 6300ESB ICH. V5REF must be powered up before VCC3\_3, or after VCC3\_3 within 0.7 V. Also, V5REF must also power down after VCC3\_3 or before VCC3\_3 within 0.7 V. These rules must be followed in order to ensure the safety of the 6300ESB ICH. If the rule is violated, internal diodes will attempt to draw power sufficient to damage the diodes from the VCC3\_3 rail. [Figure 155](#) shows a sample implementation of how to satisfy the V5REF/VCC3\_3 sequencing rule.

This rule also applies to V5REF\_Sus and VccSus3\_3. However, in most platforms, the VccSus3\_3 rail is derived from the 5 VSB through a voltage regulator and therefore, the VccSus3\_3 rail will always come up after the VccSus5 rail. As a result, V5REF\_Sus (which is derived directly from VccSus5) will always be powered up before VccSus3\_3 and thus circuitry to satisfy the sequence requirement is not needed. However, in platforms that do not derive the VccSus3\_3 rail from the VccSus5 rail, this rule must be observed in the platform design as described above. See [Figure 155](#).

**Figure 155. Example 3.3 V/V5REF Sequencing Circuitry**



### 13.3.4.5 ICH Power Consumption

Refer to the *Intel 6300ESB ICH Datasheet* for power consumption information (see [“Reference Documentation”](#) on page 19).

### 13.3.4.6 Thermal Design Power

For information on 6300ESB ICH thermal design refer to the *Intel 6300ESB ICH Thermal and Mechanical Design Guide* (see [“Reference Documentation”](#) on page 19).

### 13.3.4.7 ICH Power Delivery

Power delivery to the 6300ESB ICH is accomplished on several layers. The following examples are for the stack-up documented in [Section 3, “Platform Stack-Up and Placement Overview”](#) on page 34 of this document.

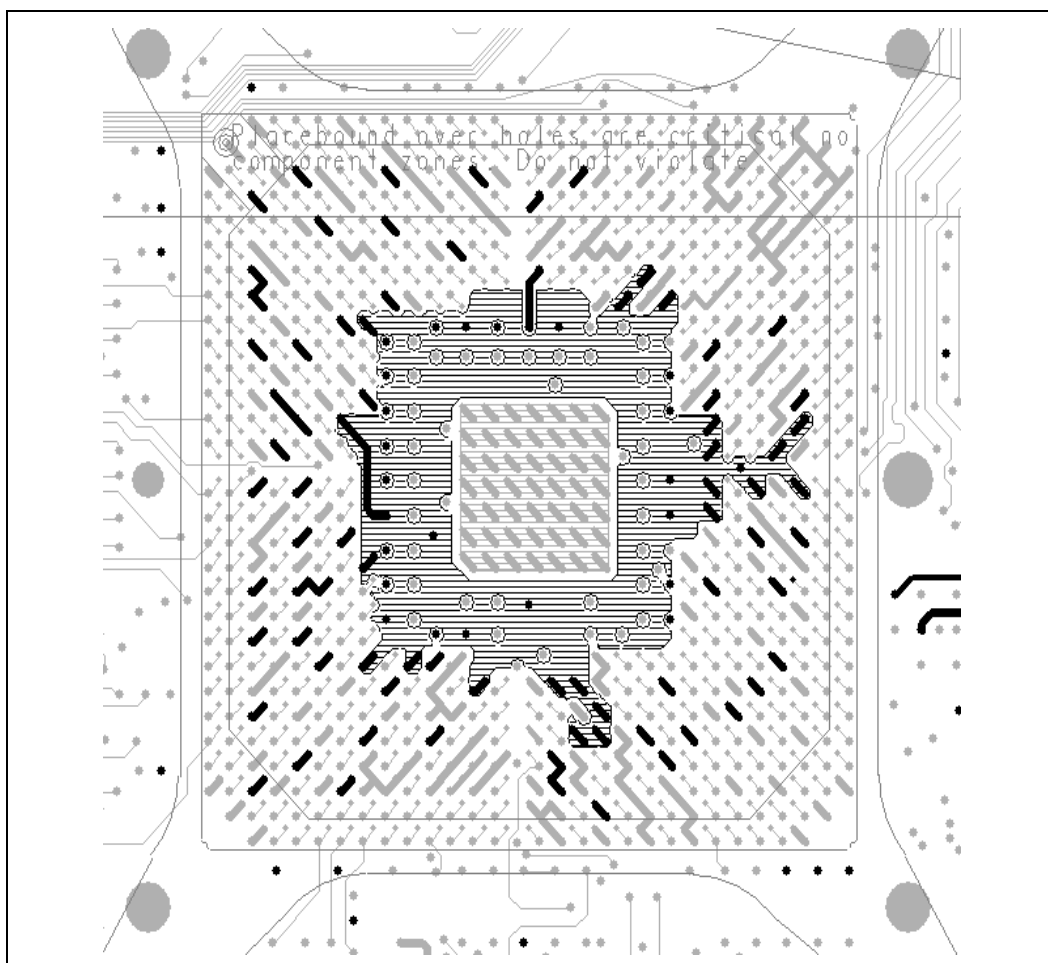
**Figure 156. Layer 1 Power Delivery (3.3 V/1.5 V)**

Figure 157. Layer 2 Power Delivery (3.3 V/GND)

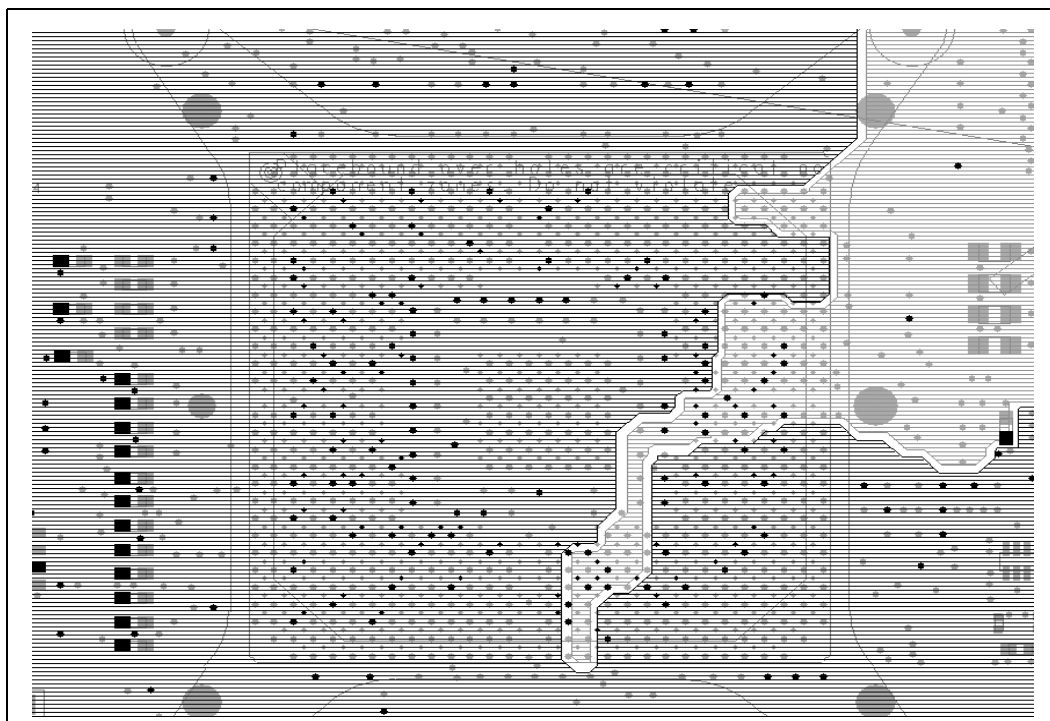
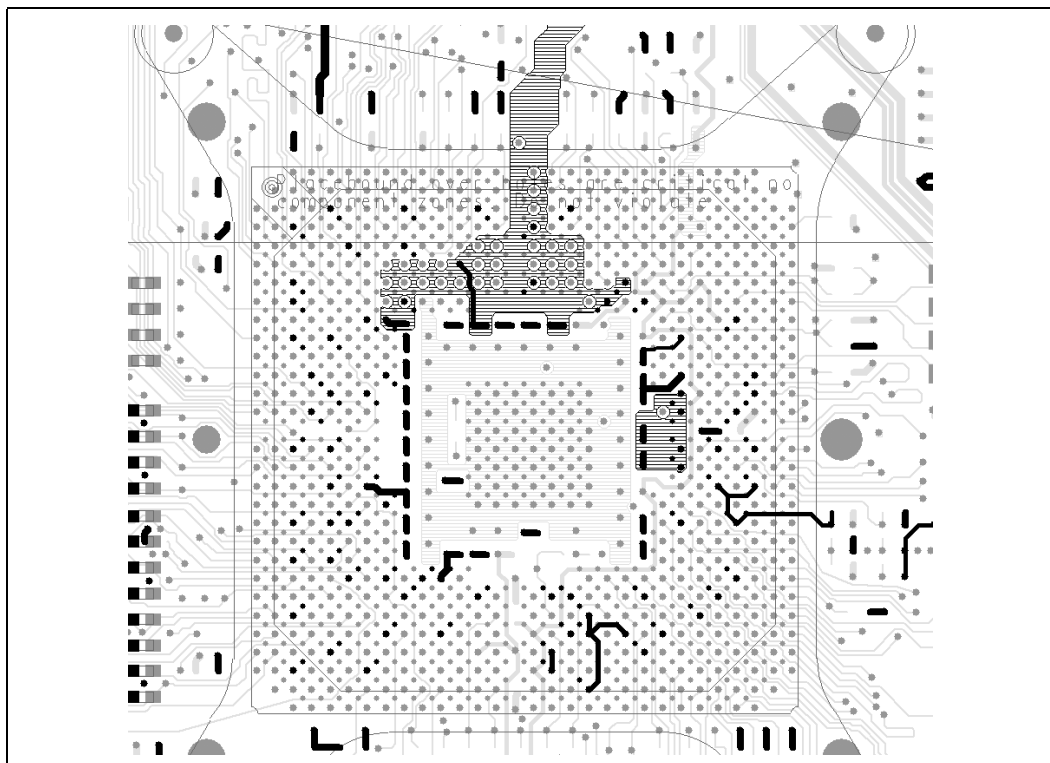


Figure 158. Layer 6 Power Delivery (1.5 V/GND)



### 13.3.4.7.1 Standby Power Distribution

To avoid radiated or conducted noise being coupling into the 6300ESB ICH through the resume wells, the standby power rails (V5REF\_Sus and VccSus3\_3) should be implemented using planes rather than traces. The planes will have the capability to absorb the noise; a trace would serve as antenna.

### 13.3.4.8 ICH Decoupling

The 6300ESB ICH is capable of generating large current swings when switching between logic high and logic low. This condition could cause the component voltage rails to drop below specified limits. To avoid this type of situation, ensure that the appropriate amount of bulk capacitance is added in parallel to the voltage input pins. It is recommended that the developer use the amount of decoupling capacitors specified in [Table 104](#) to ensure the component maintains stable supply voltages. The capacitors should be placed as close to the package as possible (100 mils nominal). It is recommended that for prototype board designs the designer include pads for extra power plane decoupling capacitors.

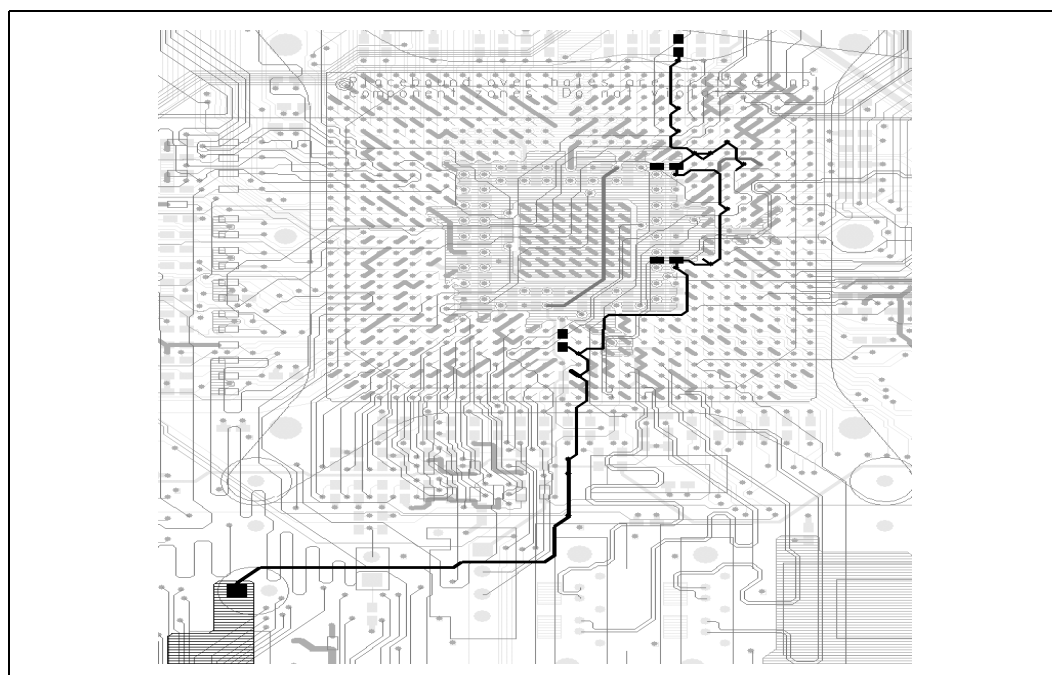
**Table 104. Decoupling Requirements**

Pin	Capacitor	Quantity	Decoupling Placement
V_CPU_IO	0.1 $\mu$ F	1	Close to pins
V <sub>CC</sub> RTC	0.1 $\mu$ F	2	One close to the 6300ESB ICH, one close to the battery
V <sub>CC</sub> 3_3	0.1 $\mu$ F 0.01 $\mu$ F	12 4	
V <sub>CC</sub> Sus3_3	0.1 $\mu$ F 0.01 $\mu$ F 1.0 $\mu$ F	4 1 1	
V <sub>CC</sub> 1_5	0.1 $\mu$ F 0.01 $\mu$ F	6 2	
V <sub>CC</sub> Sus1_5	0.1 $\mu$ F	4	
V5REF_Sus	0.1 $\mu$ F	1	
V5REF	0.1 $\mu$ F	1	
V <sub>CC</sub> PLL	0.1 $\mu$ F	3	
V <sub>CC</sub> HI	0.1 $\mu$ F	2	
VCCREF (3.3 V)	1.0 $\mu$ F	1	
VCCA	0.1 $\mu$ F	1	

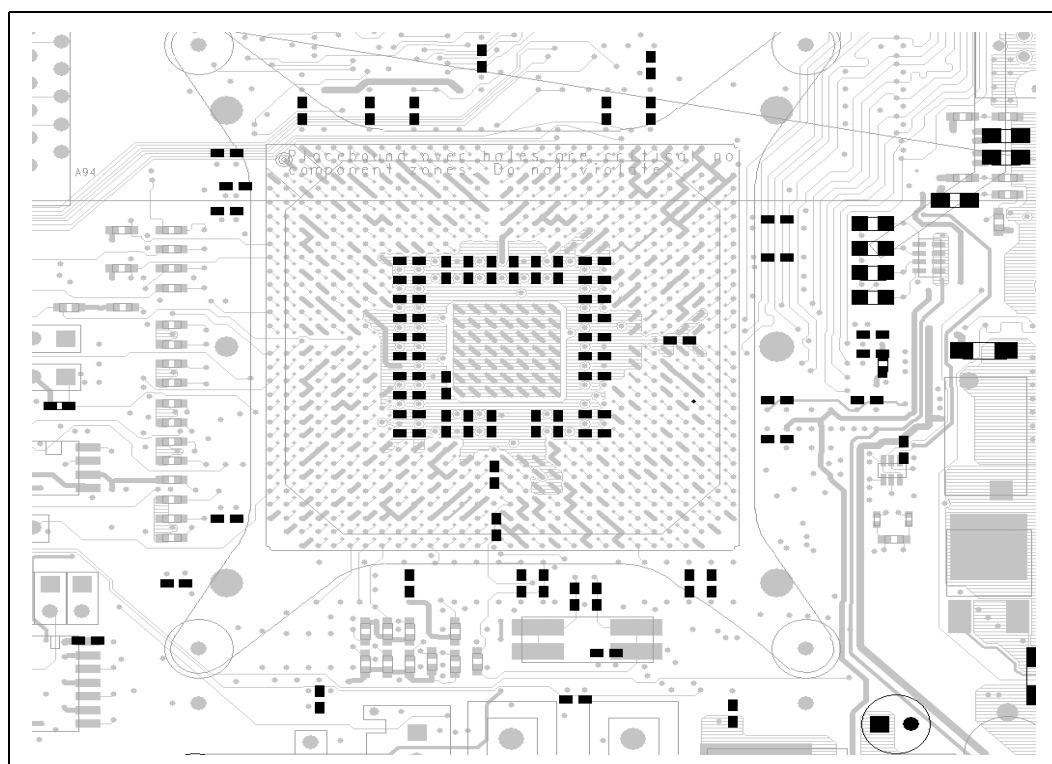
**NOTE:** Capacitors should be placed less than 100 mils from the package.



**Figure 159. Decoupling Capacitor Placement for VccSus1\_5**



**Figure 160. Example Decoupling Capacitor Placement**



## 13.3.5 DDR DIMM Power Delivery

### 13.3.5.1 2.55 V Power Delivery

2.55 V power is delivered on layers 1 and 6. On layer 1 there is room to make a copper flood under the channel B DIMMs. This copper flood forms a parallel plate capacitor with the ground plane on layer 2. Due to the ground referencing requirements for DDR, for channel A power delivery there is no room to pour a flood under the DIMM connectors, so wide power fingers are used instead. It is necessary to get as many wide power fingers on layer 6 and layer 1 as possible for clean power delivery. In order to meet DDR timings, it is important to make sure that DC resistance of the 2.55 V power plane is as low as possible. [Figure 161](#) and [Figure 162](#) show an example of this power delivery scheme.

### 13.3.5.2 1.275 V VTT Power Delivery

1.5 V VTT power is delivered on layer 1 for both the channel A and channel B DIMMs through a U-shaped power plane around the channel B DIMMs. [Figure 161](#) and [Figure 162](#) show an example of this power delivery scheme.

**Figure 161. DDR DIMMs Layer 1 Power Delivery**

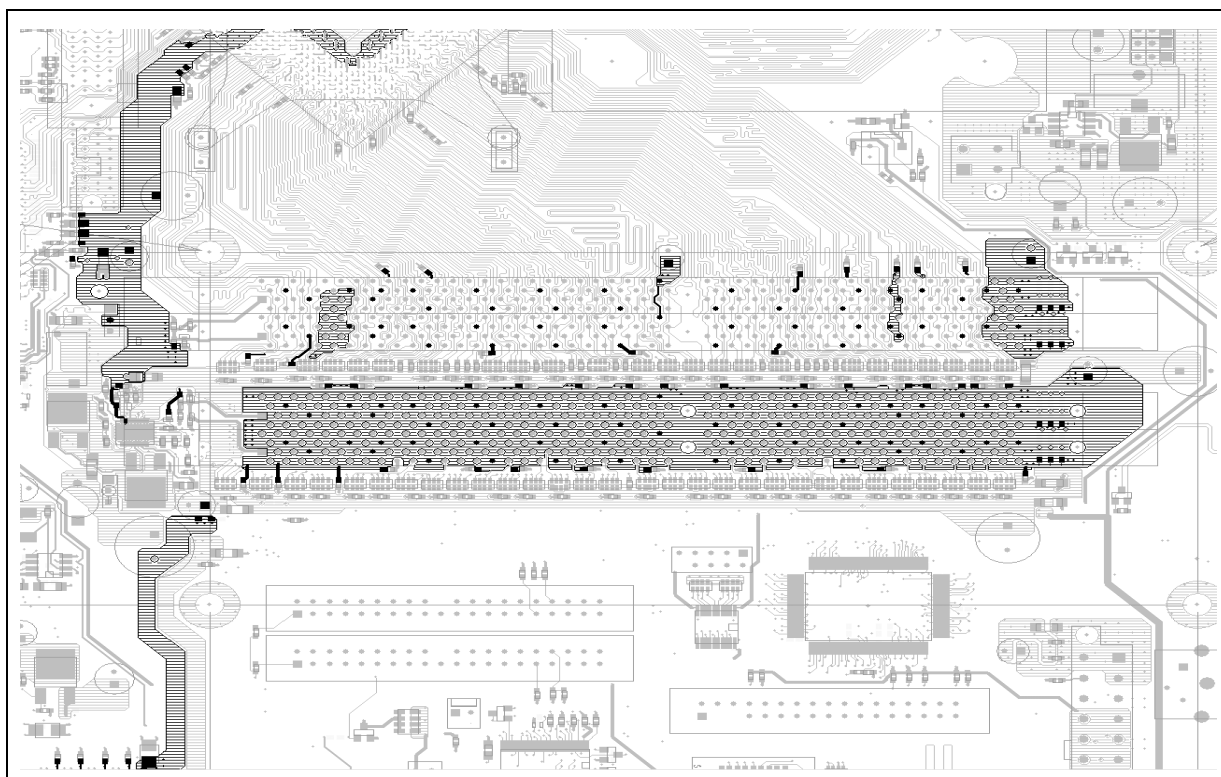
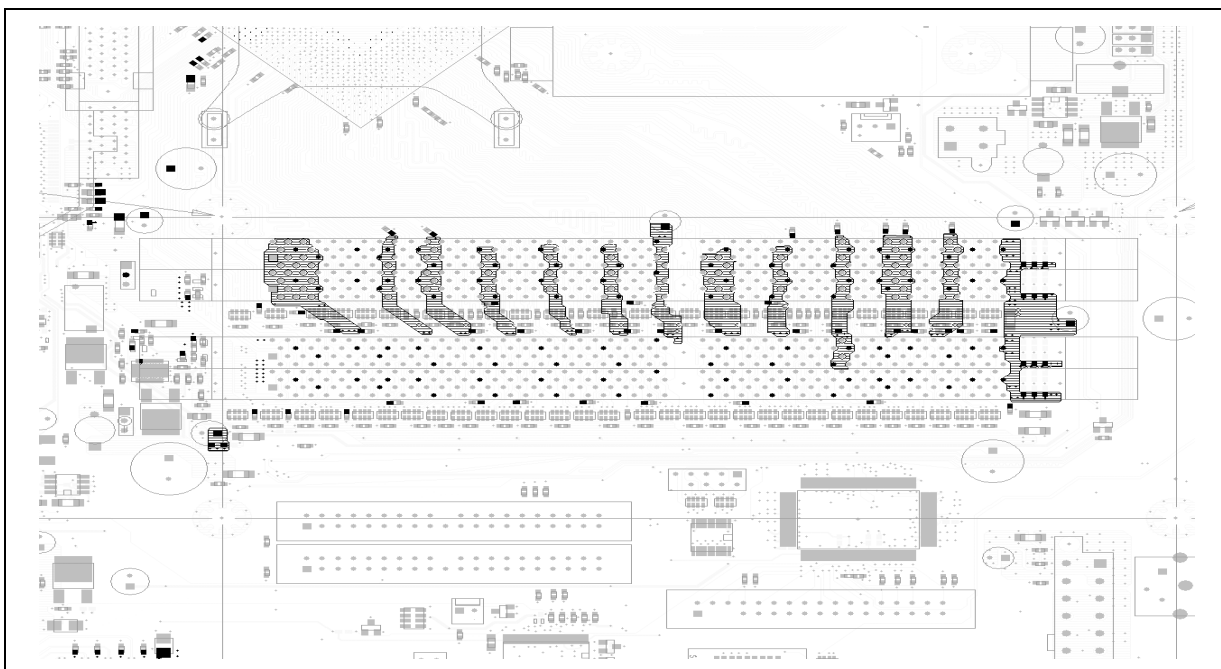


Figure 162. DDR DIMMS Layer 6 Power Delivery



### 13.3.5.3 DDR DIMMs Decoupling

Table 105. DDR DIMMs Decoupling

Pin	Decoupling Requirements	Decoupling Type (Pin Type)	Decoupling Placement
VCC_2.55	(42) 0.1 $\mu$ F	Decoupling capacitors	As close to power the DIMM power pins as possible and sprinkled through out the DDR power flood
VTT_1.275	(54) 0.1 $\mu$ F	Decoupling capacitors	As close to termination resistors as possible

Figure 163. DDR DIMM High-Speed Decoupling

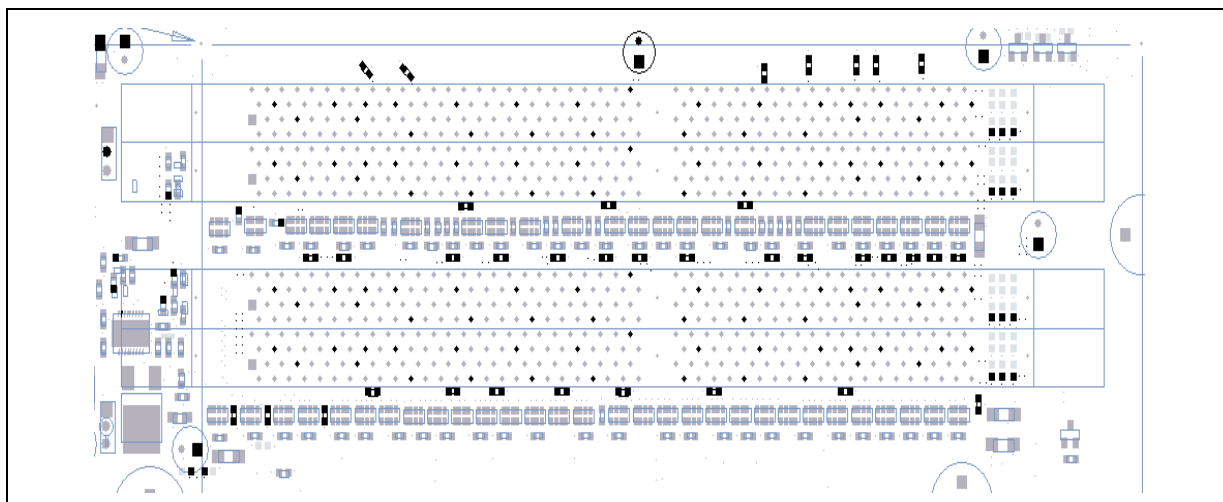
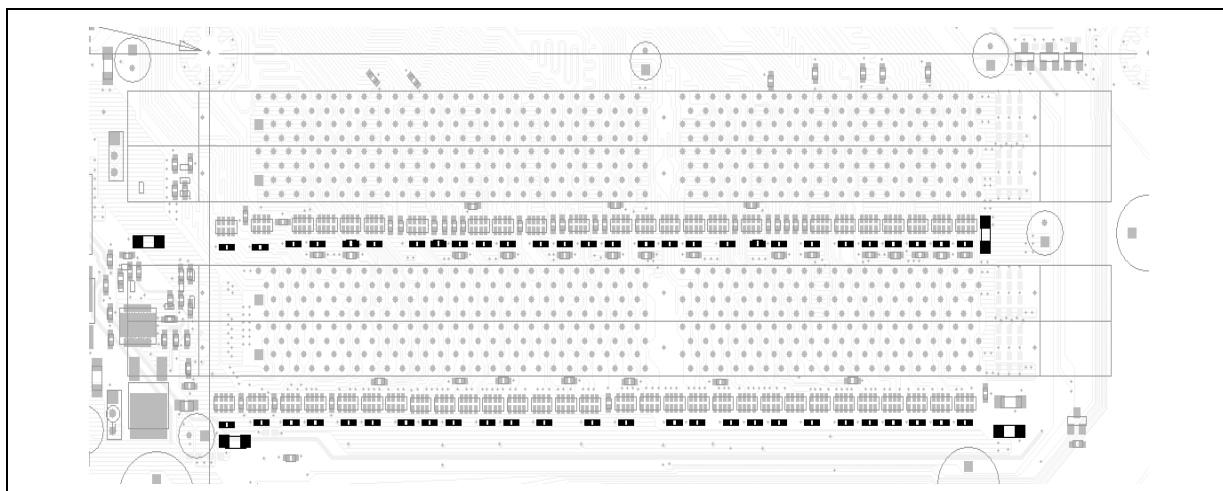


Figure 164. DDR DIMM VTT High-Speed Decoupling



# Platform Mechanical Guidelines

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# 14

## 14.1 Intel® 875P MCH/Intel® E7210 MCH Package and Retention Mechanism Keep-Outs

Refer to the *Intel 875P/E7210 MCH Chipset Thermal and Mechanical Design Guide* (see “Reference Documentation” on page 19).

# EMI Design Guidelines

# 15

**Note:** Contents specific to this platform will be added to this section in a future revision. The following are general EMI design considerations.

## 15.1 Introduction

This section is intended to provide electrical and mechanical design engineers with information that will aid in developing a platform that will meet government EMI regulations. Processor shielding, differential and spread spectrum clocking, and the test methodology impact to FCC Class B requirements are specifically discussed.

Designers should be aware that implementing all the recommendations in this guideline will not ensure compliance to EMI regulations. Rather, these guidelines may help to reduce the emissions from processors and motherboards and make chassis design easier.

### 15.1.1 Terminology

**Electromagnetic Interference (EMI)** — Electromagnetic radiation from an electrical source that interrupts the normal function of an electronic device.

**Electromagnetic Compatibility (EMC)** — The successful operation of electronic equipment in its intended electromagnetic environment.

### 15.1.2 Brief EMI Theory

Electromagnetic energy transfer may be viewed in four ways: radiated emissions, radiated susceptibility, conducted emissions, and conducted susceptibility. For system designers, reduction of radiated and conducted emissions is the way to achieve EMC compliance. Susceptibility is typically not a major concern in the server environment, although it may be more important in an industrial environment.

The main component of EMI is a radiated electromagnetic wave, which consists of both electric (E-fields) and magnetic (H-fields) waves traveling together and oriented perpendicular to one another. Although E- and H-fields are intimately tied together, they are generated by different sources. E-fields are created by voltage potentials while H-fields are created by current flow. In a steady state environment (where voltage or current is unchanging), E- and H-fields are also static and of no concern to EMI. Changing voltages and currents are of concern since they contribute to EMI. If a dynamic E-field is present, then there must be a corresponding dynamic H-field, and vice versa. Motherboards with fast processors will generate high-frequency E- and H-fields from currents and voltages present in the component silicon and signal traces.

Two methods exist for minimizing E- and H-field system emissions: prevention and containment. Prevention is achieved by implementing design techniques that minimize the ability of the motherboard to generate EMI fields. Containment is used in a chassis environment to contain

radiated energy within the chassis. Careful consideration of board layout, trace routing, and grounding may significantly reduce a motherboard's radiated emissions and make chassis design easier.

### 15.1.3 EMI Regulations and Certifications

Original Equipment Manufacturers (OEMs) ensure EMC compliance by meeting EMI regulatory requirements. System designers must ensure that their computer systems do not exceed the emission limit standards set by applicable regulatory agencies. Regulatory requirements referenced in this document include:

- United States Federal Communication Commission (FCC) Part 15 Class B
- International Electrotechnical Commission's International Special Committee on Radio Interference (CISPR) Publication 22 Class B limits

The FCC rules are viewed to require any OEM who sells an off-the-shelf motherboard in the United States to pass an open chassis test. Open chassis testing is defined as removing the chassis cover (or top and two sides) and testing for EMI compliance (although permitted emission levels are allowed to be higher). Removing the cover greatly reduces the shielding provided by the chassis and increases the amount of EMI radiation. The purpose of this regulation is to ensure that system boards have reasonable emission levels since they are one of the main contributors to EMI.

## 15.2 EMI Design Considerations

The following sections discuss design techniques that may be applied to minimize EMI emissions. Some ideas have been incorporated into Intel-enabled designs (differential clock drivers, selective clock gating, etc.) and some must be implemented by motherboard designers (trace routing, clocking schemes, etc.).

### 15.2.1 Spread Spectrum Clocking (SSC)

Spread spectrum clocking is defined as continuously ramping (or modulating) the processor clock frequency over a predefined range (see [Figure 165](#)). SSC reduces radiated emissions by spreading the radiated energy over a wider frequency band (see [Figure 166](#)). Thus, instead of maintaining a constant system frequency, SSC modulates the clock frequency along a predetermined path (or modulating profile). [Figure 165](#) shows an example of a predetermined modulation frequency. The modulation frequency is usually selected to be larger than 30 kHz (above the audio band) while small enough not to upset system timings (less than 0.8% of the clock frequency). SSC has been demonstrated to effectively reduce peak radiation levels, making EMC compliance easier to achieve.

To conserve the minimum period requirement for bus timing, the SSC clock is modulated between  $f_{nom}$  and  $(1-\delta)*f_{nom}$  where  $f_{nom}$  is the nominal frequency for a constant frequency clock. The " $\delta$ " specifies the total amount of spreading as a relative percentage of  $f_{nom}$ . The modulation percentage is always a function of  $1-\delta$  and not  $1+\delta$ , as increasing the clock frequency above the rated speed of the processor may cause unpredictable operation.

Figure 165. Spread Spectrum Modulation Profile

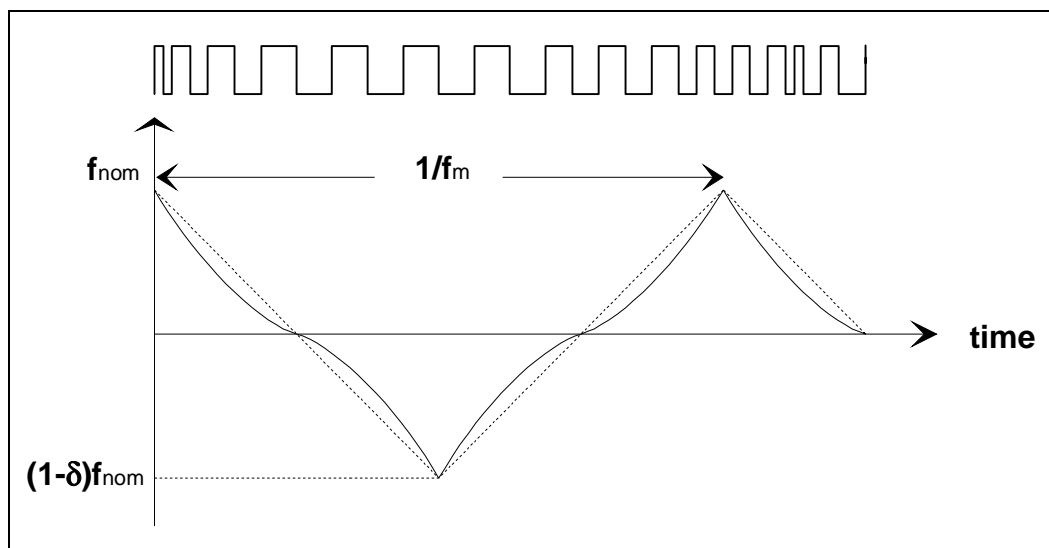
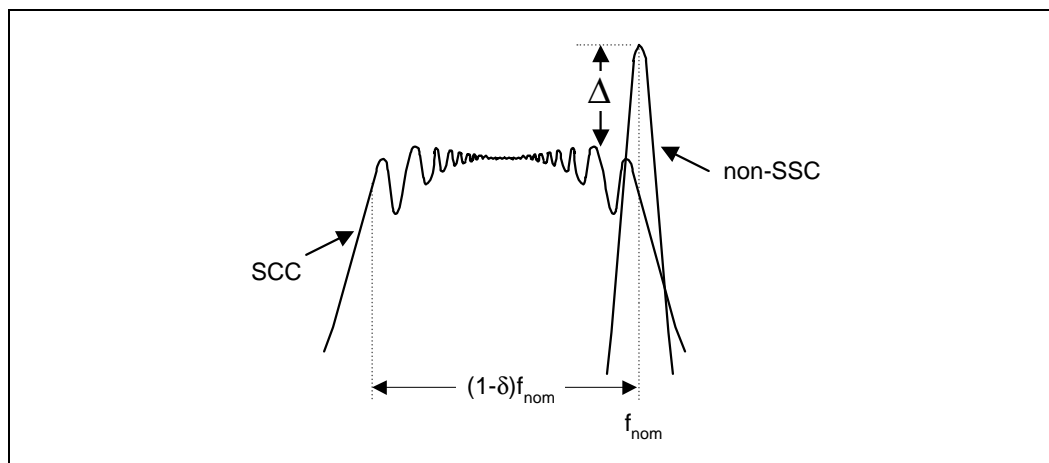


Figure 166. Impact of Spread Spectrum Clocking on Radiated Emissions



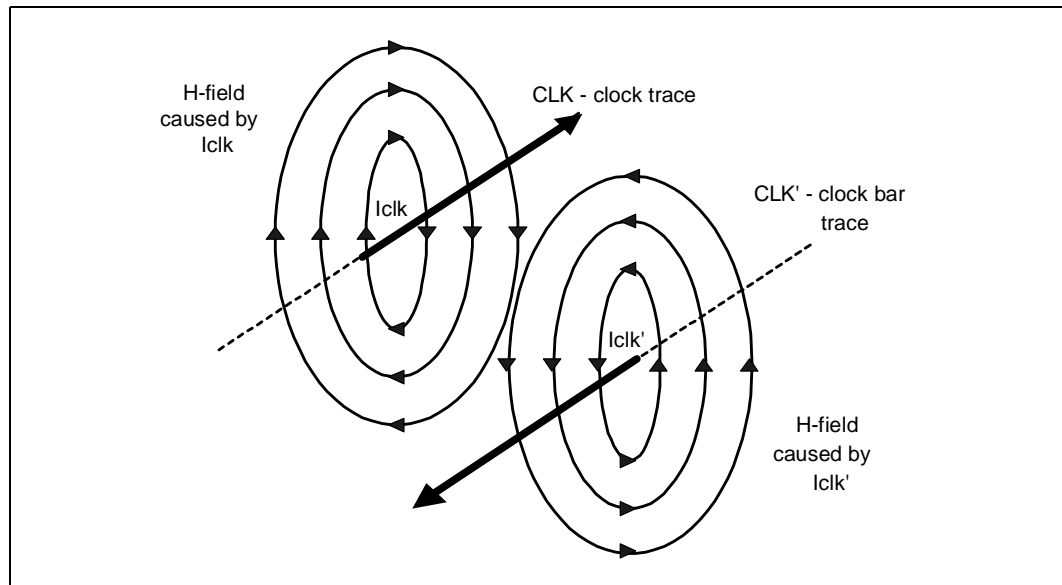
## 15.2.2 Differential Clocking

Differential clocking requires that the clock generator supply both clock and clock-bar traces. Clock-bar has equal and opposite current as the primary clock and is also 180 degrees out of phase. To maximize the benefit of differential clocking, both clock lines must be routed parallel to each other for their entire length. Devices connected to the clock must also be designed to accept both the clock and clock-bar signals.

EMI reduction due to differential clocking is caused by H-field cancellation. Since H-field orientation is generated by and is dependent upon current flow, two equal currents flowing in opposite directions and 180 degrees out of phase will have their H-fields cancelled (see [Figure 167](#)). Lower H-fields will result in reduced EMI radiation.



**Figure 167. Cancellation of H-fields Through Inverse Currents**



Differential clocking may also reduce the amount of noise coupled to other traces, which improves signal quality and reduces EMI. I/O signals are particularly important because they often leave the system chassis (serial and parallel ports, keyboards, mouse, etc.) and will radiate noise that has been induced onto them. A single-ended clock's return path is usually a reference plane, which is shared by other signals/traces. When noise is created on a single-ended clock, the noise will appear on the reference plane and may be coupled to I/O traces. A differential clock's return path is the clock-bar signal/trace, which is more isolated than the reference plane and minimizes potential I/O trace coupling.

For best results, the trace lengths and routing of the clock lines must be closely matched and spacing between the two traces should be kept as small as possible. This will minimize loop area and maximize H-field cancellation. In addition, the real and parasitic terminations of each signal of a differential pair should be the same. Also, the skew between the signal level transitions on the two lines must be small compared to the rise time of the level transitions.

Placing ground traces on the outside of the differential pair may further reduce emissions. Intermediate vias to ground may be needed to reduce the opportunity for re-radiation from the ground traces themselves. Distance between vias should be less than  $\frac{1}{4}$  of a wavelength of the fifth harmonic of the processor core frequency.

## 15.2.3 PCI Bus Clock Control

Experimental data has indicated a reduction in EMI may be possible by disabling the clocks to unused (and therefore unterminated) PCI slots. CK409, the clock chip that has been specified and designed for this platform, supports individual control of the various PCI clocks. Designers have the option to enable or disable individual PCI clocks depending upon their specific system configuration requirements. Refer to the *CK409 Clock Synthesizer Design Guidelines* for details on how to configure the PCI clocks.

## 15.2.4 EMI Test Capabilities

FCC regulations in the United States specify the maximum test frequency for products with clocks in excess of 1 GHz is five times the highest clock frequency or 40 GHz, whichever is lower. OEMs are advised to inquire into the capabilities of their preferred EMC test lab to ensure they are able to scan up to the required frequency range.

History indicates that processor performance and frequency double approximately every two years. With this in mind, it would be advisable to be prepared for the frequencies that will need to be scanned in the next few years.

Since the FCC rules ultimately require testing to 40 GHz, commercial test equipment has been developed which is capable of making measurements to that frequency. Although it will be some time before processors require testing at this frequency, it may be cheaper to upgrade to 40 GHz now rather than making several intermediate steps.

It is also possible to upgrade various parts at different times. The spectrum analyzer may be upgraded to 40 GHz today while only obtaining the necessary antennas to support the initial processor frequencies. As processor speed increases, the necessary antennas and cables could be purchased which would support testing to the higher levels. Cost flexibility in antenna selection is probably the greatest, since different antenna designs are necessary for different frequency ranges.

# Schematic Checklist

# 16

## 16.1 Introduction

This checklist highlights design considerations that should be reviewed prior to manufacturing a motherboard that implements the 875P MCH/E7210 MCH/6300ESB ICH chipset. Refer to the most recent version of the platform design guide for more detailed instructions on designing a motherboard.

## 16.2 Processor Interface

### 16.2.1 CPU Connector/MCH Items

**Table 106. CPU Connector/MCH Items (Sheet 1 of 2)**

Checklist Items	Connections/Recommendations	Reason/Impact
ADS#	Connect to ADS# pin on the MCH. No other termination required.	AGTL+ Common Clock I/O signal
BNR#	Connect to BNR# pin on the MCH. No other termination required.	AGTL+ Common Clock I/O signal
BPRI#	Connect to BPRI# pin on the MCH. No other termination required.	AGTL+ Common Clock Input signal
BR0#	Connect to BREQ0# pin on the MCH. Terminate to V_CPU_IO through a $200\ \Omega \pm 5\%$ resistor external pull-up.	The chipset contains on-die termination for the BREQ0# signal. The processor does not contain on-die termination for this particular AGTL+ signal; thus external termination is required only on the processor end. AGTL+ Common Clock I/O signal. Refer to <a href="#">Section 5.1.6.4</a> .
RESET#	Connect to the CPURST# on the MCH. Terminate to V_CPU_IO through a $62\ \Omega \pm 5\%$ resistor near the processor. $150\ \Omega \pm 5\%$ series resistor to the ITP.	The chipset contains on-die termination for the CPURST# signal. The processor does not contain on-die termination for this particular AGTL+ signal; thus external termination is required only on the processor end. RESET# termination should equal the resistance value of on die AGTL+ termination resistance (Rtt) value. AGTL+ Common Clock Input signal. Refer to <a href="#">Section 5.1.6.4</a> .
DBSY#	Connect to DBSY# pin on the MCH. No other termination required.	AGTL+ Common Clock I/O signal.
DEFER#	Connect to DEFER# pin on the MCH. No other termination required.	AGTL+ Common Clock Input signal.

Table 106. CPU Connector/MCH Items (Sheet 2 of 2)

Checklist Items	Connections/Recommendations	Reason/Impact
DBI[3:0]#	Connect to DINV[3:0]# pin on the MCH. No other termination required.	AGTL+ Source Synch I/O signal
DRDY#	Connect to DRDY# pin on the MCH. No other termination required.	AGTL+ Common Clock I/O signal
A[31:3]#	Connect to HA[31:3]# pins on MCH. No other termination required.	Chipset does not support extended addressing over 4 GBytes, leave A[35:32]# unconnected. AGTL+ Source Synch I/O signal
ADSTB[1:0]#	Connect to HADSTB[1:0]# pins on MCH. No other termination required.	AGTL+ Source Synch I/O signal
D[63:0]#	Connect to HD[63:0]# pins on MCH. No other termination required.	AGTL+ Source Synch I/O signal
DSTBP[3:0]#	Connect to HDSTBP[3:0]# pins on MCH. No other termination required.	AGTL+ Source Synch I/O signal
DSTBN[3:0]#	Connect to HDSTBN[3:0]# pins on MCH. No other termination required.	AGTL+ Source Synch I/O signal
HIT#	Connect to HIT# pin on MCH. No other termination required.	AGTL+ Common Clock I/O signal
HITM#	Connect to HITM# pin on MCH. No other termination required.	AGTL+ Common Clock I/O signal
LOCK#	Connect to HLOCK# pin on MCH. No other termination required.	AGTL+ Common Clock I/O signal
REQ[4:0]#	Connect to HREQ[4:0]# pin on MCH. No other termination required.	AGTL+ Source Synch I/O signal
TRDY#	Connect to HTRDY# pin on MCH. No other termination required.	AGTL+ Common Clock Input signal
PROCHOT#	Connect to PROCHOT# on VRD and MCH. Terminate to V_CPU_IO through a 120 $\Omega$ —140 $\Omega$ $\pm$ 5% resistor	Asynch GTL+ Input/Output signal Refer to <a href="#">Section 5.1.6.7</a>
RS[2:0]#	Connect to RS[2:0]# pin on the MCH. No other termination required.	AGTL+ Common Clock Input signal

## 16.2.2 CPU Connector/ICH Items

Checklist Items	Connections/Recommendations	Reason/Impact
A20M#	Connect to A20M# pin on the 6300ESB ICH. No other termination required.	Asynch GTL + Input signal. Refer to <a href="#">Section 5.1.6.2</a> .
FERR#	Connect to FERR# pin on the 6300ESB ICH. Terminate to V_CPU_IO through a $62\ \Omega \pm 5\%$ resistor near 6300ESB ICH.	This output signal is not terminated on the processor. Termination is required on system board. Asynch GTL + Output signal. Refer to <a href="#">Section 5.1.6.1</a> .
IGNNE#	Connect to IGNNE# pin on the 6300ESB ICH. No other termination required.	Asynch GTL + Input signal. Refer to <a href="#">Section 5.1.6.2</a> .
INIT#	Connect to INIT# pin on the 6300ESB ICH and to FWH through voltage translation. Level shifting is required to meet the input logic levels of the flash BIOS.	Asynch GTL + Input signal. Refer to <a href="#">Section 5.1.6.5</a> .
LINT[1:0]	LINT[0]/INTR connects to INTR on 6300ESB ICH. LINT[1]/NMI connects to NMI on 6300ESB ICH. No other termination required.	Asynch GTL + Input signal. Refer to <a href="#">Section 5.1.6.2</a> .
PWRGOOD	CPU, MCH, and 6300ESB ICH power supplies are ANDed together. Terminate to V_CPU_IO through a $300\ \Omega \pm 5\%$ resistor near the processor. May be implemented using Glue Chip 4* logic.	Asynch GTL + Input signal. Refer to <a href="#">Section 5.1.6.6</a> .
SLP#	Connect to CPUSLP# on the 6300ESB ICH. No other termination required.	Asynch GTL + Input signal. Refer to <a href="#">Section 5.1.6.2</a> .
SMI#	Connect to SMI# pin on the 6300ESB ICH. No other termination required.	Asynch GTL + Input signal. Refer to <a href="#">Section 5.1.6.2</a> .
STPCLK#	Connect to STPCLK# pin on the 6300ESB ICH. No other termination required.	Asynch GTL + Input signal. Refer to <a href="#">Section 5.1.6.2</a> .

## 16.2.3 CPU Connector Only Items

Table 107. CPU Connector Only Items (Sheet 1 of 3)

Checklist Items	Connections/Recommendations	Reason/Impact
A[35:32]#	No Connect	Chipset does not support extended addressing over 4 GBytes. Leave A[35:32]# unconnected. AGTL+ Source Synch I/O.
AP[1:0]#	No Connect if unused.	Chipset does not support parity protection on the address bus. AGTL+ Common Clock I/O signal.
BCLK0	Connect to CPU0 on the CK409 through a $33\ \Omega \pm 5\%$ series resistor. Terminate to GND through a $49.9\ \Omega \pm 1\%$ resistor.	System Bus Clock signal. Refer to <a href="#">Section 4.1.1</a> .
BCLK1	Connect to CPU0# on the CK409 through a $33\ \Omega \pm 5\%$ series resistor. Terminate to GND through a $49.9\ \Omega \pm 1\%$ resistor.	System Bus Clock signal. Refer to <a href="#">Section 4.1.1</a> .
BOOTSELECT	Connect to dual loadline select circuitry.	Refer <a href="#">Section 5.1.6.10</a> .
BPM[5:0]#	Connect to BPM[5:0] on the ITP header Terminate to V_CPU_IO through a $62\ \Omega \pm 5\%$ resistor place near the processor. Pull up to V_CPU_IO using a $20\ \Omega - 1\ \text{k}\Omega$ resistor if no interposer support	AGTL+ Common Clock I/O signal.
BINIT#	No Connect if unused.	Chipset does not support this signal. AGTL+ Common Clock I/O signal.
BSEL[0]	Connect to MCH's SEL0 pin and FSA pin on CK409. 1 k $\Omega$ pull-up to 3.3 V required at CK409. MCH requires divider for 1.5 V tolerant inputs	Refer <a href="#">Section 5.1.6.18</a> .
BSEL[1]	Connect to MCH's SEL1 pin and FSB pin on CK409. 1 k $\Omega$ pull-up to 3.3 V required at CK409. MCH requires divider for 1.5 V tolerant inputs	Refer <a href="#">Section 5.1.6.18</a> .
COMP[1:0]	Terminate to GND through a $61.9\ \Omega \pm 1\%$ resistor. Minimize the distance from termination resistor and CPU pin.	Refer to <a href="#">Section 5.1.6.9</a> .
DBR#	Connect to front panel header and switches. 8.2 k $\Omega$ pull-up to VCC Sus3_3 near 6300ESB ICH and connect to system reset logic (front-panel reset) and ITP. May be left No Connect for no interposer support	
DP#[3:0]	No Connect if unused.	Chipset does not support parity protection on the data bus. AGTL+ Common Clock I/O signal.

**Table 107. CPU Connector Only Items (Sheet 2 of 3)**

Checklist Items	Connections/Recommendations	Reason/Impact
IERR#	No Connect if unused. Terminate to V_CPU_IO through a $62\ \Omega \pm 5\%$ resistor from the processor if used.	Asynch GTL + Output signal. Refer to <a href="#">Section 5.1.6.3</a>
GTLREF[3:0]	Connect to a resistor divider consisting of a $200\ \Omega \pm 1\%$ pull-up to V_CPU_IO and a $169\ \Omega \pm 1\%$ pull-down to GND and connect to pin F15 (HDVREF0) of the MCH. Decouple with a $0.1\ \mu\text{F}$ or $1.0\ \mu\text{F}$ at the voltage divider circuit, and through a $220\ \text{pF}$ at the CPU pin. Connect $0.63 \times \text{VCC\_AVG}$ divider to one of the 4 GTLREF pins. Others are NC.	Refer to <a href="#">Section 5.1.6.13</a> .
ITP_CLK0	Connect to CPU1# on CK409 through a $33\ \Omega \pm 5\%$ resistor. Terminate to GND through a $49.9\ \Omega \pm 1\%$ resistor. Connect to NC for no interposer support.	System Bus Clock signal.
ITP_CLK1	Connect to CPU1# on CK409 through a $33\ \Omega \pm 5\%$ resistor. Terminate to GND through a $49.9\ \Omega \pm 1\%$ resistor. Connect to NC for no interposer support.	System Bus Clock signal.
OPTIMIZED / COMPAT# (Pentium 4 processor with HT Technology) IMPSEL (Pentium 4 Processor)	No Connect	
MCERR#	No Connect if unused.	Chipset does not support this signal.
RSP#	No Connect if unused.	Chipset does not support this signal. AGTL+ Common Clock Input signal.
SKTOCC#	Connect to CPU_PRESENT# pin on the GlueChip4. Depends on customer need.	
TCK	Connect to TCK on ITP. $27.4\ \Omega \pm 1\%$ pull-down to GND near ITP and $47\ \Omega \pm 5\%$ pull-down to GND near processor for ITP-USB. Pull down to VSS using a $20\ \Omega - 1\ \text{k}\Omega$ resistor if no interposer support.	TAP Input signal— refer to the <i>Intel Pentium 4 Processor with HT Technology<sup>1</sup> Debug Port Design Guide</i>
TDI	Connect to TDI on ITP. Terminate to V_CPU_IO through a $150\ \Omega \pm 5\%$ resistor near the processor. Pull up to V_CPU_IO using a $20\ \Omega - 1\ \text{k}\Omega$ resistor if no interposer support.	TAP Input signal— refer to the <i>Intel Pentium 4 Processor with HT Technology Debug Port Design Guide</i>
TDO	Connect to TDO on ITP. Terminate to V_CPU_IO through $51\ \Omega \pm 5\%$ resistor near $47\ \Omega \pm 5\%$ series resistor to ITP. May be left No Connect if no interposer support.	TAP Output signal.
TESHI[12:0]	Terminate to V_CPU_IO through $62\ \Omega \pm 5\%$ resistor. TESHI[7:2] and TESI[1:0] may be grouped together.	Refer to <a href="#">Section 5.1.6.8</a> .

Table 107. CPU Connector Only Items (Sheet 3 of 3)

Checklist Items	Connections/Recommendations	Reason/Impact
THERMTRIP#	Connect to THRMTRIP# pin on the 6300ESB ICH. Terminate to V_CPU_IO through a $62\ \Omega \pm 5\%$ resistor near the 6300ESB ICH.	Asynch GTL + Output signal. Refer to <a href="#">Section 5.1.6.1</a> .
THERMDA	Connect to REMOTE1+ on HECETA. Connect to external diode monitoring circuit if used.	Refer to <a href="#">Section 5.1.6.15</a> .
THERMDC	Connect to REMOTE1- / NTESTIN on HECETA. Connect to external diode monitoring circuit if used.	Refer to <a href="#">Section 5.1.6.15</a> .
TMS	Connect to TMS pin on the ITP. $39.2\ \Omega \pm 1\%$ pull-up to V_CPU_IO near ITP and $47\ \Omega \pm 5\%$ pull-up to V_CPU_IO near processor for ITP-USB. Pull up to V_CPU_IO using a $20\ \Omega - 1\ \text{k}\Omega$ resistor if no interposer support	TAP Input signal.
TRST#	Connect to TRST pin on the ITP connect. Terminate to GND through $510\ \Omega \sim 680\ \Omega \pm 5\%$ resistor. Pull down to V_CPU_IO using a $20\ \Omega - 1\ \text{k}\Omega$ resistor if no interposer support	TAP Input signal.
VCCA	Connect to PLL supply filter.	Refer to <a href="#">Section 13.3.1.7</a> .
RESERVED	All pins must remain unconnected.	Refer to <a href="#">Section 5.1.6.11</a> .
VCCIOPLL	Connect to PLL supply filter.	Refer to <a href="#">Section 13.3.1.7</a> .
VCCSENSE	Connect to VR control silicon if used.	Refer to <a href="#">Figure 135</a> .
VCCVID	Connect to CPU VREGn.	Refer to <a href="#">Section 13.3.1.6</a> .
VID[5:0]	Connect to VR control silicon and possibly hardware monitor circuitry. Requires $1\ \text{k}\Omega \pm 5\%$ pull-up to 3.3 V.	Refer to <a href="#">Section 5.1.6.14</a> .
VIDPWRGD	Connect to power good output of the 1.2 V linear supply with a $2.43\ \text{k}\Omega$ pull-up.	
VSSA	Connect to PLL supply filter.	Refer to <a href="#">Section 13.3.1.7</a> .
VSSSENSE	Connect to VR control silicon if used.	Refer to <a href="#">Figure 135</a>



## 16.3 MCH Interface

### 16.3.1 MCH / FSB Items

Checklist Items	Connections/Recommendations	Reason/Impact
ADS#	Connect to ADS# pin on the CPU.	
BNR#	Connect to BNR# pin on the CPU.	
BPRI#	Connect to BPRI# pin on the CPU.	
BREQ0#	Connect to BR0# pin on the CPU. Terminate to V_CPU_IO through a 200 $\Omega$ $\pm$ 5% resistor near the processor.	Refer to <a href="#">Section 5.1.6.4</a> .
CPURST#	Connect to the RESET# on the CPU. Terminate to V_CPU_IO through a 62 $\Omega$ $\pm$ 5% resistor near the processor.	Refer to <a href="#">Section 5.1.6.4</a> .
DBSY#	Connect to DBSY# pin on the CPU.	
DEFER#	Connect to DEFER# pin on the CPU.	
DINV[3:0]#	Connect to DBI[3:0]# pin on the CPU.	
DRDY#	Connect to DRDY# pin on the CPU.	
HA[31:3]#	Connect to A[31:3]# pins on CPU.	
HADSTB[1:0]#	Connect to ADSTB[1:0]# pins on CPU.	
HD[63:0]#	Connect to D[63:0]# pins on CPU.	
HDSTBP[3:0]#	Connect to DSTBP[3:0]# pins on CPU.	
HDSTBN[3:0]#	Connect to DSTBN[3:0]# pins on CPU.	
HIT#	Connect to HIT# pin on CPU.	
HITM#	Connect to HITM# pin on CPU.	
HLOCK#	Connect to LOCK# pin on CPU.	
HREQ[4:0]#	Connect to REQ[4:0]# pin on CPU.	
HTRDY#	Connect to TRDY# pin on CPU.	
PROCHOT#	Connect to PROCHOT# on VRD and CPU. Pull-up to V_CPU_IO through a 120 $\Omega$ - 140 $\Omega$ $\pm$ 5% resistor.	Refer to <a href="#">Section 5.1.6.7</a> .
RS[2:0]#	Connect to RS[2:0]# pin on CPU.	

## 16.3.2 MCH / FSB Only Items

Checklist Items	Connections/Recommendations	Reason/Impact
HCLKN	Connect to CPU2# in CK409. Connect to a series $33\ \Omega \pm 5\%$ resistor and terminate to GND through a $49.9\ \Omega \pm 1\%$ resistor.	
HCLKP	Connect to CPU2 in CK409. Connect to a series $33\ \Omega \pm 5\%$ resistor and terminate to GND through a $49.9\ \Omega \pm 1\%$ resistor.	
HDVREF0 (pin F15)	Connect voltage divider through $200\ \Omega$ pull-up to VCC_CPU and to GND through a $169\ \Omega$ resistor and connect to GTLREF of the CPU. Decouple with a $0.1\ \mu\text{F}$ or $1.0\ \mu\text{F}$ capacitor as close to the MCH as possible and a $220\ \text{pF}$ as close as possible to the CPU.	Refer to <a href="#">Section 5.1.6.13</a> .
HDVREF1 (pin A7)	Pull-up to MCH_VTT through a $200\ \Omega$ resistor and decouple with a $0.1\ \mu\text{F}$ or a $220\ \text{pF}$ capacitor as close as possible to the MCH.	Refer to <a href="#">Section 5.1.6.13</a> .
HDRCOMP	Pull-down to GND through a $20\ \Omega \pm 1\%$ resistor.	Refer to <a href="#">Section 5.1.6.16</a> .
HDSWING	Connect voltage divider circuit to MCH_VTT through a $301\ \Omega \pm 1\%$ pull-up resistor and to GND through a $102\ \Omega \pm 1\%$ pull-down resistor. Decouple voltage divider with a $0.01\ \mu\text{F}$ at the pin of the MCH.	Refer to <a href="#">Section 5.1.6.17</a> .
PWROK	Connect PWRGD_3V on the Gluechip 4.	
BSEL[1:0]	For a voltage divider with the BSEL[1:0] to the CPU, use a $2\ \text{k}\Omega$ resistor from power to the BSEL line and a $2.49\ \text{k}\Omega$ resistor from BSEL to GND.	Refer to <a href="#">Section 5.1.6.18</a> .

## 16.3.3 MCH / DDR-A Items

Table 108. MCH / DDR-A Items (Sheet 1 of 2)

Checklist Items	Connections/Recommendations	Reason/Impact
SCMDCLK_A0	Connect to CK0P in DIMM0.	Refer to <a href="#">Section 6.6.2</a> .
SCMDCLK_A0#	Connect to CK0N in DIMM0.	Refer to <a href="#">Section 6.6.2</a> .
SCMDCLK_A1	Connect to CK1 in DIMM0.	Refer to <a href="#">Section 6.6.2</a> .
SCMDCLK_A1#	Connect to CK1# in DIMM0.	Refer to <a href="#">Section 6.6.2</a> .
SCMDCLK_A2	Connect to CK2 in DIMM0.	Refer to <a href="#">Section 6.6.2</a> .
SCMDCLK_A2#	Connect to CK2# in DIMM0.	Refer to <a href="#">Section 6.6.2</a> .
SCMDCLK_A3	Connect to CK0P in DIMM1.	Refer to <a href="#">Section 6.6.2</a> .
SCMDCLK_A3#	Connect to CK0N in DIMM1.	Refer to <a href="#">Section 6.6.2</a> .
SCMDCLK_A4	Connect to CK1 in DIMM1.	Refer to <a href="#">Section 6.6.2</a> .
SCMDCLK_A4#	Connect to CK1# in DIMM1.	Refer to <a href="#">Section 6.6.2</a> .
SCMDCLK_A5	Connect to CK2 in DIMM1.	Refer to <a href="#">Section 6.6.2</a> .
SCMDCLK_A5#	Connect to CK2# in DIMM1.	Refer to <a href="#">Section 6.6.2</a> .

**Table 108. MCH / DDR-A Items (Sheet 2 of 2)**

Checklist Items	Connections/Recommendations	Reason/Impact
SMA_A[12:0]	Connect to A[12:0] on DIMM0 and DIMM1. Terminate to DDR_TERM through a $47\ \Omega \pm 5\%$ resistor.	Refer to <a href="#">Section 6.6.4</a> .
SBA_A[1:0]	Connect to BA[1:0] pin on both DIMM0 and DIMM1. Terminate to DDR_TERM through a $47\ \Omega \pm 5\%$ resistor.	Refer to <a href="#">Section 6.6.4</a> .
SRAS_A#	Connect to RAS# pin on both DIMM0 and DIMM1. Terminate to DDR_TERM through a $47\ \Omega \pm 5\%$ resistor.	Refer to <a href="#">Section 6.6.4</a> .
SCAS_A#	Connect to CAS# pin on both DIMM0 and DIMM1. Terminate to DDR_TERM through a $47\ \Omega \pm 5\%$ resistor.	Refer to <a href="#">Section 6.6.4</a> .
SWE_A#	Connect to WE# pin on both DIMM0 and DIMM1. Terminate to DDR_TERM through a $47\ \Omega \pm 5\%$ resistor.	Refer to <a href="#">Section 6.6.4</a> .
SDQ_A[63:0]	Connect to SDQ[63:0] on both DIMM0 and DIMM1. Terminate to DDR_TERM through a $56\ \Omega \pm 5\%$ resistor.	Refer to <a href="#">Section 6.6.5</a> .
SDQS_A[8:0]	Connect to SDQS[8:0] pins on both DIMM0 and DIMM1. Terminate to DDR_TERM through a $56\ \Omega \pm 5\%$ resistor.	Refer to <a href="#">Section 6.6.5</a> .
SECC_A[7:0]	Connect to SECC[7:0] pins on both DIMM0 and DIMM1. Terminate to DDR_TERM through a $56\ \Omega \pm 5\%$ resistor.	Refer to <a href="#">Section 6.6.5</a> .
SCKE_A[3:0]	Connect to SCKE_A[1:0] to CKE[1:0] on DIMM0 and SCKE_A[3:2] to CKE[1:0] on DIMM1. Terminate to DDR_TERM through a $47\ \Omega \pm 5\%$ resistor.	Refer to <a href="#">Section 6.6.3</a> .
SCS_A[3:0]#	Connect to SCS_A[1:0]# to CS[1:0]# on DIMM0 and SCS_A[3:2]# to CS[1:0]# on DIMM1. Terminate to DDR_TERM through a $47\ \Omega \pm 5\%$ resistor.	Refer to <a href="#">Section 6.6.3</a> .
SMVREF_A	Terminate to ground through a $2.2\ \mu\text{F} \pm 20\%$ capacitor and $0.1\ \mu\text{F} \pm 20\%$ capacitor.	Refer to <a href="#">Section 6.8.2</a> .
SMXRCOMP	$42.2\ \Omega \pm 1\%$ pulled to VDD (2.6 V), place resistors within 1.0 inch of the MCH and pull to GND through a $42.2 \pm 1\%$ resistor. Decouple 2.6 V with a $2.2\ \mu\text{F}$ capacitor locally if power is drawn from the flood.	Refer to <a href="#">Section 6.9</a> .
SMXRCOMP VOH and VOL	Connect to a resistor divider consisting of a $31.1\ \text{k}\Omega \pm 1\%$ resistor and a $10\ \text{k}\Omega \pm 1\%$ resistor. Decouple 2.6 V with a $2.2\ \mu\text{F}$ capacitor locally if power is drawn from the flood. Decouple resistor divider with a $1\ \mu\text{F}$ capacitor if more than 1" from the MCH. Place a $0.01\ \mu\text{F}$ capacitor at the MCH.	Refer to <a href="#">Section 6.9</a> .

## 16.3.4 MCH / DDR-B Items

Table 109. MCH / DDR-B Items (Sheet 1 of 2)

Checklist Items	Connections/Recommendations	Reason/Impact
SCMDCLK_B0	Connect to CK0P in DIMM0.	Refer to <a href="#">Section 6.6.2</a> .
SCMDCLK_B0#	Connect to CK0N in DIMM0.	Refer to <a href="#">Section 6.6.2</a> .
SCMDCLK_B1	Connect to CK1 in DIMM0.	Refer to <a href="#">Section 6.6.2</a> .
SCMDCLK_B1#	Connect to CK1# in DIMM0.	Refer to <a href="#">Section 6.6.2</a> .
SCMDCLK_B2	Connect to CK2 in DIMM0.	Refer to <a href="#">Section 6.6.2</a> .
SCMDCLK_B2#	Connect to CK2# in DIMM0.	Refer to <a href="#">Section 6.6.2</a> .
SCMDCLK_B3	Connect to CK0P in DIMM1.	Refer to <a href="#">Section 6.6.2</a> .
SCMDCLK_B3#	Connect to CK0N in DIMM1.	Refer to <a href="#">Section 6.6.2</a> .
SCMDCLK_B4	Connect to CK1 in DIMM1.	Refer to <a href="#">Section 6.6.2</a> .
SCMDCLK_B4#	Connect to CK1# in DIMM1.	Refer to <a href="#">Section 6.6.2</a> .
SCMDCLK_B5	Connect to CK2 in DIMM1.	Refer to <a href="#">Section 6.6.2</a> .
SCMDCLK_B5#	Connect to CK2# in DIMM1.	Refer to <a href="#">Section 6.6.2</a> .
SMA_B[12:0]	Connect to A[12:0] on both DIMM0 and DIMM1. Terminate to DDR_TERM through a $47\ \Omega \pm 5\%$ resistor.	Refer to <a href="#">Section 6.6.4</a> .
SBA_B[1:0]	Connect to BA[1:0] pin on both DIMM0 and DIMM1. Terminate to DDR_TERM through a $47\ \Omega \pm 5\%$ resistor.	Refer to <a href="#">Section 6.6.4</a> .
SRAS_B#	Connect to RAS# pin on both DIMM0 and DIMM1. Terminate to DDR_TERM through a $47\ \Omega \pm 5\%$ resistor.	Refer to <a href="#">Section 6.6.4</a> .
SCAS_B#	Connect to CAS# pin on both DIMM0 and DIMM1. Terminate to DDR_TERM through a $47\ \Omega \pm 5\%$ resistor.	Refer to <a href="#">Section 6.6.4</a> .
SWE_B#	Connect to WE# pin on each DIMM0 and DIMM1. Terminate to DDR_TERM through a $47\ \Omega \pm 5\%$ resistor.	Refer to <a href="#">Section 6.6.4</a> .
SDQ_B[63:0]	Connect to SDQ[63:0] on both DIMM0 and DIMM1. Terminate to DDR_TERM through a $56\ \Omega \pm 5\%$ resistor.	Refer to <a href="#">Section 6.6.5</a> .
SDQS_B[8:0]	Connect to SDQS[8:0] pins on both DIMM0 and DIMM1. Terminate to DDR_TERM through a $56\ \Omega \pm 5\%$ resistor.	Refer to <a href="#">Section 6.6.5</a> .
SECC_B[7:0]	Connect to SECC[7:0] pins on both DIMM0 and DIMM1. Terminate to DDR_TERM through a $56\ \Omega \pm 5\%$ resistor.	Refer to <a href="#">Section 6.6.5</a> .
SCKE_B[3:0]	Connect to SCKE_B[1:0] to CKE[1:0] on DIMM0 and SCKE_B[3:2] to CKE[1:0] on DIMM1. Terminate to DDR_TERM through a $47\ \Omega \pm 5\%$ resistor.	Refer to <a href="#">Section 6.6.3</a> .
SCS_B[3:0]#	Connect to SCS_B[1:0]# to CS[1:0]# on DIMM0 and SCS_B[3:2]# to CS[1:0]# on DIMM1. Terminate to DDR_TERM through a $47\ \Omega \pm 5\%$ resistor.	Refer to <a href="#">Section 6.6.3</a> .

**Table 109. MCH / DDR-B Items (Sheet 2 of 2)**

Checklist Items	Connections/Recommendations	Reason/Impact
SMVREF_B	Connect to a resistor divider of $150\ \Omega \pm 1\%$ to both VDD (2.6 V) and ground. Terminate to ground through a $2.2\ \mu\text{F} \pm 20\%$ capacitor and a $0.1\ \mu\text{F} \pm 20\%$ capacitor. Also terminate VDD (2.6 V) to ground through a $2.2\ \mu\text{F}$ capacitor.	Refer to <a href="#">Section 6.8.2</a> .
SMYRCOMP	$42.2\ \Omega \pm 1\%$ pulled to VDD (2.6 V), place resistors within 1.0 inch of the MCH and pull to GND through a $42.2 \pm 1\%$ resistor. Decouple 2.6 V with a $2.2\ \mu\text{F}$ capacitor locally if power is drawn from the flood.	Refer to <a href="#">Section 6.9</a> .
SMYRCOMP VOH and VOL	Connect to a resistor divider consisting of a $30.1\ \text{k}\Omega \pm 1\%$ resistor and a $10\ \text{k}\Omega \pm 1\%$ resistor. Decouple 2.6 V with a $2.2\ \mu\text{F}$ capacitor locally if power is drawn from the flood. Decouple resistor divider with a $1\ \mu\text{F}$ capacitor if more than 1" from the MCH. Place a $0.01\ \mu\text{F}$ capacitor at the MCH.	Refer to <a href="#">Section 6.9</a> .

### 16.3.5 MCH / AGP Items (Intel® 875P MCH Only)

Checklist Items	Connections/Recommendations	Reason/Impact
GADSTBF[1:0]	Connect to GAD_STB[1:0] in AGP.	Refer to <a href="#">Section 7.2.2</a> .
GADSTBS[1:0]	Connect to GAD_STB[1:0]# in AGP.	
GAD[31:0]	Connect to GAD[31:0] in AGP.	
GCBE[3:0]	Connect to GC_BE[3:0]# in AGP.	
GDEVSEL	Connect to GDEVSEL# in AGP.	
GFRAME	Connect to GFRAME# in AGP.	
GGNT	Connect to GGNT# in AGP.	
GIRDY	Connect to GIRDY# in AGP.	
GPARG/ADD_DETECT	Connect to GPARG in AGP.	
DBI_HI	Connect to DBI_HI/PIPE# in AGP.	
DBI_LO	Connect to DBI_LO in AGP.	
GREQ	Connect to GREQ# in AGP.	
GSTOP	Connect to GSTOP# in AGP.	
GTRDY	Connect to GTRDY# in AGP.	
GRBF	Connect to RBF# in AGP.	
GSBA[7:0]#	Connect to SBA[7:0] in AGP.	
GSBSTBF	Connect to SB_STB in AGP.	
GSBSTBS	Connect to SB_STB# in AGP.	
GST[2:0]	Connect to ST[2:0] in AGP.	
GWBF	Connect to WBF# in AGP.	

### 16.3.6 MCH / AGP Only Items (Intel® 875P MCH Only)

Checklist Items	Connections/Recommendations	Reason/Impact
GRCOMP	Pulled up to 1.5 V core through a $43.2 \Omega \pm 1\%$ resistor on chipset decoupling.	
GSWING	Connects from the 875P MCH to a resistor divider network of the AGP SWING/VREF reference circuit.	Refer to <a href="#">Section 7.2.4.5</a> and <a href="#">Figure 68</a> for more detailed information.
GVREF	Connect to the AGP Ref pin of the AGP connector and to a resistor divider network of the AGP SWING/VREF Reference Circuit.	<a href="#">Section 7.2.4.4</a> and <a href="#">Figure 68</a> for more detailed information. NOTE: This signal must be connected for the E7210 MCH.
GCLKIN	Connect to 3V662/pin#26 on CK409 through a $33 \Omega \pm 5\%$ series resistor.	

### 16.3.7 MCH / HUB Items

Checklist Items	Connections/Recommendations	Reason/Impact
HI[10:0]	Connect to HI[10:0] in 6300ESB ICH.	Refer to <a href="#">Section 9.4</a> .
HISTRS	Connect to HI_STBS in 6300ESB ICH.	Refer to <a href="#">Section 9.4</a> .
HISTRF	Connect to HI_STBF in 6300ESB ICH.	Refer to <a href="#">Section 9.4</a> .
HI_VREF	Connect to MCH REF of HUB connector voltage divider circuit on chipset decoupling.	Refer to <a href="#">Section 9.4</a> .
HI_SWING	Connect to voltage divider circuit on chipset decoupling.	Refer to <a href="#">Section 9.4</a> .
HI_RCOMP	Pull up to 1.5 V core through $52.3 \Omega \pm 1\%$ resistor on decoupling.	Refer to <a href="#">Section 9.4</a> .

### 16.3.8 MCH / CSA Items

Checklist Items	Connections/Recommendations	Reason/Impact
CI[10:0]	CI[10:0] connect to CI[0:10] on 82547GI GbE LAN controller.	
CISTRF	Connect to CI_STBF on the 82547GI GbE LAN controller.	
CISTRS	Connect to CI_STBS on the 82547GI GbE LAN controller.	
CI_RCOMP	Pull up to 1.5 V core through a $52.3 \Omega \pm 1\%$ resistor.	
CI_SWING	Connect to SWING generation circuit with a $0.1 \mu\text{F}$ decoupling capacitor at MCH pin.	
CI_VREF	Connect to VREF generation circuit with a $0.1 \mu\text{F}$ decoupling capacitor at the MCH pin.	

## 16.3.9 MCH / Power Items

Checklist Items	Connections/Recommendations	Reason/Impact
VTT	Connect to output of MCH_VTT regulator.	
VCC_DDR	Connect to output of 2.6 V VREG.	
VCCA_AGP	Connect to output of VCCA_AGP filter.	
VCCA_FSB	Connect to output of VCCA_FSB filter.	Refer to <a href="#">Section 13.3.3.2</a> .
VCCA_SM	Connect to output of VCCA_SM filter.	Refer to <a href="#">Section 13.3.3.2</a> .
VCC	Connect to 1.5 V core through plane filter.	Refer to <a href="#">Section 13.3.3.1</a> .
VCC_AGP	Connect to 1.5 V core.	

## 16.3.10 MCH / Miscellaneous Items

Checklist Items	Connections/Recommendations	Reason/Impact
RSTIN#	Connect to PXPCIRST# on the 6300ESB ICH through a 0 $\Omega$ resistor and tie to GND through a 10 pF $\pm$ 5% capacitor.	
RESERVED	No Connect	

## 16.4 Clock CK409 Interface

Table 110. Clock CK409 Interface (Sheet 1 of 4)

Checklist Items	Connections/Recommendations	Reason/Impact
3V66_0	Connect to the 66 MHz in of CSA device, MCH, 6300ESB ICH, or AGP. Connect to a series 33 $\Omega$ $\pm$ 5% resistor and terminate to GND through a 10 pF $\pm$ 5% capacitor.	CLK66 Clock Group
3V66_1	Connect to the 66 MHz in of CSA device, MCH, 6300ESB ICH, or AGP. Connect to a series 33 $\Omega$ $\pm$ 5% resistor and terminate to GND through a 10 pF $\pm$ 5% capacitor.	CLK66 Clock Group
3V66_2	Connect to the 66 MHz in of CSA device, MCH, 6300ESB ICH, or AGP. Connect to a series 33 $\Omega$ $\pm$ 5% resistor and terminate to GND through a 10 pF $\pm$ 5% capacitor.	CLK66 Clock Group
3V66_3	Connect to the 66 MHz in of CSA device, MCH, 6300ESB ICH, or AGP. Connect to a series 33 $\Omega$ $\pm$ 5% resistor and terminate to GND through a 10 pF $\pm$ 5% capacitor.	CLK66 Clock Group

Table 110. Clock CK409 Interface (Sheet 2 of 4)

Checklist Items	Connections/Recommendations	Reason/Impact
3V66_4 / VCH	Connect to the 66 MHz in of CSA device, MCH, 6300ESB ICH, or AGP. Connect to a series $33\ \Omega \pm 5\%$ resistor and terminate to GND through a $10\ \text{pF} \pm 5\%$ capacitor.	CLK66 Clock Group
CPU0	Connect to CPU, MCH, or ITP. Connect to a series $33\ \Omega \pm 5\%$ resistor and terminate to GND through a $49.9\ \Omega \pm 1\%$ resistor.	Host Clock Group
CPU0#	Connect to CPU, MCH, or ITP. Connect to a series $33\ \Omega \pm 5\%$ resistor and terminate to GND through a $49.9\ \Omega \pm 1\%$ resistor.	Host Clock Group
CPU1	Connect to CPU, MCH, or ITP. Connect to a series $33\ \Omega \pm 5\%$ resistor and terminate to GND through a $49.9\ \Omega \pm 1\%$ resistor.	Host Clock Group
CPU1#	Connect to CPU, MCH, or ITP. Connect to a series $33\ \Omega \pm 5\%$ resistor and terminate to GND through a $49.9\ \Omega \pm 1\%$ resistor.	Host Clock Group
CPU2	Connect to CPU, MCH, or ITP. connect to a series $33\ \Omega \pm 5\%$ resistor and terminate to GND through a $49.9\ \Omega \pm 1\%$ resistor.	Host Clock Group
CPU2#	Connect to CPU, MCH, or ITP. Connect to a series $33\ \Omega \pm 5\%$ resistor and terminate to GND through a $49.9\ \Omega \pm 1\%$ resistor.	Host Clock Group
CPU_STOP#	Pull-up to VCC3_CLK through a $1\ \text{k}\Omega \pm 5\%$ resistor.	Host Clock Group
DOT_48MHz	Connect to ICH. Connect to a series $33\ \Omega \pm 5\%$ resistor and terminate to GND through a $10\ \text{pF} \pm 5\%$ capacitor.	
FSB / FSA	Connect to Host clock frequency select circuit. See the <i>CK409 Clock Synthesizer/Driver Specification</i> for more details.	
REF0	Connect to 14 MHz input buffer of ICH or audio device. Connect through a series $33\ \Omega \pm 5\%$ resistor and terminate to GND through a $10\ \text{pF} \pm 5\%$ capacitor.	
REF1	Connect to 14 MHz input buffer of ICH or audio device. Connect through a series $33\ \Omega \pm 5\%$ resistor and terminate to GND through a $10\ \text{pF} \pm 5\%$ capacitor.	
IREF	Terminate to GND through a $475\ \Omega \pm 1\%$ resistor.	
VSS_IREF	Terminate to GND of IREF resistor.	
PCI0	Connect to 33 MHz input buffer of PCI devices, PCI connector, BIOS chip, or 6300ESB ICH through a series $33\ \Omega \pm 5\%$ resistor and terminate to GND through a $10\ \text{pF} \pm 5\%$ capacitor.	
PCI1	Connect to 33 MHz input buffer of PCI devices, PCI connector, BIOS chip, or 6300ESB ICH through a series $33\ \Omega \pm 5\%$ resistor and terminate to GND through a $10\ \text{pF} \pm 5\%$ capacitor.	



**Table 110. Clock CK409 Interface (Sheet 3 of 4)**

Checklist Items	Connections/Recommendations	Reason/Impact
PCI2	Connect to 33 MHz input buffer of PCI devices, PCI connector, BIOS chip, or 6300ESB ICH through a series $33\ \Omega \pm 5\%$ resistor and terminate to GND through a $10\ \text{pF} \pm 5\%$ capacitor.	
PCI3	Connect to 33 MHz input buffer of PCI devices, PCI connector, BIOS chip, or 6300ESB ICH through a series $33\ \Omega \pm 5\%$ resistor and terminate to GND through a $10\ \text{pF} \pm 5\%$ capacitor.	
PCI4	Connect to 33 MHz input buffer of PCI devices, PCI connector, BIOS chip, or 6300ESB ICH through a series $33\ \Omega \pm 5\%$ resistor and terminate to GND through a $10\ \text{pF} \pm 5\%$ capacitor.	
PCI5	Connect to 33 MHz input buffer of PCI devices, PCI connector, BIOS chip, or 6300ESB ICH through a series $33\ \Omega \pm 5\%$ resistor and terminate to GND through a $10\ \text{pF} \pm 5\%$ capacitor.	
PCI6	Connect to 33 MHz input buffer of PCI devices, PCI connector, BIOS chip, or 6300ESB ICH through a series $33\ \Omega \pm 5\%$ resistor and terminate to GND through a $10\ \text{pF} \pm 5\%$ capacitor.	
PCIF0	Connect to 33 MHz input buffer of PCI devices, PCI connector, BIOS chip, or 6300ESB ICH through a series $33\ \Omega \pm 5\%$ resistor and terminate to GND through a $10\ \text{pF} \pm 5\%$ capacitor.	
PCIF1	Connect to 33 MHz input buffer of PCI devices, PCI connector, BIOS chip, or 6300ESB ICH through a series $33\ \Omega \pm 5\%$ resistor and terminate to GND through a $10\ \text{pF} \pm 5\%$ capacitor.	
PCIF2	Connect to 33 MHz input buffer of PCI devices, PCI connector, BIOS chip, or 6300ESB ICH through a series $33\ \Omega \pm 5\%$ resistor and terminate to GND through a $10\ \text{pF} \pm 5\%$ capacitor.	
PCI_STOP#	If not used pull up to VCC3 through $1\ \text{k}\Omega$ . Otherwise, see the <i>CK409 Clock Synthesizer/Driver Specification</i> for more details.	PCICLK Group
PWRDWN#	Pull-up to VCC3 through a $1\ \text{k}\Omega$ resistor.	
SCLK	Connect to SMBus CLK.	
SDATA	Connect to SMBus Data.	
SRC	Connect to Serial ATA clock input to 6300ESB ICH through a series $33.2\ \Omega \pm 5\%$ resistor and terminate to GND through a $49.9\ \Omega \pm 1\%$ resistor.	
SRC#	Connect to Serial ATA clock input to 6300ESB ICH through to a series $33.2\ \Omega \pm 5\%$ resistor and terminate to GND through a $49.9\ \Omega \pm 1\%$ resistor.	
USB_48Mhz	Connect to ICH_USB clock input through a series $33\ \Omega \pm 5\%$ resistor and terminate to GND through a $10\ \text{pF} \pm 5\%$ capacitor.	
VDD	Connect through a $300\ \Omega$ ( $100\ \text{MHz}$ ) FB to VCC3 with one $10\ \mu\text{F}$ bulk decoupling capacitor and one $0.1\ \mu\text{F}$ capacitor for each VDD pin.	

Table 110. Clock CK409 Interface (Sheet 4 of 4)

Checklist Items	Connections/Recommendations	Reason/Impact
VDD48	Terminate to VCC3_CLK through a $10\ \Omega \pm 5\%$ resistor and terminate to GND through one $4.7\ \mu\text{F}$ capacitor and one $0.1\ \mu\text{F}$ capacitor	
VDDA	Connect through a $300\ \Omega$ (100 MHz) FB to VCC3 with one $10\ \mu\text{F}$ bulk decoupling capacitor and one $0.1\ \mu\text{F}$ capacitor for each VDD pin.	
VSS	Terminate to GND.	
VTT_PWRGD#	Connect to PWRGD circuitry. See the <i>CK409 Clock Synthesizer/Driver Specification</i> for more details. Connect to VCC3_CLK through a $10\ \text{K}\Omega \pm 5\%$ resistor.	
XTAL_IN	Connect to 14.318 MHz Crystal. See the <i>CK409 Clock Synthesizer/Driver Specification</i> for decoupling capacitor calculation.	Capacitor values may vary slightly from manufacturer to manufacturer.
XTAL_OUT	Connect to 14.318 MHz Crystal. See the <i>CK409 Clock Synthesizer/Driver Specification</i> for decoupling capacitor calculation.	Capacitor values may vary slightly from manufacturer to manufacturer.

## 16.5 AGP 4X/8X Interface (Intel® 875P MCH only)

### 16.5.1 AGP Connector / MCH Items

Checklist Items	Connections/Recommendations	Reason/Impact
GAD_STB[1:0]	Connect to GADSTBF[1:0] in MCH.	Refer to <a href="#">Section 7.2.2</a> .
GAD_STB[1:0]#	Connect to GADSTBS[1:0] in MCH.	
GAD[31:0]	Connect to GAD[31:0] in MCH.	
GC_BE[3:0]#	Connect to GCBE[3:0] in MCH.	
GDEVSEL#	Connect to GDEVSEL in MCH.	
GFRAME#	Connect to GFRAME in MCH.	
GGNT#	Connect to GGNT in MCH.	
GIRDY#	Connect to GIRDY in MCH.	
GPAR	Connect to GPAR/ADD_DETECT in MCH.	
PIPE# / DBI_HI	Connect to DBI_HI in MCH.	
GREQ#	Connect to GREQ in MCH.	
GSTOP#	Connect to GSTOP in MCH.	
GTRDY#	Connect to GTRDY in MCH.	
RBF#	Connect in GRBF in MCH.	
SBA[7:0]	Connect to GSBA[7:0]# in MCH.	
SB_STB	Connect to GSBSTBF in MCH.	
SB_STB#	Connect to GSBSTBS MCH.	
ST[2:0]	Connect to GST[2:0] in MCH.	
WBF#	Connect GWBF in MCH.	
VREFCG	Connect to AGPREF_MCH of the AGP SWING/VREF and the resistor divider of the GC_DET# Reference Circuit.	Refer to <a href="#">Section 7.2.4.4</a> .
GC_DET	Connect to the input of the GC_DET# on AGP SWING/VREF reference schematics.	Pulled low by an AGP 3.0 graphics card, and left floating by an AGP 2.0 graphics card. Refer to <a href="#">Section 7.2.4.2</a> and <a href="#">Figure 67</a> for more detailed information.
MB_DET	Connect to GND.	

## 16.5.2 AGP Connector Only Items

Checklist Items	Connections/Recommendations	Reason/Impact
INTA#	Connect P_INTA# in PCI.	
INTB#	Connect P_INTB# in PCI.	
3.3VAUX	Connect to V_3P3_PCI in PCI VAUX.	
VCC3	Connect to VCC3.	
12V	Connect to +12 V.	
VCC	Connect to VCC.	
VDDQ	Connect to V_1P5_CORE in 1.5 V core.	
AGPCLK	Connect to a 66 MHz clock of the CK409.	
GPERR#	Connect to the input of the G_PERR_PU# on AGP SWING/VREF Reference Circuit.	Refer to <a href="#">Section 7.2.4.1</a> and <a href="#">Figure 67</a> for more detailed information.
GSERR#	Pull up to 1.5 V core through a 6.8 k $\Omega$ $\pm$ 5%.	
OVRCNT	No Connect	
PCIRST	Connect to the system PCIRST logic	
PME#	Connect to P_PME# on PCI.	
TYPEDET#	No Connect	Signal not required due to the use of 1.5 V connector.
USB+	No Connect	5 V tolerant
USB-	No Connect	5 V tolerant
RSVD	No Connect	
VREFGC	No Connect	

## 16.6 DDR Dual-Channel Interface

### 16.6.1 DDR Channel A DIMM0 and DIMM1 / MCH Items

Table 111. DDR Channel A DIMM0 and DIMM1 / MCH Items (Sheet 1 of 2)

Checklist Items	Connections/Recommendations	Reason/Impact
CK0P	DIMM0: Connect to SCMDCLK_A0. DIMM1: Connect to SCMDCLK_A3.	Refer to <a href="#">Section 6.6.2</a> .
CK0N	DIMM0: Connect to SCMDCLK_A0#. DIMM1: Connect to SCMDCLK_A3#.	Refer to <a href="#">Section 6.6.2</a> .
CK1	DIMM0: Connect to SCMDCLK_A1. DIMM1: Connect to SCMDCLK_A4.	Refer to <a href="#">Section 6.6.2</a> .
CK1#	DIMM0: Connect to SCMDCLK_A1#. DIMM1: Connect to SCMDCLK_A4#.	Refer to <a href="#">Section 6.6.2</a> .
CK2	DIMM0: Connect to SCMDCLK_A2. DIMM1: Connect to SCMDCLK_A5.	Refer to <a href="#">Section 6.6.2</a> .
CK2#	DIMM0: Connect to SCMDCLK_A2#. DIMM1: Connect to SCMDCLK_A5#.	Refer to <a href="#">Section 6.6.2</a> .
A[12:0]	DIMM0: Connect to SMA_A[12:0]. Terminate to DDR_TERM through a parallel of $47\ \Omega \pm 5\%$ resistor.	Refer to <a href="#">Section 6.6.4</a> .
BA[1:0]	DIMM0 and DIMM1: Connect to SBA_A[1:0]. Terminate to DDR_TERM through a $47\ \Omega \pm 5\%$ resistor.	Follow DDR address/command signal routing topology guidelines. Refer to <a href="#">Section 6.6.4</a> .
RAS#	DIMM0 and DIMM1: Connect to SRAS_A#. Terminate to DDR_TERM through a $47\ \Omega \pm 5\%$ resistor.	Follow DDR address/command signal routing topology guidelines. Refer to <a href="#">Section 6.6.4</a> .
CAS#	DIMM0 and DIMM1: Connect to SCAS_A#. Terminate to DDR_TERM through a $47\ \Omega \pm 5\%$ resistor.	Follow DDR address/command signal routing topology guidelines. refer to <a href="#">Section 6.6.4</a> .
WE#	DIMM0 and DIMM1: Connect to SWE_A#. Terminate to DDR_TERM through a $47\ \Omega \pm 5\%$ resistor.	Follow DDR address/command signal routing topology guidelines. Refer to <a href="#">Section 6.6.4</a> .
DQ[63:0]	DIMM0 and DIMM1: Connect to SDQ_A[63:0]. Terminate to DDR_TERM through a $56\ \Omega \pm 5\%$ resistor.	Follow DDR data signal routing topology guidelines. Refer to <a href="#">Section 6.6.5</a> .
DQS[8:0]	DIMM0 and DIMM1: Connect to SDQS_A[8:0]. Terminate to DDR_TERM through a $56\ \Omega \pm 5\%$ resistor.	Follow DDR data signal routing topology guidelines. Refer to <a href="#">Section 6.6.5</a> .
SECC[7:0]	Connect to SECC_A[7:0] for both DIMM1 and DIMM0.	Follow DDR data signal routing topology guidelines. Refer to <a href="#">Section 6.6.5</a> .

Table 111. DDR Channel A DIMM0 and DIMM1 / MCH Items (Sheet 2 of 2)

Checklist Items	Connections/Recommendations	Reason/Impact
CKE[1:0]	Connect SCKE_A[1:0] to CKE[1:0] on DIMM0. Connect SCKE_A[3:2] to CKE[1:0] on DIMM1. Terminate to DDR_TERM through a $47\ \Omega \pm 5\%$ resistor.	Refer to <a href="#">Section 6.6.3</a> .
CS[1:0]#	<ul style="list-style-type: none"> <li>Connect SCS_A[1:0]# to CS[1:0]# on DIMM0.</li> <li>Connect SCS_A[3:2]# to CS[1:0]# on DIMM1.</li> <li>Terminate to DDR_TERM through a <math>47\ \Omega \pm 5\%</math> resistor.</li> </ul>	Refer to <a href="#">Section 6.6.3</a> .
DIMM VREF		Refer to <a href="#">Section 6.8.3</a> .

## 16.6.2 DDR Channel-A DIMM0 and DIMM1 Only Items

Checklist Items	Connections/Recommendations	Reason/Impact
A13 / NC	No Connect for both DIMM0 and DIMM1.	
DM[8:0] / SDQS[17]	Connect to GND for both DIMM0 and DIMM1.	
BA2	No Connect for both DIMM0 and DIMM1.	
SA[2:0]	DIMM0: Connect to GND. DIMM1: Connect SA[2:1] to GND, and Connect SA0 to 2.6 V.	
WP / NC	No Connect for both DIMM0 and DIMM1.	
RESET#	No Connect for both DIMM0 and DIMM1.	
FETEN / NC	No Connect for both DIMM0 and DIMM1.	
SDA	Connect to Gluechip* 4, CNR60, and CK409.	
SCL	Connect to SMB_CLK_MAIN.	
VDDSPD	Connect to power (from a minimum of 2.3 V to a maximum of 3.6 V). Strongly recommend connecting to 2.6 V core.	
VDDID	No Connect for both DIMM0 and DIMM1.	
VDD	Connect to 2.6 V on both DIMM0 and DIMM1.	
VDDQ	Connect to 2.6 V on both DIMM0 and DIMM1.	
VSS	Connect to GND on both DIMM0 and DIMM1.	
NC	No Connect for both DIMM0 and DIMM1.	
CS3#	No Connect for both DIMM0 and DIMM1.	
CS2#	No Connect for both DIMM0 and DIMM1.	

### 16.6.3 DDR Channel-B DIMM0 and DIMM1 / MCH Items

**Table 112. DDR Channel-B DIMM0 and DIMM1 / MCH Items (Sheet 1 of 2)**

Checklist Items	Connections/Recommendations	Reason/Impact
CK0P	DIMM0: Connect to SCMDCLK_B0. DIMM1: Connect to SCMDCLK_B3.	Refer to <a href="#">Section 6.6.2</a> .
CK0N	DIMM0: Connect to SCMDCLK_B0#. DIMM1: Connect to SCMDCLK_B3#.	Refer to <a href="#">Section 6.6.2</a> .
CK1	DIMM0: Connect to SCMDCLK_B1. DIMM1: Connect to SCMDCLK_B4.	Refer to <a href="#">Section 6.6.2</a> .
CK1#	DIMM0: Connect to SCMDCLK_B1#. DIMM1: Connect to SCMDCLK_B4#.	Refer to <a href="#">Section 6.6.2</a> .
CK2	DIMM0: Connect to SCMDCLK_B2. DIMM1: Connect to SCMDCLK_B5.	Refer to <a href="#">Section 6.6.2</a> .
CK2#	DIMM0: Connect to SCMDCLK_B2#. DIMM1: Connect to SCMDCLK_B5#.	Refer to <a href="#">Section 6.6.2</a> .
CS[1:0]#	Connect SCS_B[1:0]# to CS[1:0]# on DIMM0 Connect SCS_B[3:2]# to CS[1:0]# on DIMM1 Terminate to DDR_TERM through a $47\ \Omega \pm 5\%$ resistor.	Refer to <a href="#">Section 6.6.4</a> .
A[12:0]	DIMM0: Connect to SMA_B[12:0]. Terminate to DDR_TERM through a parallel of $47\ \Omega \pm 5\%$ resistor.	Follow DDR address/command signal routing topology guidelines. Refer to <a href="#">Section 6.6.4</a> .
BA[1:0]	DIMM0 and DIMM1: Connect to SBA_B[1:0]. Terminate to DDR_TERM through a $47\ \Omega \pm 5\%$ resistor.	Follow DDR address/command signal routing topology guidelines. Refer to <a href="#">Section 6.6.4</a> .
RAS#	DIMM0 and DIMM1: Connect to SRAS_B#. Terminate to DDR_TERM through a $47\ \Omega \pm 5\%$ resistor.	Follow DDR address/command signal routing topology guidelines. refer to <a href="#">Section 6.6.4</a> .
CAS#	DIMM0 and DIMM1: Connect to SCAS_B#. Terminate to DDR_TERM through a $47\ \Omega \pm 5\%$ resistor.	Follow DDR address/command signal routing topology guidelines. Refer to <a href="#">Section 6.6.4</a> .
WE#	DIMM0 and DIMM1: Connect to SWE_B#. Terminate to DDR_TERM through a $47\ \Omega \pm 5\%$ resistor.	Follow DDR data signal routing topology guidelines. Refer to <a href="#">Section 6.6.4</a> .
DQ[63:0]	DIMM0 and DIMM1: Connect to SDQ_B[63:0] Terminate to DDR_TERM through a $56\ \Omega \pm 5\%$ resistor.	Follow DDR data signal routing topology guidelines. Refer to <a href="#">Section 6.6.5</a> .
DQS[8:0]	DIMM0 and DIMM1: Connect to SDQS_B[8:0] Terminate to DDR_TERM through a $56\ \Omega \pm 5\%$ resistor.	Refer to <a href="#">Section 6.6.5</a> .

Table 112. DDR Channel-B DIMM0 and DIMM1 / MCH Items (Sheet 2 of 2)

Checklist Items	Connections/Recommendations	Reason/Impact
SECC[7:0]	Connect to SECC_B[7:0] for both DIMM1 and DIMM0.	Refer to <a href="#">Section 6.6.5</a> .
CKE[1:0]	Connect SCKE_B[1:0] to CKE[1:0] on DIMM0. Connect SCKE_B[3:2] to CKE[1:0] on DIMM1. Terminate to DDR_TERM through a $47\ \Omega \pm 5\%$ resistor.	Refer to <a href="#">Section 6.6.3</a> .
DIMM VREF	DIMM0 and DIMM1: Connect to a resistor divider of $75\ \Omega \pm 1\%$ to both VDD (2.6 V) and ground. Decouple each DIMM with a 0.1 $\mu$ F capacitor.	Refer to <a href="#">Section 6.8.3</a> .

## 16.6.4 DDR Channel-B DIMM0 and DIMM1 Only Items

Checklist Items	Connections/Recommendations	Reason/Impact
A13 / NC	No Connect for both DIMM0 and DIMM1.	
DM[8:0] / SDQS[17]	Connect to GND for both DIMM0 and DIMM1.	
BA2	No Connect for both DIMM0 and DIMM1.	
SA[2:0]	DIMM0: Connect SA[2,0] to GND, and Connect SA1 to 2.6 V. DIMM1: Connect SA2 to GND, and Connect SA[1:0] to 2.6 V.	
WP / NC	No Connect for both DIMM0 and DIMM1.	
RESET#	No Connect for both DIMM0 and DIMM1.	
FETEN / NC	No Connect for both DIMM0 and DIMM1.	
SDA	Connect to Gluechip 4, CNR60, and CK409.	
SCL	Connect to SMB_CLK_MAIN.	
VDDSPD	Connect to power (from a minimum of 2.3 V to a maximum of 3.6 V). Strongly recommend connecting to 3.3 V core.	
VDDID	No Connect for both DIMM0 and DIMM1.	
VDD	Connect to 2.6 V on both DIMM0 and DIMM1.	
VDDQ	Connect to 2.6 V on both DIMM0 and DIMM1.	
VSS	Connect to GND on both DIMM0 and DIMM1.	
NC	No Connect for both DIMM0 and DIMM1.	
CS3#	No Connect for both DIMM0 and DIMM1.	
CS2#	No Connect for both DIMM0 and DIMM1.	



## 16.7 ICH Interface

This checklist highlights design considerations that should be reviewed prior to manufacturing a motherboard that implements an 6300ESB ICH. The items contained within this checklist attempt to address important connections to these devices and any critical supporting circuitry.

**Note:** This is not a complete list and does not ensure that a design will function properly.

**Note:** Platforms were validated with all interfaces in use.

**Caution:** Inputs to the 6300ESB ICH must not be left floating unless otherwise noted.

### 16.7.1 PCI-X Interface Checklist

**Table 113. PCI-X Interface Checklist (Sheet 1 of 3)**

Checklist Items	Recommendations	Interface Not Used	Reason/Impact
PXAD[32:63]	8.2 K $\Omega$ pull-up resistors to VCC3.3	May leave as no connect	
PXAD[0:31]	No extra pull-ups needed.	May leave as no connect	
PXPCICLK	Ensure this pin is connected to a 66MHz clock output of the clock generator (CK409) through a 33 $\Omega$ resistor.	Ensure this pin is connected to a 66MHz clock output of the clock generator (CK409) through a 33 $\Omega$ resistor	
PXRCOMP	30 $\Omega$ $\pm$ 1% pull-down resistor to Vss	30 $\Omega$ $\pm$ 1% pull-down resistor to Vss	Place close to the 6300ESB ICH.
PXACK64#	8.2 K $\Omega$ pull-up resistor to VCC3.3	8.2 K $\Omega$ pull-up resistor to VCC3.3	
PXM66EN	10 K $\Omega$ pull-up resistor to VCC3.3	10 K $\Omega$ pull-up resistor to VCC3.3	See <i>PCI-X Specification 1.0a</i> for more recommendations.
PXPCIXCAP	4.7 K $\Omega$ pull-up resistor to VCC3.3 for three slot configurations 8.2 K $\Omega$ pull-up resistor to VCC3.3 for all other configurations	May leave as no connect	When the signal is read as a logic high there is no effect. (Does not support PCI-X 133 MHz). See <i>PCI-X Specification 1.0a</i> for more recommendations on PXPCIXCAP connections.
PXREQ64#	8.2 K $\Omega$ pull-up resistor to VCC3.3	8.2 K $\Omega$ pull-up resistor to VCC3.3	
PXREQ[0:1]# PXREQ[2]# / GPIO[0] PXREQ[3]# / GPIO[1]	8.2 K $\Omega$ pull-up resistors to VCC3.3	8.2 K $\Omega$ pull-up resistors to VCC3.3	

Table 113. PCI-X Interface Checklist (Sheet 2 of 3)

Checklist Items	Recommendations	Interface Not Used	Reason/Impact
PXGNT[0:1]# PXGNT[2]# / GPIO[16] PXGNT[3]# / GPIO[17]	No extra pull-ups needed.	May leave as no connect.	These signals are actively driven by the 6300ESB ICH
PXDEVSEL#	8.2 K $\Omega$ pull-up resistor to VCC3.3	8.2 K $\Omega$ pull-up resistor to VCC3.3	
PXFRAME#	8.2 K $\Omega$ pull-up resistor to VCC3.3	8.2 K $\Omega$ pull-up resistor to VCC3.3	
PXIRDY#	8.2 K $\Omega$ pull-up resistor to VCC3.3	8.2 K $\Omega$ pull-up resistor to VCC3.3	
PXPAR	No extra pull-ups needed	May leave as no connect	
PXPAR64	8.2 K $\Omega$ pull-up resistor to VCC3.3	May leave as no connect	
PXPERR#	8.2 K $\Omega$ pull-up resistor to VCC3.3	8.2 K $\Omega$ pull-up resistor to VCC3.3	
PXSERR#	8.2 K $\Omega$ pull-up resistor to VCC3.3	8.2 K $\Omega$ pull-up resistor to VCC3.3	See <i>PCI-X specification rev 1.0a</i> .
PXSTOP#	8.2 K $\Omega$ pull-up resistor to VCC3.3	8.2 K $\Omega$ pull-up resistor to VCC3.3	
PXTRDY#	8.2 K $\Omega$ pull-up resistor to VCC3.3	8.2 K $\Omega$ pull-up resistor to VCC3.3	
RASERR#	8.2 K $\Omega$ pull-up resistor to VCC3.3	May leave as no connect	
PXC/BE#[4:7]	8.2 K $\Omega$ pull-up resistors to VCC3.3	May leave as no connect	
PXC/BE#[0:3]	No extra pull-ups needed.	May leave as no connect	
PXPCLKI	No extra pull-ups needed. Ensure this is connected to PXPCLK04 through a 33 $\Omega$ resistor.	No extra pull-ups needed Ensure this is connected to PXPCLK04 through a 33 $\Omega$ resistor	Feedback clock
PXPCLKO4	No extra pull-ups needed. Ensure this is connected to PXPCLKI through a 33 $\Omega$ resistor.	No extra pull-ups needed. Ensure this is connected to PXPCLKI through a 33 $\Omega$ resistor.	This signal is actively driven by the 6300ESB ICH.
PXPCLKO[0:3]	No extra pull-ups needed. Ensure this is connected to the PCI-X/PCI Device through a 33 $\Omega$ resistor.	May leave as no connect.	These signals are actively driven by the 6300ESB ICH.
PXPCIRST#	No extra pull-up needed. Connected to the MCH, External Controllers (LAN etc.), FWH, SIO Controllers and Glue Chip respective reset signals.	No extra pull-up needed. Connected to the MCH, External Controllers (LAN etc.), FWH, SIO Controllers and Glue Chip respective reset signals.	These signals are actively driven by the 6300ESB ICH.
PXIRQ[0:3]#/ GPIO[33:36]	8.2 K $\Omega$ pull-up resistors to VCC3.3	May leave as no connect	
PXPLOCK#	8.2 K $\Omega$ pull-up resistors to VCC3.3	8.2 K $\Omega$ pull-up resistors to VCC3.3	See <i>PCI-X specification rev 1.0a</i>

**Table 113. PCI-X Interface Checklist (Sheet 3 of 3)**

Checklist Items	Recommendations	Interface Not Used	Reason/Impact
PCIXSBRST#	When utilizing this pin ensure the circuit shown in <a href="#">Section 9.14.3</a> is implemented. Connected to all devices that reside on the PCI-X bus.	May leave as no connect.	The external circuit ensures proper functionality.
IDSEL (on PCI-X Connector)	A 100 $\Omega$ series resistor on IDSEL should be connected to the PCI-X AD bus.	N/A	Improves signal quality when connected.
3.3 Vaux (on PCI-X Connector)	Leave this unconnected on the PCI-X slots.	N/A	6300ESB ICH does not support PCI-X bus power management.

## 16.7.2 PCI Interface Checklist

**Table 114. PCI Interface Checklist (Sheet 1 of 2)**

Checklist Items	Recommendations	Interface Not Used	Reason/Impact
DEVSEL#, FRAME#, IRDY#	Recommend an 8.2 K $\Omega$ pull-up resistor to $V_{CC3.3}$ or a 2.7 $\Omega$ K pull-up resistor to $V_{CC5}$ .	Recommend an 8.2 K $\Omega$ pull-up resistor to $V_{CC3.3}$ or a 2.7 $\Omega$ K pull-up resistor to $V_{CC5}$ .	See <i>PCI 2.2 Component Specification</i> pull-up recommendations for $V_{CC3.3}$ and $V_{CC5}$ .
PAR	No extra pull-up needed	Recommend an 8.2 K $\Omega$ pull-up resistor to $V_{CC3.3}$	
PCICLK	Ensure this pin is connected to a 33MHz clock output of the clock generator (CK409) through a 33 $\Omega$ resistor.	Ensure this pin is connected to a 33MHz clock output of the clock generator (CK409) through a 33 $\Omega$ resistor	This signal is not 5 V tolerant.
PERR#, PLOCK#	Recommend an 8.2 K $\Omega$ pull-up resistor to $V_{CC3.3}$ or a 2.7 $\Omega$ K pull-up resistor to $V_{CC5}$ .	Recommend an 8.2 K $\Omega$ pull-up resistor to $V_{CC3.3}$ or a 2.7 K $\Omega$ pull-up resistor to $V_{CC5}$ .	See the <i>PCI 2.2 Component Specification</i> pull-up recommendations for $V_{CC3.3}$ and $V_{CC5}$ .
PME#	No extra pull-up needed.	May leave as no connect.	PME# is in the Resume power plane and has an internal pull-up resistor. See <a href="#">section 9.14.4</a> for PME# wiring recommendations.
SERR#, STOP#, TRDY#	Recommend an 8.2 K $\Omega$ pull-up resistor to $V_{CC3.3}$ or a 2.7 K $\Omega$ pull-up resistor to $V_{CC5}$ .	Recommend an 8.2 K $\Omega$ pull-up resistor to $V_{CC3.3}$ or a 2.7 K $\Omega$ pull-up resistor to $V_{CC5}$ .	See the <i>PCI 2.2 Component Specification</i> pull-up recommendations for $V_{CC3.3}$ and $V_{CC5}$ .

Table 114. PCI Interface Checklist (Sheet 2 of 2)

Checklist Items	Recommendations	Interface Not Used	Reason/Impact
PIRQ[H:E]#/GPIO[5:2]	Recommend a 2.7 K $\Omega$ pull-up resistor to V <sub>CC5</sub> or 8.2 K $\Omega$ resistor to V <sub>CC3.3</sub> .	Recommend a 2.7 K $\Omega$ pull-up resistor to V <sub>CC5</sub> or 8.2 K $\Omega$ resistor to V <sub>CC3.3</sub> .	In Non-APIC Mode, the PIRQx# signals may be routed to interrupts 3, 4, 5, 6, 7, 9, 10, 11, 12, 14, or 15 as described in <a href="#">Section 9.13.2</a> .  Each PIRQx# line has a separate Route Control Register. (See the <i>6300ESB ICH External Design Specification</i> for more information.)  In APIC mode, these signals are connected to the internal I/O APIC in the following fashion: <ul style="list-style-type: none"> <li>PIRQ[E]# is connected to IRQ20</li> <li>PIRQ[F]# is connected to IRQ21</li> <li>PIRQ[G]# is connected to IRQ22</li> <li>PIRQ[H]# is connected to IRQ23</li> </ul>
PIRQ[A:D]#	Recommend a 2.7 K $\Omega$ pull-up resistor to V <sub>CC5</sub> or 8.2 K $\Omega$ to V <sub>CC3.3</sub> .	Recommend a 2.7 K $\Omega$ pull-up resistor to V <sub>CC5</sub> or 8.2 K $\Omega$ to V <sub>CC3.3</sub> .	In Non-APIC Mode, the PIRQx# signals may be routed to interrupts 3, 4, 5, 6, 7, 9, 10, 11, 12, 14, or 15 as described in <a href="#">Section 9.13.2</a> .  Each PIRQx# line has a separate Route Control Register. (See the <i>6300ESB ICH External Design Specification</i> for more information.)  In APIC mode, these signals are connected to the internal I/O APIC in the following fashion: <ul style="list-style-type: none"> <li>PIRQ[A]# is connected to IRQ16</li> <li>PIRQ[B]# is connected to IRQ17</li> <li>PIRQ[C]# is connected to IRQ18</li> <li>PIRQ[D]# is connected to IRQ19</li> </ul>
REQ#[0:3]	Recommend an 8.2 K $\Omega$ pull-up resistor to V <sub>CC3.3</sub> or a 2.7 K $\Omega$ pull-up resistor to V <sub>CC5</sub>	Recommend an 8.2 K $\Omega$ pull-up resistor to V <sub>CC3.3</sub> or a 2.7 K $\Omega$ pull-up resistor to V <sub>CC5</sub>	See the <i>PCI 2.2 Component Specification</i> pull-up recommendations for V <sub>CC3.3</sub> and V <sub>CC5</sub> .
GNT#[0:3]	No external pull-up resistors are required on PCI GNT signals. However, when external pull-up resistors are implemented they must be pulled up to V <sub>CC3.3</sub> .	May leave as no connect.	These signals are actively driven by the 6300ESB ICH.
AD[0:31], C/BE[0:3]#	No extra pull-up needed.	Recommend 8.2 K $\Omega$ pull-up resistors to V <sub>CC3.3</sub>	
IDSEL (on PCI Connectors)	A 300 $\Omega$ to 900 $\Omega$ series resistor on IDSEL should be connected to the PCI AD bus.	N/A	Improves signal quality when connected.

## 16.7.3 Hub Interface Checklist

**Table 115. Hub Interface Checklist**

Checklist Items	Recommendations	Reason/Impact
HI[11]	When HI_11 is not used: Pull to $V_{SS}$ through a weak pull-down resistor: <ul style="list-style-type: none"> <li>60 <math>\Omega</math> (when trace impedance is 60 <math>\Omega</math>)</li> <li>56 <math>\Omega</math> (when trace impedance is 56 <math>\Omega</math>)</li> <li>50 <math>\Omega</math> (when trace impedance is 50 <math>\Omega</math>)</li> </ul>	HI[11] will be driven by the 6300ESB ICH (should be terminated low depending on board trace resistance).
HI[0:10]	No extra pull-up resistor.	
HI_STBF	No extra pull-up resistor.	
HI_STBS	No extra pull-up resistor.	
HICLK	Ensure this pin is connected to a 66MHz clock output of the clock generator (CK409) through a 33 $\Omega$ resistor.	
HICOMP	Tie the HICOMP pin to a 52.3 $\Omega \pm 1\%$ (when trace impedance is 60 $\Omega$ ) or 48.7 $\Omega \pm 1\%$ (when trace impedance is 56 $\Omega$ ), or 43.2 $\Omega \pm 1\%$ (when impedance is 50 $\Omega$ ) pull-up resistor (to $V_{CC1\_5}$ ).	ZCOMP is no longer supported.
HIREF	350 mV (See voltage divider recommendations in <a href="#">Section 9.4.1.4.</a> )	
HI_VSWING	800 mV (See voltage divider recommendations in <a href="#">Section 9.4.1.4.</a> )	

## 16.7.4 FWH/LPC Interface Checklist

**Table 116. FWH/LPC Interface Checklist**

Checklist Items	Recommendations	Interface Not Used	Reason/Impact
FWH[0:3]/LAD[0:3]	No extra pull-ups required. Connect straight to FWH/LPC.	May leave as no connect.	6300ESB ICH integrates 20 K $\Omega$ nominal pull-up resistors on these signal lines.
LDRQ[0:1]	No extra pull-ups required. Connect straight to LPC.	May leave as no connect.	6300ESB ICH integrates 20 K $\Omega$ nominal pull-up resistors on these signal lines.
FWH[4]/LFRAME#	No extra pull-ups required. Connect straight to FWH/LPC.	May leave as no connect.	6300ESB ICH integrates 20 K $\Omega$ nominal pull-up resistors on these signal lines.
FWH Decoupling	Follow vendor recommendation.	May leave as no connect.	

## 16.7.5 GPIO Checklist

Table 117. GPIO Checklist

Checklist Items	Recommendations	Reason/Impact
GPIO Pins	<p><b>GPIO[0:7]:</b>            These pins are in the Core Power Well.            These signals are inputs thus they need to be pulled up.            Unused core well inputs must be pulled up to <math>V_{CC3.3}</math> or <math>V_{CC5}</math>.            Pull-ups (8.2 K<math>\Omega</math>) must use the <math>V_{CC3.3}</math> plane.            Pull-ups (2.7 K<math>\Omega</math>) must use the <math>V_{CC5}</math> plane.            GPIO[0:1] may be used as REQ[2:3]#.            GPIO[2:5] may be used as PIRQ[E:H]#.            Signals GPIO[0:5] are 5 V tolerant</p> <p><b>GPIO[8] and GPIO [11:13]:</b>            These pins are in the Resume Power Well. Pull-ups (8.2 K<math>\Omega</math>) must use the <math>V_{CCSUS3.3}</math> plane.            These signals are inputs thus they need to be pulled up.            Unused resume well inputs must be pulled up to <math>V_{CCSus3.3}</math>.  <b>NOTE:</b> These signals are <b>NOT</b> 5 V tolerant.</p> <p><b>GPIO[16:23]:</b>            These pins are in the Core Power Well            Fixed as output only. May be left NC.            GPIO[16:17] may be used as GNT[2:3]#.  <b>NOTE:</b> These signals are <b>NOT</b> 5 V tolerant.</p> <p><b>GPIO[24,25,27,28]:</b>            I/O pins. Default as outputs so may be left as no connect.            These pins are in the Resume Power Well.            GPIO[24,25, 28:27] From resume power well. (<b>Note:</b> Use 8.2 K<math>\Omega</math> pull-up to <math>V_{CCSus3.3}</math> when these signals are pulled up).  <b>NOTE:</b> These signals are <b>NOT</b> 5 V tolerant.</p>	Ensure ALL unconnected signals are <b>OUTPUTS ONLY!</b>
GPIO Pins	<p><b>GPIO[32:43]:</b>            I/O pins. From core power well.            Default as outputs so may be left as NC.            GPIO[32] may be used as WDT_TOUT#            GPIO[33:36] may be used as PXIRQ[0:3]#            GPIO[40:43] these GPIOs have High Strength Output Capability (for driving LEDs)  <b>NOTE:</b> These signals are <b>NOT</b> 5 V tolerant.</p> <p><b>GPIO[56:57]:</b>            Output pins. From Resume power well.            These are OD signals, use 8.2 K<math>\Omega</math> pull-ups to <math>V_{CCSus3.3}</math></p>	Ensure ALL unconnected signals are <b>OUTPUTS ONLY!</b>

## 16.7.6 USB Checklist

**Table 118. USB Checklist**

Checklist Items	Recommendations	Interface Not Used	Reason/Impact
USBP[0:3]P, USBP[0:3]N	No external resistors are required.	May leave as no connect.	Effective output driver impedance of 45 $\Omega$ provided.
OC[0:3]#	No external resistors are required.	May leave as no connect.	
USBRBIAS#	Connected to the same 22.6 $\Omega \pm 1\%$ resistor to GND as USBRBIAS.	May leave as no connect.	
USBRBIAS	22.6 $\Omega \pm 1\%$ connected to GND.	May leave as no connect.	
CLK48	Ensure this pin is connected to a 48MHz clock output of the clock generator (CK409) through a 33 $\Omega$ resistor	May leave as no connect.	

## 16.7.7 Power Management Checklist

**Table 119. Power Management Checklist (Sheet 1 of 2)**

Checklist Items	Recommendations	Reason/Impact
PWROK	Recommend a 10 K $\Omega$ pull-down to GND. This signal should be connected to power monitoring logic, and should go high no sooner than 100 ms after both $V_{CC3.3}$ and $V_{CC1\_5}$ have reached their nominal voltages.	Timing requirement.
RSMRST#	Recommend a 10 K $\Omega$ pull-down resistor to GND. This signal should be connected to power monitoring logic, and should go high no sooner than 10 ms after both $V_{CCSus3.3}$ and $V_{CCSus1\_5}$ have reached their nominal voltages.	Timing requirement.
PWRBTN#	No extra pull-up resistors.	This signal has an integrated pull-up of 18 K $\Omega$ - 42 K $\Omega$ . This signal is internally debounced inside the 6300ESB ICH.
RI#	RI# does not have an internal pull-up. Recommend an 8.2 K $\Omega$ pull-up resistor to $V_{CCSus3.3}$ .	When this signal is enabled as a wake event, it is important to keep this signal powered during the power loss event. If this signal goes low (active), when power returns the RI_STS bit will be set and the system will interpret that as a wake event.
SLP_S3#, SLP_S4#, SLP_S5#	No pull up/down resistors needed.	Driven by 6300ESB ICH.
SUS_STAT#/LPCPD#	No extra pull-up resistors.	Driven by the 6300ESB ICH.
SUSCLK	No extra pull-up resistors.	Driven by the 6300ESB ICH.

Table 119. Power Management Checklist (Sheet 2 of 2)

Checklist Items	Recommendations	Reason/Impact
SYS_RESET#	Recommend an 8.2 K $\Omega$ pull-up resistor to V <sub>CCSus</sub> 3.3. Also recommend a 100 $\Omega$ to 1 K $\Omega$ pull-down resistor isolated from SYS_RESET# by means of a normally open switch.	Input to 6300ESB ICH cannot float. This pin forces an internal reset to the 6300ESB ICH after the signal is internally debounced.
THRM#	Connect to temperature sensor. Pull-up when not used (an 8.2 K $\Omega$ pull-up resistor to V <sub>CC</sub> 3.3).	Input to 6300ESB ICH cannot float. THRM# polarity bit defaults THRM# to active low, so pull up.
THRMTRIP#	A pull-up resistor to the V <sub>CPU_IO</sub> well (62 $\Omega$ ). See Processor Design Guide to insure proper pull-up value.	Input to the 6300ESB ICH cannot float.
VRMPWRGD	A 8.2 K $\Omega$ pull-up to V <sub>cc</sub> 3.3.	

## 16.7.8 CPU Signals Checklist

**Note:** Ensure processor recommendations for the following signals are taken into consideration as well as the following recommendations.

Table 120. CPU Signals Checklist

Checklist Items	Recommendations	Reason/Impact
A20GATE	Pull-up signal to V <sub>CC</sub> 3.3 through a 10 K $\Omega$ resistor. or If software control of A20M# is desired, connect to a GPIO that is driven high at the rising edge of reset.	Typically driven by an open drain external micro-controller.  If this signal is not used pull-up to V <sub>CC</sub> 3.3 through a 10 K $\Omega$ resistor.
A20M#, CPUSLP#	No external resistors required.	Push/pull buffers now drive the output signals.
FERR#	Requires a external pull-up resistor to V <sub>CPU_IO</sub> .(62 $\Omega$ ).	
IGNNE#	No external resistors required.	Push/pull buffers now drive the output signals.
INIT#	See <a href="#">Section 12.4</a> for more information.	
INTR, NMI	No external resistors required.	Push/pull buffers now drive the output signals.
RCIN#	Pull-up signals to V <sub>CC</sub> 3.3 through a 10 K $\Omega$ resistor.	Typically driven by an open drain external micro-controller.
SERIRQ	External 8.2 K $\Omega$ pull-up resistor to V <sub>CC</sub> 3.3 is recommended.	
SMI#, STPCLK#	No external resistors required.	Push/pull buffers now drive the output signals.



## 16.7.9 System Management Checklist

Table 121. System Management Checklist

Checklist Items	Recommendations	Reason/Impact
SMBCLK, SMBDATA	<p>Typical value of pull-up resistors is 8.2 K<math>\Omega</math> to VccSus3.3.</p> <p>Value of pull-up resistors determined by line load.</p> <p>Connect SMLINK[0] to SMBCLK and SMLINK[1] to SMBDATA.</p>	<p>Requires external pull-up resistors.</p> <p>Typical value and power well determined by SMBus Architecture and Design Consideration section.</p> <p>Pull-up value also determined by bus section characteristics. Additional circuitry may be required to connect high and low power sections.</p> <p>In order to be fully compliant with the <i>SMBus 2.0 specification</i> (which requires the Host Notify cycle), the SMLink and SMBus signals <b>must</b> be tied together externally. This recommendation ensures proper functionality of the SMBus 2.0/SMLink Interface for legacy TCO and for cases when an external ASF controller is used.</p>
SMLINK[1:0]	<p>Requires external 8.2 K<math>\Omega</math> pull-up resistors to VccSus3.3.</p> <p>Connect SMLINK[0] to SMBCLK and SMLINK[1] to SMBDATA.</p>	<p>Value of pull-up resistors determined by line load.</p> <p>To be fully compliant with the <i>SMBus 2.0 specification</i> (which requires the Host Notify cycle), the SMLink and SMBus signals <b>must</b> be tied together externally. This recommendation ensures proper functionality of the SMBus 2.0/SMLink Interface for legacy TCO and for cases when an external ASF controller is used.</p>
INTRUDER#	Pull signal to V <sub>CC</sub> RTC (VBAT) through a 1 M $\Omega$ signal.	
SMBALERT#/ GPIO[11]	See GPIO section when SMBALERT# not implemented.	

## 16.7.10 RTC Checklist

Table 122. RTC Checklist

Checklist Items	Recommendations	Reason/Impact
RTCRST#	Use a 20 K $\Omega$ pull-up resistor to VccRTC and a 1.0 $\mu$ F capacitor to ground.	Time constant due to RC filter on this line should be 18-25 ms.
RTCX1, RTCX2	Connect a 32.768 kHz Crystal Oscillator across these pins with a 10 M $\Omega$ resistor. See <a href="#">Section 9.15.2</a> for capacitor guidelines.	The external circuitry shown in <a href="#">Figure 118</a> is required to maintain the RTC's accuracy. The circuitry is required since the new RTC oscillator is sensitive to step voltage changes in VCCRTC and VBIAS. A negative step on power supply of more than 100 mV will temporarily shut off the oscillator for hundreds of milliseconds.
VBIAS	Ensure the VBIAS pin of the 6300ESB ICH is connected to Vbatt through a 0.047 $\mu$ F capacitor. (See <a href="#">Section 9.15.1</a> .)	For noise immunity on VBIAS signal.

## 16.7.11 UART Checklist

Table 123. UART Checklist

Checklist Items	Recommendations	Interface Not Used	Reason/Impact
SIU0_CTS#	No extra pull-ups needed.	May leave as no connect.	
SIU1_CTS#	No extra pull-ups needed.	May leave as no connect.	Internal pull-up (15 K $\Omega$ – 35 K $\Omega$ ).
SIU0_DCD#	No extra pull-ups needed.	May leave as no connect.	
SIU1_DCD#	No extra pull-ups needed.	May leave as no connect.	Internal pull-up (15 K $\Omega$ – 35 K $\Omega$ ).
SIU0_DSR#	No extra pull-ups needed.	May leave as no connect.	
SIU1_DSR#	No extra pull-ups needed.	May leave as no connect.	Internal pull-up (15 K $\Omega$ – 35 K $\Omega$ ).
SIU0_DTR#	No extra pull-ups needed.	May leave as no connect.	Strap Function: TOP Swap (See the 6300ESB ICH External Design Specification for more information.) Pull-down to GND to use TOP Swap function. Value depends on platform specifics.
SIU1_DTR#	No extra pull-ups needed.	May leave as no connect.	Internal pull-up (15 K $\Omega$ – 35 K $\Omega$ ).
SIU0_RI#	No extra pull-ups needed.	May leave as no connect.	
SIU1_RI#	No extra pull-ups needed.	May leave as no connect.	Internal pull-up (15 K $\Omega$ – 35 K $\Omega$ ).
SIU0_RTS#	No extra pull-ups needed.	May leave as no connect.	Driven by the 6300ESB ICH. Do NOT pull down this signal.
SIU1_RTS#	No extra pull-ups needed.	May leave as no connect.	Internal pull-up (15 K $\Omega$ – 35 K $\Omega$ ).
SIU0_RXD	No extra pull-ups needed.	May leave as no connect.	
SIU1_RXD	No extra pull-ups needed.	May leave as no connect.	Internal pull-up (15 K $\Omega$ – 35 K $\Omega$ ).
SIU0_TXD	No extra pull-ups needed.	May leave as no connect.	
SIU1_TXD	No extra pull-ups needed.	May leave as no connect.	Internal pull-up (15 K $\Omega$ – 35 K $\Omega$ ).
UART_CLK	Recommend a 48 MHz clock source.	May leave as no connect.	See <a href="#">Section 9.16</a> .

## 16.7.12 AC '97 Checklist

**Table 124. AC '97 Checklist**

Checklist Items	Recommendations	Interface Not Used	Reason/Impact
AC_BITCLK	No extra pull-down resistors required. Series termination resistor 33 $\Omega$ to 47 $\Omega$ from the motherboard codec to the 6300ESB ICH.	May leave as no connect.	This pin has a weak internal 20 K $\Omega$ nominal pull-down.
AC_RST#	No extra pull-down resistor required.	May leave as no connect.	Internal pull-down (9 K $\Omega$ -50 K $\Omega$ )
AC_SDOUT	Use a jumper to an 8.2 K $\Omega$ pull-up resistor. Should not be stuffed for default operation. Series termination resistor 0 $\Omega$ to 47 $\Omega$ to the on-board codec and to the CNR.	May leave as no connect.	This pin has a weak internal 20 K $\Omega$ nominal pull-down. Strap Function: Safe Mode (See the <i>6300ESB ICH External Design Specification for more information.</i> ) To properly detect a safe mode condition, a strong pull-up will be required to override this internal pull-down.
AC_SDIN[2]	Requires a 10 K $\Omega$ pull-down to GND when a CNR card is used on the platform. Series termination resistors 33 $\Omega$ to 47 $\Omega$ from the AC_SDIN lines to the 6300ESB ICH.	May leave as no connect.	This pin has a weak internal 20 K $\Omega$ nominal pull-down. For platforms routing AC_SDIN[2] to CNR, the additional 10 K $\Omega$ pull-down is required to set the proper DC level for CNR card switching circuitry. Used for a codec detection/addressing mechanism on the CNR card.
AC_SDIN[1], AC_SDIN[0]	Internal pull-downs in the 6300ESB ICH; no external pull-downs required. Series termination resistors 0 $\Omega$ to 47 $\Omega$ from the AC_SDIN lines to the 6300ESB ICH.	May leave as no connect.	These pins have a weak internal 20 K $\Omega$ nominal pull-down.
AC_SYNC	No extra pull-down resistor required.	May leave as no connect.	Some implementations add termination for signal integrity. This signal is platform specific.

## 16.7.13 Miscellaneous Signals

Table 125. Miscellaneous Signals Checklist

Checklist Items	Recommendations	Reason/Impact
CLK14	Ensure this pin is connected to a 14 MHz clock output of the clock generator (CK409) through a 33 $\Omega$ resistor.	
SPKR	See <a href="#">Section 9.8.3</a> for more information.	Strap function: No Reboot. (See the <i>6300ESB ICH External Design Specification</i> for more information.) Has integrated pull-down. The integrated pull-down is only enabled at boot/reset for strapping functions; at all other times, the pull-down is disabled.
WDT_TOUT#/ GPIO[32]	No extra pull-down resistor required.	Driven by the 6300ESB ICH.

## 16.7.14 Serial ATA Checklist

Table 126. Serial ATA Checklist

Checklist Items	Recommendations	Interface Not Used	Reason/Impact
SATA[0:1]RXN, SATA[0:1]RXP	No extra series termination resistors or other pull-ups/pull-downs are required.	May leave as no connect.	
SATA[0:1]TXN, SATA[0:1]TXP	No extra series termination resistors or other pull-ups/pull-downs are required.	May leave as no connect.	
SATACLKN	Connect a 33 $\Omega$ series resistor between the CK409 and this signal	May leave as no connect.	
SATACLKP	Connect a 33 $\Omega$ series resistor between the CK409 this signal	May leave as no connect.	
SATALED#	Recommend a weak external pull-up to Vcc3.3	May leave as no connect.	Open Drain signal.
SATARBIASN	Short this signal with SATARBIASP at package. Connect to a 24.9 $\Omega$ $\pm 1\%$ resistor to GND.	May leave as no connect.	
SATARBIASP	Short this signal with SATARBIASN at package. This signal can be connected to the same 24.9 $\Omega$ $\pm 1\%$ resistor only if SATARBIASP is not used to connect the resistor to ground.	May leave as no connect.	See <a href="#">section 9.5.1.5</a> .

## 16.7.15 IDE Checklist

Table 127. IDE Checklist

Checklist Items	Recommendations	Interface Not Used	Reason/Impact
PDD[15:0], SDD[15:0]	No extra series termination resistors or other pull-ups/pull-downs are required. PDD7/SDD7 does not require a 10 K $\Omega$ pull-down resistor. Refer to ATA ATAPI-6 specification.	May leave as no connect.	These signals have integrated series resistors. <b>NOTE:</b> Simulation data indicates that the integrated series termination resistors are a nominal 33 $\Omega$ but may range from 21 $\Omega$ to 75 $\Omega$ .
PDDACK#, PDIOR#, PDIOW#, PDA[2:0], PDCS1#, PDCS3#, SDDACK#, SDIOR#, SDIOW#, SDA[2:0], SDCS1#, SDCS3#	No extra series termination resistors. Pads for series resistors may be implemented should the system designer have signal integrity concerns.	May leave as no connect.	These signals have integrated series resistors. <b>NOTE:</b> Simulation data indicates that the integrated series termination resistors are a nominal 33 $\Omega$ but may range from 21 $\Omega$ to 75 $\Omega$ .
PDDREQ, SDDREQ	No extra series termination resistors. No pull down resistors needed.	May leave as no connect.	These signals have integrated series resistors in the 6300ESB ICH. These signals have integrated pull down resistors in the 6300ESB ICH.
PIORDY, SIORDY	Pull-up to V <sub>CC</sub> 3.3 through 4.7 K $\Omega$ resistors. No extra series termination resistors.	Pull-up to V <sub>CC</sub> 3.3 through 4.7 K $\Omega$ resistors.	These signals have integrated series resistors in the 6300ESB ICH.
IRQ14, IRQ15	Recommend 8.2 K $\Omega$ to 10 K $\Omega$ pull-up resistors to V <sub>CC</sub> 3.3. No extra series termination resistors.	Pull-up to V <sub>CC</sub> 3.3 through 8.2 K $\Omega$ to 10 K $\Omega$ resistors.	
IDERST# (on connector)	The PCIRST# signal should be buffered to form the IDERST# signal. A 33 $\Omega$ series termination resistor is recommended on this signal.	N/A	
Cable Detect	Host Side/Device Side Detection ( <i>recommended method</i> ): Connect IDE pin PDIAG#/CBLID# to a 6300ESB ICH GPIO pin. Connect a 10 K $\Omega$ resistor to GND on the signal line. Device Side Detection: Connect a 0.047 $\mu$ F capacitor from IDE pin PDIAG#/CBLID# to GND. No 6300ESB ICH connection.	N/A	The 10 K $\Omega$ resistor to GND prevents GPI from floating when no devices are present on either IDE interface. Allows use of 3.3 V and 5 V tolerant GPIOs. <b>NOTE:</b> All Ultra DMA drives supporting modes greater than Mode 2 will have the capability to detect cables.

## 16.7.16 Power Checklist

Table 128. Power Checklist

Checklist Items	Recommendations	Reason/Impact
V <sub>CC</sub> 3.3	Use twelve 0.1 $\mu$ F and four 0.01 $\mu$ F decoupling capacitors.	
V <sub>CC</sub> 1_5	Use six 0.1 $\mu$ F and two 0.01 $\mu$ F decoupling capacitors.	
V <sub>CC</sub> Sus3.3	Use four 0.1 $\mu$ F, one 0.01 $\mu$ F, and one 1.0 $\mu$ F decoupling capacitor.	
V <sub>CC</sub> Sus1_5	Use four 0.1 $\mu$ F decoupling capacitors.	
V_CPU_IO	The power pins should be connected to the proper power plane for the CPU's CMOS Compatibility Signals. Use one 0.1 $\mu$ F decoupling capacitor.	
V <sub>CC</sub> PLL	Use three 0.1 $\mu$ F decoupling capacitors.	
V <sub>CC</sub> HI	Use two 0.1 $\mu$ F decoupling capacitors.	
VCCREF	Use one 1.0 $\mu$ F decoupling capacitor.	
V5_REF	Use one 0.1 $\mu$ F decoupling capacitor. V5REF is the reference voltage for 5 V tolerant inputs in the 6300ESB ICH. V5_REF <b>must</b> power up before or simultaneous to V <sub>CC</sub> 3.3. It must power down after or simultaneous to V <sub>CC</sub> 3.3.	For further details, see <a href="#">Section 13.3.4.4</a> . Proper connection ensures functionality of system features (i.e., USB 2.0).
V5_REF_Sus	Use one 0.1 $\mu$ F decoupling capacitor. V5_REF_Sus is the reference voltage for 5 V tolerant inputs in the 6300ESB ICH. V5_REF_Sus <b>must</b> power up before or simultaneous to V <sub>CC</sub> Sus3.3. It must power down after or simultaneous to V <sub>CC</sub> Sus3.3. For most platforms this is not an issue because V <sub>CC</sub> Sus3.3 is usually derived from V5_REF_Sus.	For further details, see <a href="#">Section 13.3.4.4</a> . Proper connection ensures functionality of system features (i.e., USB 2.0).
V <sub>CC</sub> RTC	Use two 0.1 $\mu$ F decoupling capacitors, one close to the 6300ESB ICH, and one close to the battery.  No clear CMOS jumper on V <sub>CC</sub> RTC. Use a jumper on RTCRST# or a GPI, or use a safe mode strapping for Clear CMOS.	
VCCA	Use one 0.1 $\mu$ F decoupling capacitor.	

# Layout Checklist

# 17

## 17.1 Introduction

This checklist highlights design considerations that should be reviewed prior to manufacturing a motherboard that implements the 875P MCH/E7210 MCH/6300ESB ICH chipset.

## 17.2 Platform Clock

### 17.2.1 Clock Groups

#### 17.2.1.1 HOST\_CLK Clock Group

#	Layout Recommendations	Yes	No	Comments <sup>(†)</sup>
1	HOST_CLK Skew between Agents: — 150 ps for clock driver — 150 ps for interconnect.			
2	Trace Width: 5 mils Differential Pair Spacing: 11 mils Spacing to Other Traces: 25 mils			
3	Serpentine Spacing: Maintain a minimum 25 mils. Keep parallel serpentine sections as short as possible. Minimize 90 degree bends. Make 45 degree bends if possible			
4	Motherboard Impedance - Differential 100 $\Omega$ typical			
5	Processor Routing Length: — Clock Driver to Rs; L1 - L1" = 0.5 inch Max — Rs to Rs-Rt Node; L2 - L2" = 0 - 0.2 inch — Rs-Rt Node to Rt; L3 - L3" = 0 - 0.2 inch — Rs-Rt Node to Load; L4 - L4" = 2 - 15 inches			
6	MCH Routing Length: — Clock Driver to Rs; L1 - L1" = 0.5 inch Max — Rs to Rs-Rt Node; L2 - L2" = 0 - 0.2 inch — Rs-Rt Node to Rt; L3 - L3" = 0 - 0.2 inch — Rs-Rt Node to Load; L4 - L4" = 2 inches - 15 inches			
7	Processor to MCH Length Matching (LT), Host clocks to CPU should be 150 mils longer.			
8	HOST_CLK0_HOST_CLK1 Length Matching: $\pm 10$ mils.			
9	Rs Series Termination Value: 33 $\Omega \pm 5\%$ .			
10	Rt Shunt Termination Value 49.9 $\Omega \pm 1\%$ (for 50 $\Omega$ odd mode motherboard impedance).			

<sup>†</sup> Refer to [Section 4.1.1.1](#).

## 17.2.1.2 BCLK General Routing

#	Layout Recommendations	Yes	No	Comments <sup>(†)</sup>
1	When routing 100/133/200 MHz selectable differential clocks, do not split up the two halves of a differential clock pair between layers, and rout to all agents on the same physical routing layer referenced to ground.			
2	If a layer transition is required, make sure to do simulations to determine the skew induced by the vias used to transition between routing layers is compensated in the traces to other agents.			
3	If a layer transition is required then both clock traces part must transition layers so that differential routing is maintained.			

† Refer to [Section 4.1.1.2](#).

## 17.2.2 CLK66 and CLK33 Clock Groups

### 17.2.2.1 TCLK33 Clock Group

#	Layout Recommendations	Yes	No	Comments <sup>(†)</sup>
1	Characteristic Trace Impedance: $60 \Omega \pm 15\%$			
2	Trace Width: 5 mils Trace Spacing: 10 mils			
3	6300ESB ICH, Flash BIOS, SIO, PCI slots: Trace Length - L1; 0 inch - 0.5 inch			
4	6300ESB ICH - L2; Z, 2 inches - 20 inches			
5	Flash BIOS, SIO Trace Length - L2; Z + (0 inch - 10 inches); maximum length 20 inches			
6	PCI slots Trace Length - L2; Z + (0 inch - 6 inches); maximum length 20 inches			
7	Resistor: $R1=33 \Omega \pm 5\%$			

† Refer to [Section 4.2.2](#).



### 17.2.2.2 Sharing 33 MHz Clocks

#	Layout Recommendations <sup>†</sup>	Yes	No
1	Characteristic Trace Impedance: $60 \Omega \pm 15\%$		
2	Trace Width: 5 mils Trace Spacing: 10 mils		
3	PCI down devices - L1; 0 inch - 5 inches; maximum length 20 inches		
4	PCI down devices - L2 and L3 Z + (0 inch - 7 inches); maximum length 20 inches. L2 and L3 should be length matched to within 250 mils		
5	Resistor: $33 \Omega \pm 5\%$		

<sup>†</sup> Refer to [Section 4.2.2.1](#).

### 17.2.2.3 CLK66 Clock Group

#	Layout Recommendations <sup>†</sup>	Yes	No
1	Characteristic Trace Impedance: $60 \Omega \pm 15\%$		
2	Trace Width: 5 mils Trace Spacing: 10 mils		
3	AGP connector, MCH, 6300ESB ICH, CSA Trace Length - L1; 0 inch - 0.5 inch		
4	Clock Driver to MCH, 6300ESB ICH, and GbE Trace Length - L2; Z - (0.5 inch- 0 inch); Maximum length 20 inches.		
5	Clock Driver to AGP connector Trace Length - L2; Z - (6 inches - 5 inches); maximum length 20 inches.		
7	Resistor: $33 \Omega \pm 1\%$		

<sup>†</sup> Refer to [Section 4.2.3](#).

### 17.2.2.4 CLK14 Clock Group

#	Layout Recommendations <sup>†</sup>	Yes	No
1	Characteristic Trace Impedance: $60 \Omega \pm 15\%$		
2	Trace Width: 5 mils Trace Spacing: 10 mils		
3	Trace Length - L1; 0 inch - 0.5 inch		
4	Trace Length - L2; 0 inch - 12 inches		
5	Trace Length - L3; 0 inch - 6 inches		
6	CLK14 total length (L1+L2+L3) (L1+L2+L3) to 6300ESB ICH must be within 500 mils of (L1+L2+L3) to SIO.		
7	Resistor: $33 \Omega \pm 5\%$		

<sup>†</sup> Refer to [Section 4.2.4](#).

### 17.2.2.5 DOTCLK and USBCLK Clock Group

#	Layout Recommendations <sup>†</sup>	Yes	No
1	Characteristic Trace Impedance: $60\ \Omega \pm 15\%$		
2	Trace Width: 5 mils Trace Spacing: 20 mils		
3	Trace Length - L1; 0 inch- 0.5 inch		
4	Trace Length - L2; 2 inches - 20 inches		
5	Resistor: $R1 = 22\ \Omega \pm 1\%$		
6	Skew Requirements: None - DOTCLK and USBCLK are asynchronous to any other clock on the board.		
7	Maximum via Count: 2		

<sup>†</sup> Refer to [Section 4.2.5](#).

### 17.2.2.6 SRC Clock Group

**Table 129. SRC Clock Group (Sheet 1 of 2)**

#	Layout Recommendations	Yes	No	Comments
1	Trace Width: 5 mils Differential Pair Spacing: 11 mils Spacing to Other Traces: 25 mils			<a href="#">Note 1</a>
2	Serpentine Spacing: Maintain a minimum 25 mils. Keep parallel serpentine sections as short as possible. Minimize 90 -degree bends. Make two, 45-degree bends if possible.			<a href="#">Note 1</a>
3	Motherboard Impedance - Differential: $100\ \Omega$ typical			<a href="#">Note 1</a>
4	Routing Length: — L1, L1': Clock Driver to Rs; 0.5 inch Max — L2, L2': Rs to Rs-Rt Node; 0 inch - 0.2 inch — L3, L3': Rs-Rt Node to Rt; 0 inch - 0.2 inch — L4, L4': Rs-Rt Node to Load; 2 inches- 15 inches			<a href="#">Note 1</a>
5	SCR - SCR# Length Matching: $\pm 10$ mils			<a href="#">Note 1</a>
6	Rs Series Termination Value: $33\ \Omega \pm 1\%$			<a href="#">Note 1</a>
7	Rt Shunt Termination Value: $49.9\ \Omega \pm 5\%$ (for $50\ \Omega$ odd mode motherboard impedance)			<a href="#">Note 1</a>

**NOTES:**

1. Refer to [Section 4.2.6.1](#).
2. Refer to [Section 4.2.6.2](#).

**Table 129. SRC Clock Group (Sheet 2 of 2)**

#	Layout Recommendations	Yes	No	Comments
8	When routing the 100 MHz differential clocks, do not split up the two halves of a differential clock pair between layers, and route to all agents on the same physical routing layer referenced to ground.			<a href="#">Note 2</a>
9	If a layer transition is required, make sure skew induced by the vias used to transition between routing layers is compensated in the traces to other agents.			<a href="#">Note 2</a>
10	Do not place vias between adjacent complementary clock traces, and avoid differential vias. Vias placed in one half of a differential pair must be matched by a via in the other half. Differential vias may be placed within length L1, between clock driver and Rs, if needed to shorten length L1.			<a href="#">Note 2</a>

**NOTES:**

1. Refer to [Section 4.2.6.1](#).
2. Refer to [Section 4.2.6.2](#).

## 17.2.3 Clock Driver Decoupling

#	Layout Recommendations <sup>(†)</sup>	Yes	No
1	For All power connection to planes, decoupling capacitors and vias, the MAXIMUM trace width allowable and shortest possible lengths should be used to ensure lowest possible inductance.		
2	The VSS pins should not be connected directly to the VSS side of the capacitors. They should be connected to the ground flood under the part which is viaed to the ground plane in order to avoid VDD glitches propagating out, getting coupled through the decoupling capacitors to the VSS pins. This method has been shown to provide the best clock performance.		
3	The ground flood should be viaed through the ground plane with no less than 12-16 vias under the part. It should be will connected		
4	For all power connections, heavy duty and /or dual vias should be used		
5	It is imperative that the standard signal vias and small traces not be used for connecting decoupling capacitors and ground floods to the power or ground planes		

<sup>†</sup> Refer to [Section 4.3](#).

## 17.3 System Bus

### 17.3.1 AGTL+ 4X Routing

Signal	Layout Recommendations <sup>(†)</sup>	Yes	No
D[63:0]#	Spacing: [3:1], Length: 2.5 inches to 6 inches, Ref: VSS, Impedance: $60\ \Omega \pm 15\%$ , Matching: $\pm 25$ mils (Refer to Notes 3 and 4 of <a href="#">Table 20</a> for length matching details.)		
DSTBP[3:0]#	Spacing: [4:1], Length: 2.5 inches to 6 inches, Ref: VSS, Impedance: $60\ \Omega \pm 15\%$ , Matching: $\pm 25$ mils (Refer to Notes 3 and 4 of <a href="#">Table 20</a> for length matching details.)		
DSTBN[3:0]#	Spacing: [4:1], Length: 2.5 inches to 6 inches, Ref: VSS, Impedance: $60\ \Omega \pm 15\%$ , Matching: $\pm 25$ mils (Refer to Notes 3 and 4 of <a href="#">Table 20</a> for length matching details.)		
DBI[3:0]#	Spacing: [3:1], Length: 2.5 inches to 6 inches, Ref: VSS, Impedance: $60\ \Omega \pm 15\%$ , Matching: $\pm 25$ mils (Refer to Notes 3 and 4 of <a href="#">Table 20</a> for length matching details.)		

<sup>†</sup> Refer to [Section 5.1.3.1](#).

### 17.3.2 AGTL+ 2X Routing

Signal	Layout Recommendations <sup>(†)</sup>	Yes	No
A[31:3]#	Spacing: [3:1], Length: 3 inches to 10 inches, Ref: VSS, Impedance: $60\ \Omega \pm 15\%$ , Matching: $\pm 100$ mils (Refer to Note 3 of <a href="#">Table 21</a> for length matching details.)		
ADSTB[1:0]#	Spacing: [4:1], Length: 3 inches to 10 inches, Ref: VSS, Impedance: $60\ \Omega \pm 15\%$ , Matching: $\pm 100$ mils (Refer to Note 3 of <a href="#">Table 21</a> for length matching details.)		
REQ[4:0]#	Spacing: [3:1], Length: 3 inches to 10 inches, Ref: VSS, Impedance: $60\ \Omega \pm 15\%$ , Matching: $\pm 100$ mils (Refer to Note 3 of <a href="#">Table 21</a> for length matching details.)		

<sup>†</sup> Refer to [Section 5.1.3.2](#).

### 17.3.3 AGTL+ 1X Routing

Signal	Layout Recommendations <sup>(†)</sup>	Yes	No
BPRI#	Spacing: [3:1], Length: 3 inches to 8 inches, Ref: VSS, Impedance: 60 $\Omega \pm 15\%$		
DEFER#	Spacing: [3:1], Length: 3 inches to 8 inches, Ref: VSS, Impedance: 60 $\Omega \pm 15\%$		
RS[2:0]#	Spacing: [3:1], Length: 3 inches to 8 inches, Ref: VSS, Impedance: 60 $\Omega \pm 15\%$		
TRDY#	Spacing: [3:1], Length: 3 inches to 8 inches, Ref: VSS, Impedance: 60 $\Omega \pm 15\%$		
ADS#	Spacing: [3:1], Length: 3 inches to 8 inches, Ref: VSS, Impedance: 60 $\Omega \pm 15\%$		
BNR#	Spacing: [3:1], Length: 3 inches to 8 inches, Ref: VSS, Impedance: 60 $\Omega \pm 15\%$		
DBSY#	Spacing: [3:1], Length: 3 inches to 8 inches, Ref: VSS, Impedance: 60 $\Omega \pm 15\%$		
DRDY#	Spacing: [3:1], Length: 3 inches to 8 inches, Ref: VSS, Impedance: 60 $\Omega \pm 15\%$		
HIT#	Spacing: [3:1], Length: 3 inches to 8 inches, Ref: VSS, Impedance: 60 $\Omega \pm 15\%$		
HITM#	Spacing: [3:1], Length: 3 inches to 8 inches, Ref: VSS, Impedance: 60 $\Omega \pm 15\%$		
LOCK#	Spacing: [3:1], Length: 3 inches to 8 inches, Ref: VSS, Impedance: 60 $\Omega \pm 15\%$		

<sup>†</sup> Refer to [Section 5.1.3.3](#).

## 17.3.4 Asynchronous GTL + Signals Group

Table 130. Asynchronous GTL + Signals Group (Sheet 1 of 2)

Signal	Layout Recommendations	Yes	No	Comments
THERMTRIP#	Impedance: $60\ \Omega \pm 15\%$ , Spacing: 7 mils, Width: 5 mils L1: 1" to 12", L2: 3 inches maximum, Rpu: $62\ \Omega \pm 5\%$			Refer to <a href="#">Section 5.1.6.1</a>
FERR#	Impedance: $60\ \Omega \pm 15\%$ , Spacing: 7 mils, Width: 5 mils L1: 1" to 12", L2: 3 inches maximum, Rpu: $62\ \Omega \pm 5\%$			Refer to <a href="#">Section 5.1.6.1</a>
A20M#	Impedance: $60\ \Omega \pm 15\%$ , Spacing: 7 mils, Width: 5 mils L1: 17 inches maximum			Refer to <a href="#">Section 5.1.6.2</a>
IGNNE#	Impedance: $60\ \Omega \pm 15\%$ Spacing: 7 mils, Width: 5 mils L1: 17 inches maximum			Refer to <a href="#">Section 5.1.6.2</a>
SMI#	Impedance: $60\ \Omega \pm 15\%$ Spacing: 7 mils, Width: 5 mils L1: 17 inches maximum			Refer to <a href="#">Section 5.1.6.2</a>
SLP#	Impedance: $60\ \Omega \pm 15\%$ Spacing: 7 mils, Width: 5 mils L1: 17 inches maximum			Refer to <a href="#">Section 5.1.6.2</a>
STPCLK#	Impedance: $60\ \Omega \pm 15\%$ Spacing: 7 mils, Width: 5 mils L1: 17 inches maximum			Refer to <a href="#">Section 5.1.6.2</a>
LINT[1:0]	Impedance: $60\ \Omega \pm 15\%$ Spacing: 7 mils, Width: 5 mils L1: 17 inches maximum			Refer to <a href="#">Section 5.1.6.2</a>
IERR#	Impedance: $60\ \Omega \pm 15\%$ Spacing: 7 mils, Width: 5 mils L1: 1 inch maximum, Rpu: $62\ \Omega \pm 5\%$			Refer to <a href="#">Section 5.1.6.3</a>
RESET#	Impedance: $60\ \Omega \pm 15\%$ Spacing: 13 mils, Width: 5 mils L1: 2 inches to 10 inches, L2: 1 inch to 2 inches, Rpu: $62\ \Omega \pm 5\%$			Refer to <a href="#">Section 5.1.6.4</a>
BR0#	Impedance: $60\ \Omega \pm 15\%$ Spacing: 13 mils, Width: 5 mils L1: 2 inches to 10 inches, L2: 1 inch to 2 inches, Rpu: $200\ \Omega \pm 5\%$			Refer to <a href="#">Section 5.1.6.4</a>
INIT#	Impedance: $60\ \Omega \pm 15\%$ Spacing: 7mils, Width: 5 mils L1: 17 inches max, L2: 2 inches max, L3: 10 inches max			Refer to <a href="#">Section 5.1.6.5</a>

**Table 130. Asynchronous GTL + Signals Group (Sheet 2 of 2)**

Signal	Layout Recommendations	Yes	No	Comments
PWRGOOD	Impedance: 60 $\Omega \pm 15\%$ Spacing: 13 mils, Width: 5 mils L1: 1 inch to 12 inches, L2: 3 inches maximum, Rpu: 300 $\Omega \pm 5\%$			Refer to <a href="#">Section 5.1.6.6</a>
PROCHOT	Impedance: 60 $\Omega \pm 15\%$ Spacing: 7 mils, Width: 5 mils L1: 0.75 inch max, L2: 10 inches max, L3: 10 inches max, L4: 0.5" max, Rpu: 120 $\Omega - 140 \Omega \pm 5\%$			Refer to <a href="#">Section 5.1.6.7</a>
TESTHI	Impedance: 60 $\Omega \pm 15\%$ Spacing: 7 mils, Width: 5 mils L1: 1 inch max, Rpu: 62 $\Omega \pm 5\%$			Refer to <a href="#">Section 5.1.6.8</a>
COMP[1:0]	Impedance: 60 $\Omega \pm 15\%$ Spacing: 13 mils, Width: 5 mils L1: 1.5 inches max, Rpd: 61.9 $\Omega \pm 1\%$			Refer to <a href="#">Section 5.1.6.9</a>
BOOTSELE CT	Impedance: 60 $\Omega \pm 15\%$ Spacing: 7 mils, Width: 5 mils			Refer to <a href="#">Section 5.1.6.10</a>
RESERVED	N/A			Refer to <a href="#">Section 5.1.6.11</a>
OPTIMIZED / COMPAT#	N/A			Refer to <a href="#">Section 5.1.6.12</a>

## 17.3.5 Power / Other Signals

Signal	Layout Recommendations	Yes	No	Comments
GTLVREF[3:0]	Spacing: 15 mils, Width: 12 mils L1+L2: 3.5 inches max, L3: 3 inches max, L4+L5+L6: 1.5 inches max			Refer to <a href="#">Section 5.1.6.13</a>
VID[5:0]	Spacing: 5 mils, Width: 5 mils L1+L2+L5: 15 inches max			Refer to <a href="#">Section 5.1.6.14</a>
VCCVID / VCCVIDLB	Trace connecting AF3 and AF4 should be as wide as practical, but no less than 25 mils.			Refer to <a href="#">Section 13.3.1.6</a>
VCCA / VSSA / VCCIOPLL	Trace should be a minimum of 12 mils. VCCA and VSSA should be routed together. Place decoupling capacitor with 600 mils of VCCA/ VSSA pins.			Refer to <a href="#">Section 13.3.1.7</a>
THERMDA / THERMDC	Spacing: 10 mils, Width: 10 mils. Route two lines in parallel and close together. L1: 4 inches ~ 8 inches			Refer to <a href="#">Section 5.1.6.15</a>
Host RCOMP	Spacing: 7 mils, Width: 10 mils L1: 0.5 inch max, Rpd: 20 $\Omega \pm 1\%$			Refer to <a href="#">Section 5.1.6.16</a>
Host SWING	Spacing: 10 mils, Width: 12 mils L1: 3 inches max			Refer to <a href="#">Section 5.1.6.17</a>
BSEL[1:0]	Spacing: 5 mils, Width: 5 mils			Refer to <a href="#">Section 5.1.6.18</a>

## 17.4 DDR System Memory

### 17.4.1 Clocks - SCMDCLK[5:0], SCMDCLK[5:0]#

**Note:** Designs must meet the complete layout recommendations found in [Section 6.6.2](#).

**Table 131. Clocks - SCMDCLK[5:0], SCMDCLK[5:0]# (Sheet 1 of 2)**

#	Layout Recommendations	Yes	No
1	Reference plane: Ground Referenced		
2	Layer assignment: Layers 1 and 6- Microstrip		
3	Single ended trace impedance ( $Z_0$ ): $42\ \Omega \pm 15\%$		
4	Differential mode impedance ( $Z_{diff}$ ): $70\ \Omega \pm 20\%$		
5	Nominal trace width (see exceptions for breakout region below): 8 mils		
6	Nominal pair spacing (edge to edge): 5 mils		
7	Minimum pair to pair spacing (see exceptions for breakout region below): 20 mils		
8	Minimum serpentine spacing: 20 mils		
9	Minimum spacing to other DDR signals (see exceptions for breakout region below): 20 mils		
10	Minimum isolation spacing to non-DDR signals: 20 mils		
11	Maximum via count: 2 (per side)		
12	Package length (P1): $750\ \text{mils} \pm 500\ \text{mils}$ (see package length report)		
13	Breakout length (L1): Max = 550 mils		
14	Total motherboard length limits (L1 + L2): — Min = 3.5 inches — Max = 6.5 inches		
15	Total length limits (P1 + L1 + L2): Max = 6.3 inches		
16	Clock target lengths: — Total length for DIMM0 group = X0 (See <a href="#">Section 6.2.2</a> for target reference length X0 definition) — Total length for DIMM1 group = X1 (See <a href="#">Section 6.2.2</a> for target reference length X1 definition)		



**Table 131. Clocks - SCMDCLK[5:0], SCMDCLK[5:0]# (Sheet 2 of 2)**

#	Layout Recommendations	Yes	No
17	SCLK to SCLK# length matching: Match total length to $\pm 10$ mils		
18	Clock to clock length matching (total length): — Match all DIMM0 clocks to $X0 \pm 20$ mils (See <a href="#">Section 6.2.2</a> for target reference length X0 definition) — Match all DIMM1 clocks to $X1 \pm 20$ mils (See <a href="#">Section 6.2.2</a> for target reference length X1 definition) — Maximum clock length variance = 1.0"		
19	Breakout exceptions (reduced geometries for MCH breakout region): — 5 mil trace with 5 mil pair space allowed — 5 mil pair to pair spacing allowed — 10 mil spacing to other DDR signals allowed — Maximum breakout length is 0.5"		
20	DIMM field exceptions (reduced geometries for DIMM pin field region): — 6 mil trace with 5 mil pair space allowed — Maximum reduced trace width length is 1.5" — 10 mil spacing to other DDR signals allowed — Maximum reduced spacing length is 1.0"		

## 17.4.2 Control Signals - SCKE[3:0]#, SCS[3:0]#

**Note:** Designs must meet the complete layout recommendations found in [Section 6.6.5](#).

**Table 132. Control Signals - SCKE[3:0]#, SCS[3:0]# (Sheet 1 of 2)**

#	Layout Recommendations	Yes	No
1	Reference plane: Ground Referenced		
2	Layer assignment: Layers 1 and 6- Microstrip		
3	Characteristic trace impedance ( $Z_0$ ): $60 \Omega \pm 15\%$		
4	Nominal trace width: 5 mils		
5	Minimum trace to trace spacing (see breakout and DIMM field exceptions below): 12 mils		
6	Minimum isolation spacing to non-DDR Signals: 20 mils		
7	Package length (P1): $750 \text{ mils} \pm 500 \text{ mils}$ (see package length report)		
8	Breakout Length (L1): Max = 550 mils		

**Table 132. Control Signals - SCKE[3:0]#, SCS[3:0]# (Sheet 2 of 2)**

#	Layout Recommendations	Yes	No
9	Total length (L1 + L2), MCH ball to DIMM pin: — Min = 1.5" — Max = 5.0"		
11	Trace length (L3), DIMM pin to parallel termination resistor pad: Max = 1.2"		
12	Parallel termination resistor (Rt): 47 $\Omega \pm 5\%$		
13	Maximum recommended motherboard via count per signal: 2		
14	CTRL to SCMDCLK length matching (total length including package): (CLKmax - 2.0 inches) < CTRL < (CLKmin - 0.5 inch)		
15	Breakout exceptions (reduced geometries for MCH breakout region): — 5 mil spacing to other DDR signals is allowed — Maximum breakout length is 0.5 inch		
16	DIMM field exceptions (reduced geometries for DIMM pin field region): — 6 mil spacing to other DDR signals is allowed — Maximum reduced spacing length is 1.5 inches total		

### 17.4.3 Address/Command— SMA[12:0], SBA[12:0], SRAS#, SCAS#, SWE#

**Note:** Designs must meet the complete layout recommendations found in [Section 6.6.4](#).

**Table 133. Address/Command— SMA[12:0], SBA[12:0], SRAS#, SCAS#, SWE# (Sheet 1 of 2)**

#	Layout Recommendations	Yes	No
1	Reference plane: Ground Referenced		
2	Layer assignment: Layers 1 and 6- Microstrip		
3	Characteristic trace impedance ( $Z_0$ ): — L2 segment: 50 $\Omega \pm 15\%$ — L1, L3, and L4 segments: 60 $\Omega \pm 15\%$		
4	Nominal trace width: — L2 segment: 7 mils — L1, L3, and L4 segments: 5 mils		
5	Minimum trace to trace spacing (see breakout and DIMM field exceptions below): 12 mils		
6	Minimum isolation spacing to non-DDR Signals: 20 mils		
7	Package length (P1): 750 mils $\pm$ 500 mils (see pkg length report)		

**Table 133. Address/Command— SMA[12:0], SBA[12:0], SRAS#, SCAS#, SWE# (Sheet 2 of 2)**

#	Layout Recommendations	Yes	No
8	Breakout length (L1): Max = 500 mils		
9	Total length (L1 + L2), MCH ball to 1st DIMM pin: Min = 1.5"		
10	Trace length (L3), 1st DIMM pin to Last DIMM pin: — Min = 0.2" — Max = 0.6"		
11	Total length (L1 + L2 + L3), MCH ball to last DIMM pin: Max = 5.0"		
12	Total length (P1 + L1+ L2 + L3), MCH die to last DIMM pin: Max = 5.3"		
13	Trace length (L4), last DIMM pin to parallel termination resistor pad: Max = 1.0"		
14	Parallel termination resistor (Rt): 47 $\Omega$ $\pm$ 5%		
15	Maximum recommended motherboard via count per signal: 2		
16	CMD to SCMDCLK length matching (total length including package): (CLKmax - 2.0 inches) < CMD < (CLKmin - 0.5 inch)		
17	Breakout exceptions (reduced geometries for MCH breakout region): — 5 mil spacing to other DDR signals is allowed — Maximum breakout length is 0.5 inch		
18	DIMM field exceptions (reduced geometries for DIMM pin field region): — 5 mil spacing to other DDR signals is allowed — Maximum reduced spacing length is 1.5 inches total		

## 17.4.4 Data Signals - SDQ[63:0], SDQS[8:0], SESECC[7:0]

Designs must meet the complete layout recommendations found in [Section 6.6.5](#).

**Table 134. Data Signals - SDQ[63:0], SDQS[8:0], SESECC[7:0] (Sheet 1 of 2)**

#	Layout Recommendations	Yes	No
1	Reference plane: Ground Referenced		
2	Layer assignment: Layers 1 and 6- Microstrip		
3	Characteristic trace impedance ( $Z_0$ ): — L2 segment: 50 $\Omega$ $\pm$ 15% (40 $\Omega$ for length > 5.7 inches) — L1, L3, and L4 segments: 60 $\Omega$ $\pm$ 15%		

Table 134. Data Signals - SDQ[63:0], SDQS[8:0], SESECC[7:0] (Sheet 2 of 2)

#	Layout Recommendations	Yes	No
4	Nominal trace width: — L2 segment: 7 mils (11 mils for length > 5.7 inches) — L1, L3, and L4 segments: 5 mils		
5	Minimum trace to trace spacing (see breakout and DIMM field exceptions below): — SDQ signals: 12 mils (15 mils for length > 5.7 inches) — SDQS signals: 15 mils (17 mils for length > 5.0 inches)		
6	Minimum isolation spacing to non-DDR Signals: 20 mils		
7	Package length (P1): 750 mils $\pm$ 500 mils (see package length report)		
8	Breakout length (L1): Max = 550 mils (breakout segment)		
9	Total length (L1 + L2), MCH ball to 1st DIMM Pad: Min = 1.5"		
10	Trace length (L3), 1st DIMM pad to Last DIMM pad: — Min = 0.2 inch — Max = 0.6 inch		
11	Total length (L1 + L2 + L3), MCH ball to last DIMM pad: Max = 6.5 inches		
12	Total length (P1 + L1 + L2 + L3), MCH die to last DIMM pad: Max = 6.9 inches		
13	Trace length (L4), Last DIMM pad to parallel termination resistor pad: Max = 1.0 inch		
14	Parallel termination resistor (Rt): 56 $\Omega$ $\pm$ 5%		
15	Maximum recommended motherboard via count per signal: 2		
16	SDQS to SCMDCLK length matching (total length including package): (CLKmax - 2.0 inches) < SDQS < (CLKmin + 1.0 inch)		
17	SDQ/SECC to SDQS length matching (total length including package): Match SDQ/SECC to SDQS to within $\pm$ 25 mils per byte lane		
18	Breakout exceptions (reduced geometries for MCH breakout region): 5 mil trace allowed 5 mil spacing to other DDR signals is allowed Maximum breakout length is 0.5 inch		
19	DIMM field exceptions (reduced geometries for DIMM pin field region): — 5 mil trace allowed — 5 mil spacing to other DDR signals is allowed (DQ only) — 10 mil spacing to other DDR signals is allowed (DQS only) — Maximum reduced spacing length is 2.5 inches total		

## 17.4.5 DDR Reference Voltage

### 17.4.5.1 DDR VREF at the MCH

Parameter	Layout Recommendations <sup>†</sup>	Yes	No
VREF Routing	Minimum 12 mils wide and separated from other traces by a minimum of 12-mils spacing, except during breakout, which allows for 7 mils spacing to other signals for no more than 350 mils.		
Voltage Divider	Place resistor divider consisting of two, 150 $\Omega \pm 1\%$ resistors within 1.0 inch of the MCH.		
Decoupling at the Resistor Divider	Two 2.2 $\mu\text{F}$ capacitors. Place one 2.2 $\mu\text{F}$ capacitor between SM_VREF and ground and the other between VDD (2.6 V) and ground.		
Decoupling at SM_VREF Source Pin	Place one 0.1 $\mu\text{F}$ capacitor as close as possible to the MCH SM_VREF source pin.		
Decoupling for Un-used SM_VREF Pin	Place two capacitors, a 2.2 $\mu\text{F}$ and a 0.1 $\mu\text{F}$ , on the unsourced SM_VREF pin.		

<sup>†</sup> Refer to [Section 6.8.2.1](#).

### 17.4.5.2 DDR VREF at the DIMMs

Parameter	Layout Recommendations <sup>†</sup>	Yes	No
VREF Routing	Minimum 12 mils wide and separated from other traces by a minimum of 12-mils spacing.		
Voltage Divider	Place resistor divider consisting of two 75 $\Omega \pm 1\%$ resistors within 1.0 inch of the DIMM connectors.		
Decoupling at the resistor divider	Two 0.1 $\mu\text{F}$ capacitors. Place one 0.1 $\mu\text{F}$ capacitor as close as possible to each DIMM VREF pin		

<sup>†</sup> Refer to [Section 6.8.3](#).

## 17.4.6 DDR Resistive Compensation (SMRCOMP) per-Channel

### 17.4.6.1 DDR SMRCOMP

Parameter	Layout Recommendations <sup>†</sup>	Yes	No
RCOMP Resistors	42.2 $\Omega \pm 1\%$ pulled to VDD (2.6 V), place resistors within 1.0 inch of the MCH.		
RCOMP Routing	Minimum trace width of 12 mils and minimum spacing from other signals of 10 mils.		
Decoupling	Decouple each RCOMP circuit with 2.2 $\mu\text{F}$ capacitor.		

<sup>†</sup> Refer to [Section 6.9](#).

## 17.4.6.2 DDR RCOMP VOH and VOL

Parameter	Layout Recommendations <sup>†</sup>	Yes	No
Nominal RCOMPVOH	Nominal VOH = 1.89 V $\pm$ 2%		
Nominal RCOMPVOL	Nominal VOL = 0.61 V $\pm$ 2%		
RCOMP Resistors	R1 = 3.112*R2, Recommend R2 = 10 k $\Omega$ $\pm$ 1%		
RCOMP Routing	Minimum trace width of 12 mils and minimum spacing from other signals of 10 mils		
Decoupling	Place the 0.01 $\mu$ F capacitors no more than 1 inch from the MCH, place the 1 $\mu$ F and 2.2 $\mu$ F capacitors at the resistor divider		

<sup>†</sup> Refer to [Section 6.9](#).

## 17.5 HUB Interface

### 17.5.1 8-Bit Hub Interface

#	Layout Recommendations <sup>†</sup>	Yes	No
1	Board impedance must be 60 $\Omega$ $\pm$ 15%		
2	Traces must be routed 5 mils wide with 15 mils spacing (using given example 4-layer 4.4 mil prepreg stack-up)		
3	To breakout of the MCH and 6300ESB ICH package, the Hub Interface signals may be routed 5 on 5.		
4	MCH Breakout: 5 on 5 for 2 inches Max 6300ESB ICH Breakout: 5 on 5 for 0.3 inch Max		
5	Data signals must be matched within $\pm$ 0.1 inch of the HI_STB differential pair.		
6	HI_STBS and /HI_STBF lengths must be matched.		
7a	(Single Reference Divider Circuit only) HIREF divider should be placed no more than 4 inches of away from MCH or 6300ESB ICH.		
7b	(Local Reference Divider Circuit only) HIREF dividers should be placed no more than 4 inches of away from MCH or 6300ESB ICH.		
8	HI signals must be referenced to ground.		
9	Strobe to Strobe Length Matching: $\pm$ 100 mils Data to Data Length Matching: $\pm$ 100 mils		
10	Strobe average to Data Length Matching: $\pm$ 100 mils		

<sup>†</sup> Refer to [Section 9.4](#).

## 17.5.2 Hub Interface HIVREF/HISWING

Parameter	Layout Recommendations <sup>†</sup>	Yes	No
HIVREF Voltage Specification	350 mV $\pm$ 2.0% at 1.5 V nominal		
HISWING Voltage Specification	800 mV $\pm$ 2.0% at 1.5 V nominal		
HIVREF / HISWING Divider CRT	R1 = 226 $\Omega$ $\pm$ 1%, R2 = 147 $\Omega$ $\pm$ 1%, R3 = 113 $\Omega$ $\pm$ 1% C2 and C5 = 0.1 $\mu$ F (near divider) C1, C3, C4, and C6 = 0.01 $\mu$ F (near component)		

<sup>†</sup> Refer to [Section 9.4](#).

## 17.5.3 Hub Interface Compensation

### 17.5.3.1 RCOMP Resistor Values for Hub Interface

#	Layout Recommendations <sup>†</sup>	Yes	No
1	Trace Impedance: 60 $\Omega$ $\pm$ 15%		
2	HICOMP Calculation: 52.3 $\Omega$ $\pm$ 1%		
3	VCC = 1.5 V		

<sup>†</sup> Refer to [Section 9.4](#).

## 17.6 AGP 8X (875P MCH only)

### 17.6.1 AGP 8X Routing

#### 17.6.1.1 Source Synchronous Signals

Parameter	Layout Recommendations <sup>(†)</sup>	Yes	No
Interconnect Length	Min: 0.5 inch, Max: 3.5 inches Worst-case interconnect skews listed in are based on simulations that take into account likely layout topologies and a wide range of interconnects. Listed trace lengths include pin-to-trace breakout and trace-to-connector fan-in/out.		
Strobe to Strobe (interconnect mismatch)	Max: 5 mils Worst-case interconnect skews listed in are based on simulations that take into account likely layout topologies and a wide range of interconnects. Listed trace lengths include pin-to-trace breakout and trace-to-connector fan-in/out.		
Strobe to Data	Max: 25 mils This mismatch budget applies to the combined trace lengths of the package and board signals.		
Data to Data Spacing	Min: 3/1 S/H Parameter refers to the Space-to-Height ratio of spacing between signal traces and the height above the associated ground plane.		
Strobe to Strobe Spacing	Min: 5/1 S/H Parameter refers to the Space-to-Height ratio of spacing between signal traces and the height above the associated ground plane.		
Strobe to Data Spacing	Min: 5/1 S/H Parameter refers to the Space-to-Height ratio of spacing between signal traces and the height above the associated ground plane.		
Trace Impedance	Min: 54 $\Omega$ , Max: 66 $\Omega$		
Connector Breakout	Max: 200 mils This is the fan-in/out length that does not follow the normal trace separation requirements in the connector area on the motherboard and the edge fingers of the graphic cards		
MCH Breakout	Max: 550 mils		

<sup>†</sup> Refer to [Section 7.2.2](#).



### 17.6.1.2 Common Clock Signals

Parameter	Layout Recommendations <sup>(†)</sup>	Yes	No
Interconnect Length	Min: 0.5 inch, Max: 3.5 inches Worst-case interconnect skews listed in are based on simulations that take into account likely layout topologies and a wide range of interconnects. Listed trace lengths include pin-to-trace breakout and trace-to-connector fan-in/out.		
Common Clock-to-Common Clock Spacing	Min: 2/1 S/H Parameter refers to the Space-to-Height ratio of spacing between signal traces and the height above the associated ground plane		
Common Clock-to-Data Spacing	Min: 3/1 S/H Parameter refers to the Space-to-Height ratio of spacing between signal traces and the height above the associated ground plane.		
Common Clock-to-Strobe Spacing	Min: 5/1 S/H Parameter refers to the Space-to-Height ratio of spacing between signal traces and the height above the associated ground plane.		
Trace Impedance	Min: 54 $\Omega$ , Max: 66 $\Omega$		
Connector Breakout	Max: 200 mils This is the fan-in/out length that does not follow the normal trace separation requirements in the connector area on the motherboard and the edge fingers of the graphic cards.		
MCH Breakout	Max: 550 mils		

† Refer to [Section 7.2.2](#).

## 17.7 CSA Port

### 17.7.1 CSA Port Routing

#	Layout Recommendations <sup>(†)</sup>	Yes	No
1	Characteristic Trace Impedance: 60 $\Omega \pm 15\%$		
2	Trace Width: 5 mils		
3	Trace Spacing: 15 mils		
4	L1: 2 inches to 10 inches Also includes MCH and the 82547GI chipset platform breakout length.		
5	MCH Breakout: 5 on 5 for 2 inches		
6	82547GI Controller Breakout: 5 on 5 for 300 mils		
7	Strobe-to-Strobe Length Matching: $\pm 10$ mils		
8	Strobe-to-Data Length Matching: $\pm 50$ mils		

† Refer to [Section 8.1](#).

## 17.7.2 CSA Port Generation/Distribution of Reference Voltage

#	Layout Recommendations <sup>(†)</sup>	Yes	No
1	Reference Voltage Specification (V): $0.350 \Omega \pm 3\%$		
2	Reference swing Voltage Specification (V): For MCH and 82547GI = $0.8 \Omega \pm 3\%$		
3	1.5 V Voltage Divider Circuit Recommended Resistor Values: — R1 = $226 \Omega \pm 1\%$ — R2 = $147 \Omega \pm 1\%$ — R3 = $113 \Omega \pm 1\%$		
4	1.2 V Voltage Divider Circuit Recommended Resistor Values: — R4 = $523 \Omega \pm 1\%$ — R5 = $665 \Omega \pm 1\%$ — R6 = $604 \Omega \pm 1\%$		

<sup>†</sup> Refer to [Section 8.2](#).

## 17.7.3 CSA Port Resistive Compensation

### 17.7.3.1 RCOMP Resistor Values for MCH

#	Layout Recommendations <sup>(†)</sup>	Yes	No
1	Trace Impedance: $60 \Omega \pm 15\%$		
2	RCOMP Resistor Value: R1 = $52.3 \Omega \pm 1\%$		
3	RCOMP Resistor Tied to: VCC = 1.5		

<sup>†</sup> Refer to [Section 8.3](#).

### 17.7.3.2 RCOMP Resistor Values for 82547GI Chipset Platform

#	Layout Recommendations <sup>(†)</sup>	Yes	No
1	Trace Impedance: $60 \Omega \pm 15\%$		
2	RCOMP Resistor Value: R2 = $30.0 \Omega \pm 1\%$		
3	RCOMP Resistor Tied to: VCC = 1.2		

<sup>†</sup> Refer to [Section 8.3](#).

## 17.8 Intel® 6300ESB ICH

### 17.8.1 8-Bit Hub Interface Layout Checklist

#	Layout Recommendations	Comments
1	Board impedance needs to be $60 \Omega \pm 15\%$ .	
2	Data traces need to be routed 5 mils wide with 15 mils spacing.	
3	Strobe traces need to be routed 5 mils wide with 20 mils spacing from other signals, 15 mils spacing intra-pair.	
3	In order to breakout of the MCH and 6300ESB ICH package the Hub Interface signals may be routed 5 on 5. Signals need to be separated within 300 mils of the package.	
4	Maximum trace length is eight inches.	
5	Data signals must be matched within $\pm 0.25$ inches of the HI_STB differential pair.	
6	HI_STB/HI_STBS and HI_STB#/HI_STBF lengths need to be matched.	
7a	(Single Reference Diver Circuit only) HIREF divider should be placed no more than four inches away from MCH or 6300ESB ICH.	
7b	(Local Reference Divider Circuit only) HIREF dividers should be placed no more than four inches away from MCH or 6300ESB ICH.	
8	HI signals need to be referenced to ground.	

### 17.8.2 Serial ATA Interface Layout Checklist

**Table 135. Serial ATA Interface Layout Checklist (Sheet 1 of 2)**

#	Layout Recommendations	Comments
1	Route SATA signals ground referenced.	
2	Route SATA signals using a minimum of vias and corners. This reduces signal reflections and impedance changes. Use a maximum of two vias per trace. Vias should be matched on traces within a transmit or receive pair. No vias allowed except at MCH.	
3	When it becomes necessary to turn 90°, use two 45° turns or an arc instead of making a single 90° turn. This reduces reflections on the signal by minimizing impedance discontinuities.	
4	Do not route SATA traces under crystals, oscillators, clock synthesizers, magnetic devices or ICs that use and/or duplicate clocks.	
5	Route all traces over continuous planes (GND) with no interruptions. Avoid crossing over anti-etch when possible. Crossing over anti-etch (plane splits) increases inductance and radiation levels by forcing a greater loop area. Likewise, avoid changing layers with high-speed traces (applies to SATA signals, high-speed clocks, as well as slower signals that might be coupling to them).	
6	Keep SATA signals clear of the core logic set. High current transients are produced during internal state transitions. These transients may be difficult to filter out.	

Table 135. Serial ATA Interface Layout Checklist (Sheet 2 of 2)

#	Layout Recommendations	Comments
7	Keep traces at least 90 mils away from the edge of the plane (Vcc or GND depending on which plane to which the trace is routed). This helps prevent the coupling of the signal onto adjacent wires and helps prevent free radiation of the signal from the edge of the PCB.	
8	Maintain parallelism between SATA differential signals with the trace spacing needed to achieve 79.3 $\Omega$ differential impedance. (recommended: 7 mils width, 6 mils spacing).	
9	Minimize the length of high-speed clock and periodic signal traces that run parallel to SATA signal lines to minimize crosstalk. The minimum recommended spacing to clock signals is 100 mils.	
10	Use 100 mils minimum spacing between SATA signal pairs and other signal traces. This helps to prevent crosstalk.	
11	SATA signal pair traces should be trace length matched. Max trace length mismatch between SATA signal pair (such as TXN and TXP) should be no greater than 10 mils.	
12	Maximum length from the 6300ESB ICH to the SATA connector should not be greater than eight inches.	
13	SATARBIASP and SATARBIASN should be routed 5 on 5 with a single trace 500 mils or less to the 24.9 $\Omega$ 1% resistor to ground.	

### 17.8.3 IDE Interface Layout Checklist

#	Layout Recommendations	Comments
1	Traces need to be routed 5 mils wide and 7 mils spaces	
2	Max trace length is eight inches long.	
3	The two strobe signals must be matched within 100 mils of each other. The data lines must be within $\pm 500$ mils of the average length of the two strobe signals.	
4	If series resistors are used, they should be placed close to the IDE connector.	

## 17.8.4 USB 2.0 Layout Checklist

#	Layout Recommendations	Comments
1	With minimum trace lengths, route high-speed clock and USB differential pairs first.	
2	Route USB signals ground referenced.	
3	Route USB signals using a minimum of vias and corners. This reduces signal reflections and impedance changes.	
4	When it becomes necessary to turn 90°, use two 45° turns or an arc instead of making a single 90° turn. This reduces reflections on the signal by minimizing impedance discontinuities.	
5	Do not route USB traces under crystals, oscillators, clock synthesizers, magnetic devices or ICs that use and/or duplicate clocks.	
6	Stubs on USB signals should be avoided, as stubs will cause signal reflections and affect signal quality. When a stub is unavoidable in the design, the sum of all stubs on a given data line should not be greater than 200 mils.	
7	Route all traces over continuous planes (GND) with no interruptions. Avoid crossing over anti-etch when possible. Crossing over anti-etch (plane splits) increases inductance and radiation levels by forcing a greater loop area. Likewise, avoid changing layers with high-speed traces. (Applies to USB signals, high-speed clocks, as well as slower signals that might be coupling to them.)	
8	Keep USB signals clear of the core logic set. High current transients are produced during internal state transitions, which may be difficult to filter out.	
9	Keep traces at least 90 mils away from the edge of the plane ( $V_{CC}$ or GND depending on which plane to which the trace is routed). This helps prevent the coupling of the signal onto adjacent wires and helps prevent free radiation of the signal from the edge of the PCB.	
10	Maintain parallelism between USB differential signals with the trace spacing needed to achieve the target differential impedance.	
11	Minimize the length of high-speed clock and periodic signal traces that run parallel to USB signal lines to minimize crosstalk. The minimum recommended spacing to clock signals is 100 mils.	
12	Use 45 mils minimum spacing between USB signal pairs and other signal traces. This helps to prevent crosstalk.	
13	USB signal pair traces should be trace length matched. Max trace length mismatch between USB signal pair (such as DM1 and DP1) should be no greater than 60 mils.	
14	No termination resistors are needed for USB.	
15	Short USBRBIAS and USBRBIAS# at the package, connect with a 5 mils width, 5 mils spacing single trace 500 mils or less to the 22.6 $\Omega$ 1% resistor to ground.	
16	Maximum length from the 6300ESB ICH to the backpanel should not exceed recommended length.	
17	Maximum length from the 6300ESB ICH to the CNR should not exceed recommended length.	
18	Maximum length from the 6300ESB ICH to the Front Panel connector should not exceed recommended length.	

## 17.8.5 AC '97 Layout Checklist

#	Layout Recommendations	Comments
1	Target Board Impedance AC '97 = $60\ \Omega \pm 15\%$	
2	5 mils trace width, 10 mils spacing between traces	
3	AC_SDIN Max Trace Length 6300ESB ICH to the Primary Codec or CNR connector = 14 inches	
4	AC_SDOOUT Max trace length 6300ESB ICH to the Primary Codec or CNR connector = 14 inches	
5	AC_BIT_CLK Max trace length 6300ESB ICH to the Primary Codec or CNR connector = 14 inches	
6	Series termination resistor on AC_BIT_CLK line should be no more than 3.0 to 8.0 inches from the 6300ESB ICH.	

## 17.8.6 RTC Layout Checklist

#	Layout Recommendations	Comments
1	RTC LEAD length = one inch maximum	
2	Minimize capacitance between RTCX1 and RTCX2.	
3	Put GND plane underneath Crystal components.	
4	Don't route switching signals under the external components (unless on other side of board).	
5	RTC signals should be ground referenced.	

## 17.8.7 PCI-X Layout Checklist

#	Layout Recommendations	Comments
1	Eight inches maximum to the first slot, then 1.5 inches to each subsequent slot. PCI-X clocks and loop-back clocks are scaled accordingly. (See <a href="#">Figure 111</a> through <a href="#">Figure 113</a> for more information.)	
2	Place the PXRCOMP pull-down resistor as close to the 6300ESB ICH as possible.	
3	IDSEL (See <a href="#">Section 9.14.2.</a> )	
4	Signals should be routed with 5 mils trace width and 12 mils spacing.	

## 17.8.8 PCI Layout Checklist

#	Layout Recommendations	Comments
1	Ten inches maximum to the first slot, then one inch to each subsequent slot. PCI clocks and loop-back clocks are scaled accordingly. (See <a href="#">Figure 111</a> for more information.)	
3	Signals should be routed with 5 mils trace width and 7 mils spacing.	
3	Clock signals should be routed with 5 mils trace width and 50 mils spacing.	
4	IDSEL (See <a href="#">Section 9.4.1</a> for more information.)	

## 17.8.9 FWH Decoupling Layout Checklist

#	Layout Recommendations	Comments
1	0.1 $\mu$ F capacitors should be placed between the $V_{CC}$ supply pins and the $V_{SS}$ ground pins, and no less than 390 mils from the $V_{CC}$ supply pins.	
2	4.7 $\mu$ F capacitors should be placed between the $V_{CC}$ supply pins and the $V_{SS}$ ground pins, and no less than 390 mils from the $V_{CC}$ supply pins.	

## 17.9 Power Distribution

### 17.9.1 Power Delivery

**Table 136. Power Delivery Recommendations (Sheet 1 of 3)**

Signal	Layout Recommendations	Yes	No	Comments
VCC (CPU Core) CPU Core VTT	The VCC (CPU core) power plane is used to power the CPU core and VTT. The processor's voltage regulator must be compatible with either a VRM 10 or a VRD 10.0 design.			Refer to <a href="#">Section 13.2.1</a> .
MCH_VTT	When a Pentium 4 processor with HT Technology is inserted into the platform, the output of the MCH_VTT regulator should be set to 1.225 V and if a Pentium 4 Processor is inserted into the platform, the output of the MCH_VTT regulator should be set to 1.45 V. This regulator must be able to source 2 A and sink 600 mA in normal operation.			Refer to <a href="#">Section 13.2.2</a> .
VCCVID CPU VID	VCCVID is a 1.2 V power plane is used to power pins AF4 and AF3 on the processor. It is derived from 3.3 V and should be able to source 150 mA of current. This regulator is required for all designs.			Refer to <a href="#">Section 13.2.3</a> .

Table 136. Power Delivery Recommendations (Sheet 2 of 3)

Signal	Layout Recommendations	Yes	No	Comments
2.55 V Dual DDR Core	The 2.55 V dual power plane is used to provide power to the DDR DRAM core, the MCH DDR I/O ring, reference voltage to the 1.3 V linear regulator, and the 2.55 V to 1.5 V linear regulator. The 2.55 V power plane is created using a switch between a switching regulator and a linear stand-by regulator. The switching regulator should be able to support up to 19.5 A of current while the stand-by regulator needs only to supply 500 mA of current. The switching regulator receives its input directly from the 5 V power rail of the power supply while the linear regulator receives its input from 5 V SB. The DDR DRAM VDD and VDDQ requires at most 13 A of current in the S1 state. The current dedicated for the 875P MCH/E7210 MCH MCH's VCC_2.55 is 4.9 A.			Refer to <a href="#">Section 13.2.4</a> .
1.275 V DDR_TERM	The 1.275 V voltage regulator is for the DDR termination voltage (VTERM). A linear regulator divides the 2.55 V power rail by 2 to drive a 1.275 V reference voltage. VTERM is defined as: $VTERM_{min} = SMVREF - 40\text{ mV}$ and $VTERM_{max} = SMVREF + 40\text{ mV}$ . By deriving the VTERM voltage from the 2.55 V plane, this provides some common mode noise rejection between the DDR termination and I/O voltages. The entire power plane requires 1.8 A of current, and may be delivered a couple of different ways. One way is to use two regulators, one for each channel or one regulator for both channels.			Refer to <a href="#">Section 13.2.5</a> .
1.5 V CONN	The 1.5 V power plane is created using a dual linear regulator sourcing from the 2.55 V power rail. The 1.5 V plane powers the 6300ESB ICH core logic and HI, the MCH core, HI, CSA, AGP, and the AGP Connector. Sequencing on this rail should ensure that the 1.5 V power plane is shut off during S3. This voltage rail requires approximately 6.6 A maximum current. This regulator is required in all designs.			Refer to <a href="#">Section 13.2.6</a> .
5 V DUAL	This rail will be powered from the 5 V core ATX supply during full-power operation and from 5 V SB during STR. There is a resistive drop through the 5 V dual w/switch that must be considered. Therefore, no components should be connected directly to the 5 V dual plane.			Refer to <a href="#">Section 13.2.7</a> .



Table 136. Power Delivery Recommendations (Sheet 3 of 3)

Signal	Layout Recommendations	Yes	No	Comments
5 V SB (STANDBY)	The 5 V SB power plane comes directly off the 5 V SB power rail from the ATX power supply and has two functions. One, to provide power to resume functions via a 3.3 V SB regulator in I/O devices off of the 6300ESB ICH, and two, to provide 2.55 V power to the memory devices during the S3 state. The 6300ESB ICH requires 3.3 V SB only due to the integrated 1.5 V SB regulator. It is recommended that the ATX power supply be capable of handling 2 A of SB current.			Refer to <a href="#">Section 13.2.8</a> .
3.3 V SB (STANDBY)	The 3.3 V SB power plane is the output of a 5 V SB-to-3.3 V SB voltage regulator. The 3.3 V SB plane powers the resume well of the 6300ESB ICH and the PCI 3.3 VAUX suspend power pins. The 3.3 VAUX requirements state that during suspend, the system must deliver 375 mA to each wake-enabled card and 20 mA to each non-wake enabled card. During full-power operation, the system must be able to supply 375 mA to each card. Therefore, the total requirement is: — Full-power operation: 375 mA *(# of PCI slots) — Suspend operation: 375 mA+20 mA* (#PCI slots-1)			Refer to <a href="#">Section 13.2.9</a> .
2.55 V SB (STANDBY)	The 2.55 V SB power plane is the output of the 5 V SB-to-2.55 V SB voltage regulator. The power plane is used solely for the DDR DIMMs during the S3 suspend state (some minimal 2.55 V rail current will also be supplied to the MCH). The suspend voltage regulator for system memory is controlled by the LATCHED_BACKFEED_CUT signal. This signal should be generated using the SLP_S4# signal from the 6300ESB ICH, rather than the SLP_S5# signal, even if the platform does not support the S4 Sleep State. The SLP_S4# logic in the 6300ESB ICH ensures that system memory will be properly initialized when returning from S4 and S5 states.			Refer to <a href="#">Section 13.2.10</a> .

## 17.9.2 Decoupling Requirements

Signal	Layout Recommendations <sup>†</sup>	Yes	No
AL Polymer 560 $\mu$ F	10 capacitor, ESR: 5 m $\Omega$ , ESL: 4 nH, Filter: Output		
1206 pkg 22 $\mu$ F X5R	24 capacitor, ESR: 3.5 m $\Omega$ , ESL: 1.4 nH, Filter: Output		
Al Electrolytic 1200 $\mu$ F 16 V 2.1 A Ripple	4 capacitor, ESR: 22 m $\Omega$ , ESL: 30 nH, Filter: Input		
1206 pkg 4.7 $\mu$ F	4 capacitor, ESR: 6 m $\Omega$ , ESL: 1.1 nH, Filter: Input		

<sup>†</sup> Refer to [Section 13.3.1.2](#).

## 17.9.3 MCH Power Delivery

### 17.9.3.1 Decoupling Requirements

Signal	Layout Recommendations <sup>†</sup>	Yes	No
MCH_VTT	(1) 0.47 $\mu$ F edge capacitors as close to ball A15 (1) 0.47 $\mu$ F edge capacitors as close to ball A21 (1) 0.1 $\mu$ F edge capacitors as close to ball A31 (1) 0.1 $\mu$ F power plane decoupling as close to MCH		
VCC_1.5 HI AGP, CSA	(1) 0.1 $\mu$ F edge capacitors as close to ball AA35 (1) 0.1 $\mu$ F edge capacitors as close to ball Y1		
VCC_2.55 DDR	(1) 0.1 $\mu$ F edge capacitors as close to ball AA35 (1) 0.47 $\mu$ F edge capacitors as close to ball E35 (1) 0.22 $\mu$ F edge capacitors as close to ball R35 (1) 0.1 $\mu$ F edge capacitors as close to ball AL35 (1) 0.1 $\mu$ F edge capacitors as close to ball AR15 (1) 0.1 $\mu$ F edge capacitors as close to MCH		

<sup>†</sup> Refer to [Section 13.3.2.4](#).

### 17.9.3.2 Bulk Decoupling Requirements

Signal	Layout Recommendations <sup>†</sup>	Yes	No
MCH_VTT	(1) 0.1 $\mu$ F, (1) 0.47 $\mu$ F, (1) 1.0 $\mu$ F, (2) 4.7 $\mu$ F, (1) 470 $\mu$ F. Place on MCH VTT plane using good layout practices. such as placing the smaller value capacitors closer to the MCH than the higher value capacitors.		
VCC_2.55	(1) 22 $\mu$ F, (1) 4.7 $\mu$ F Place at the 2.55 V power plane transitions to layer 1 at the MCH.		
VCC_1.5	10 $\mu$ F, 470 $\mu$ F, 4.7 $\mu$ F Place as close to where the 1.5 V core and 1.5 V AGP/CSA planes diverge. Place at the output of the 1.5 V VR. Place between the VR and the MCH.		

<sup>†</sup> Refer to [Section 13.3.2.4](#).

## 17.9.4 DDR DIMM Power Delivery

### 17.9.4.1 Decoupling Requirements

Signal	Layout Recommendations <sup>†</sup>	Yes	No
VCC_2.55	(42) 0.1 $\mu$ F decoupling capacitors Place as close to power the DIMM power pins as possible and sprinkled through out the DDR power flood.		
DDR_TERM	(54) 0.1 $\mu$ F decoupling capacitors Place as close to termination resistors as possible.		

<sup>†</sup> Refer to [Section 13.3.5.3](#).

### 17.9.4.2 Bulk Decoupling for DIMMs

Pin	Layout Recommendations <sup>†</sup>	Yes	No
VCC_2.55	(1) 4.7 $\mu$ F, (1) 22 $\mu$ F, (1) 333 $\mu$ F, (1) 560 $\mu$ F: Place at output of the VR as close to the DIMMs as possible: (4) 470 $\mu$ F: Place at each corner of the DIMMs.		
DDR_TERM	(1) 4.7 $\mu$ F, (1) 470 $\mu$ F, (1) 1500 $\mu$ F. Place at output of the VR as close to the DIMMs as possible.		

<sup>†</sup> Refer to [Section 13.3.5.3](#).

## 17.9.5 ICH Power Delivery

### 17.9.5.1 Power Delivery Checklist

#	Layout Recommendations <sup>†</sup>	Yes	No
1	Standby power rails (V5REF_Sus and VccSus3_3) should be implemented through planes. Will reduce trace antennae effect.		
2	Decoupling capacitors should be placed as close as possible to the package (100 mils nominal.) See <a href="#">Section 13.3.4.8</a> for more details on capacitor placement.		

<sup>†</sup> Refer to [Section 13.3.4.8](#)

### 17.9.5.2 Decoupling Requirements

Signal	Layout Recommendations <sup>†</sup>	Yes	No
VCC3_3	(6) 0.1 $\mu$ F decoupling capacitors (VSS) Place near balls D1, A7, H1, P1, W24, and AD 21.		
VCCSUS3_3	(3) 0.1 $\mu$ F, (1) 0.01 $\mu$ F, (1) 1.0 $\mu$ F decoupling capacitors (VSS) Place 0.1 $\mu$ F capacitors near balls A17, A23, and V1. Place additional capacitors near balls A15 and A19.		
V_CPU_IO	(1) 0.1 $\mu$ F decoupling capacitors (VCC) Place near balls T24.		
VCC1_5	(4) 0.1 $\mu$ F, (1) 0.01 $\mu$ F decoupling capacitors (VSS) Place 0.1 $\mu$ F capacitors near balls G24, H24, K24, M24, AD4, and AD18. Place 0.01 $\mu$ F capacitor near balls AD8.		
VCCSUS1_5_A	(1) 0.01 $\mu$ F decoupling capacitors (VSS) Place near balls A19.		
VCCSUS1_5_B	(1) 0.01 $\mu$ F decoupling capacitors (VSS) Place near balls AD4.		
VCCSUS1_5_C	(1) 0.01 $\mu$ F decoupling capacitors (VSS) Place near balls A7.		
V5REF	(1) 0.1 $\mu$ F decoupling capacitors (VCC) Place near balls A8.		
V5REF_SUS	(1) 0.1 $\mu$ F decoupling capacitors (VSS) Place near balls A17.		
VCCRTC	(1) 0.1 $\mu$ F decoupling capacitors (VCC) Place near balls AD11.		
VCCUSBPLL	(1) 0.1 $\mu$ F, (1) 0.01 $\mu$ F decoupling capacitors (VSS) Place near balls D24.		
VCCSATAPLL	(1) 0.1 $\mu$ F, (1) 0.01 $\mu$ F decoupling capacitors (VSS) Place near balls AD6.		

<sup>†</sup> Refer to [Section 13.3.4.8](#).

# Reference Schematics

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18

The following pages contain schematics for all major functional components of the Intel® 875P/E7210/6300ESB chipset platform.

The page immediately following lists all of the schematics and their page numbers. (Note that page numbering in the following pages is not consecutive with the rest of this document.)

8		7	6	5	4	3	2	1
D	PAGE #	COMPONENT/FUNCTION					INTEL(R) 875P MCH	
	1	COVER PAGE.					INTEL(R) 875P MCH / 6300ESB ICH  CUSTOMER REFERENCE BOARD AND VALIDATION PLATFORM  FAB D  REV 1.3	
	2	TABLES: BLOCK DIAGRAM						
	3	TABLES: RESET MAP						
	4	TABLES: CLOCK DISTRIBUTION						
	5	TABLES: GPIO/IDSEL MAPPING						
	6	CORE: CPU CONNECTOR						
	7	CORE: CPU TERMINATION & MISC P/U, P/D						
	8	CORE: CPU-UCCP FILTGERED ANALOG SUPPLY						
	9-14	CORE: Intel® 875P MCH						
C	15	CORE: MCH ANALOG FILTERS					INFORMATION IN THIS DOCUMENT IS PROVIDED IN CONNECTION WITH INTEL(R) PRODUCTS. PROPERTY RIGHTS IS GRANTED BY THIS DOCUMENT. EXCEPT AS PROVIDED IN INTEL'S TERMS NO LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE, TO ANY INTELLECTUAL AND CONDITIONS OF SALE FOR SUCH PRODUCTS. INTEL ASSUMES NO LIABILITY WHATSOEVER, AND INTEL DISCLAIMS ANY EXPRESS OR IMPLIED WARRANTY, RELATING TO SALE AND/OR USE OF INTEL PRODUCTS INCLUDING LIABILITY OR WARRANTIES RELATING TO FITNESS FOR A PARTICULAR PURPOSE, MERCHANTABILITY, OR INFRINGEMENT OF ANY PATENT, COPYRIGHT OR OTHER INTELLECTUAL PROPERTY RIGHT. INTEL PRODUCTS ARE NOT INTENDED FOR USE IN MEDICAL, LIFE SAVING, OR LIFE SUSTAINING APPLICATIONS.  INTEL MAY MAKE CHANGES TO SPECIFICATIONS AND PRODUCT DESCRIPTIONS AT ANY TIME WITHOUT NOTICE. DESIGNERS MUST NOT RELY ON THE ABSENCE OR CHARACTERISTICS OF ANY FEATURES OR INSTRUCTIONS MARKED RESERVED OR UNDEFINED. INTEL RESERVES THESE FOR FUTURE DEFINITION AND SHALL HAVE NO RESPONSIBILITY WHATSOEVER FOR CONFLICTS OR INCOMPATIBILITIES ARISING FROM FUTURE CHANGES TO THEM.  THE INTEL(R) PENTIUM 4 PROCESSOR AND THE INTEL(R) 875P CHIPSET PLATFORM MAY CONTAIN DESIGN DEFECTS OR ERRORS KNOWN AS ERRATA WHICH MAY CAUSE THE PRODUCT TO DEVIATE FROM PUBLISHED SPECIFICATIONS. CURRENT CHARACTERIZED ERRATA ARE AVAILABLE ON REQUEST.  CONTACT YOUR LOCAL INTEL SALES OFFICE OR YOUR DISTRIBUTOR TO OBTAIN THE LATEST SPECIFICATIONS AND BEFORE PLACING YOUR PRODUCT ORDER. COPIES OF DOCUMENTS WHICH HAVE AN ORDERING NUMBER AND ARE REFERENCED IN THIS DOCUMENT, OR OTHER INTEL LITERATURE, MAY BE OBTAINED FROM: INTEL CORPORATION WWW.INTEL.COM OR CALL 1-800-548-4725 INTEL AND PENTIUM 4 ARE TRADEMARKS OR REGISTERED TRADEMARKS OF INTEL CORPORATIONS OR ITS SUBSIDIARIES IN THE UNITED STATES AND OTHER COUNTRIES. *OTHER NAMES AND BRANDS MAY BE CLAIMED AS THE PROPERTY OF OTHERS	
	16	CORE: MCH DECOUPLING AND COMPS						
	17	CORE: CK_409 (MAIN CLOCK GENERATOR)						
	18	CORE: AGP 4X/8X CONN						
	19	CORE: AGP SWING / UREF						
	20	CORE: DDR CHANNEL A DIMM CONNECTORS (0/1)						
	21-22	CORE: DDR CHANNEL A SERIES TERMINATION						
	23	CORE: DDR CHANNEL A UTERM DECOUPLING						
	24	CORE: DDR CHANNEL B DIMM CONNECTORS (0/1)						
	25-26	CORE: DDR CHANNEL B SERIES TERMINATION						
B	27	CORE: DDR CHANNEL B UTERM DECOUPLING					CONTACT YOUR LOCAL INTEL SALES OFFICE OR YOUR DISTRIBUTOR TO OBTAIN THE LATEST SPECIFICATIONS AND BEFORE PLACING YOUR PRODUCT ORDER. COPIES OF DOCUMENTS WHICH HAVE AN ORDERING NUMBER AND ARE REFERENCED IN THIS DOCUMENT, OR OTHER INTEL LITERATURE, MAY BE OBTAINED FROM: INTEL CORPORATION WWW.INTEL.COM OR CALL 1-800-548-4725 INTEL AND PENTIUM 4 ARE TRADEMARKS OR REGISTERED TRADEMARKS OF INTEL CORPORATIONS OR ITS SUBSIDIARIES IN THE UNITED STATES AND OTHER COUNTRIES. *OTHER NAMES AND BRANDS MAY BE CLAIMED AS THE PROPERTY OF OTHERS	B
	28	ICH: PCI, IDE, LPC BLOCKS						
	29	ICH: HOST, SATA, GPIO, SMBUS, CONTROL, PCI-X						
	30	ICH: HUBLINK, USB, GPIO, SERIAL, AC'97						
	31-32	ICH: POWER, GROUND, DECOPLING, AND PULLUPS						
	33	ICH: GPIO HEADERS						
	34	ICH: IDE PRIMARY & SECONDARY						
	35	ICH: USB OPTION (FRONT PANEL OR CNR)						
	36	ICH: USB FRONT PANEL/CNR VREG & OVER CURRENT						
	37	ICH: USB BACK PANEL LEFT (MAGJACK) & FNT PNL						
A	38-42	ICH: PCI-X SLOTS 1-2 & PCI SLOTS 1 - 3					SCHEMATIC TITLE: INTEL(R) 875P/6300ESB CUSTOMER REFERENCE BOARD PAGE TITLE: TITLE PAGE  INTEL 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630  LAST REVISED: 02.04.2004  REV: 1.3  SHEET: 1/90	A
	43-46	ICH: PCI-X DEVICE DOWN (GIGABIT ETHERNET CONTROLLER LAN)						
	47	ICH: PCI-X TERMINATION						
	48	ICH: PCI TERMINATION						
	49	CNR: CNR CONNECTOR						
	50-52	LAN: INTEL(R) 82547GI LAN SOLUTION						
	53	LAN: MAGJACK3/USB CONNECTOR AND DIFF PAIR TERM.						
	54	LAN: CSA INTERFACE REFERENCE						
	55	AUDIO: CODEC (AD1980, AD1981A, CS4202, STAC9752)						
	56	AUDIO: CODEC FILTERING CAPS						
	57	AUDIO: CD-IN ATAPI HEADER, LINE-IN CONN.					NOTES:  1. THIS SCHEMATIC DOCUMENTS THE GENERIC PRODUCT WITH ALL POSSIBLE CONFIGURATIONS. PLEASE REFER TO SPECIFIC PRODUCT PBA EPLs FOR ITEMS SHOWN AS OPTIONAL IN THE SCHEMATIC.  2. RESISTORS ARE IN OHMS UNLESS OTHERWISE SPECIFIED.  3. VCC = +5V UNLESS OTHERWISE SPECIFIED.  4. * SUFFIX INDICATES ACTIVE LOW SIGNAL.  5. \I SUFFIX INDICATES SIGNAL EXITS HIERARCHICAL BLOCK.  6. THIS DOCUMENT ALSO EXISTS ON ELECTRONIC MEDIA.	
	58	AUDIO: LINE-OUT CONNECTOR						
	59	AUDIO: MIC-IN CONN., FRONT PANEL AUDIO HEADER						
	60	AUDIO: 6 CH HEADER						
	61	AUDIO: LINE-OUT/HP JACK SENSE						
	62	AUDIO: AUDIO VREG						
POWER SYMBOLS USED: VCC3 VCC +12V -12V								
8		7	6	5	4	3	2	1



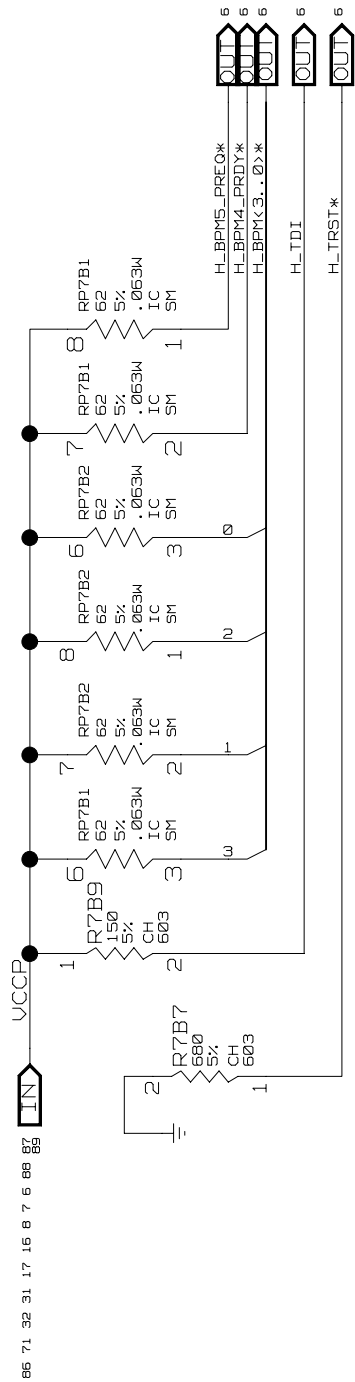
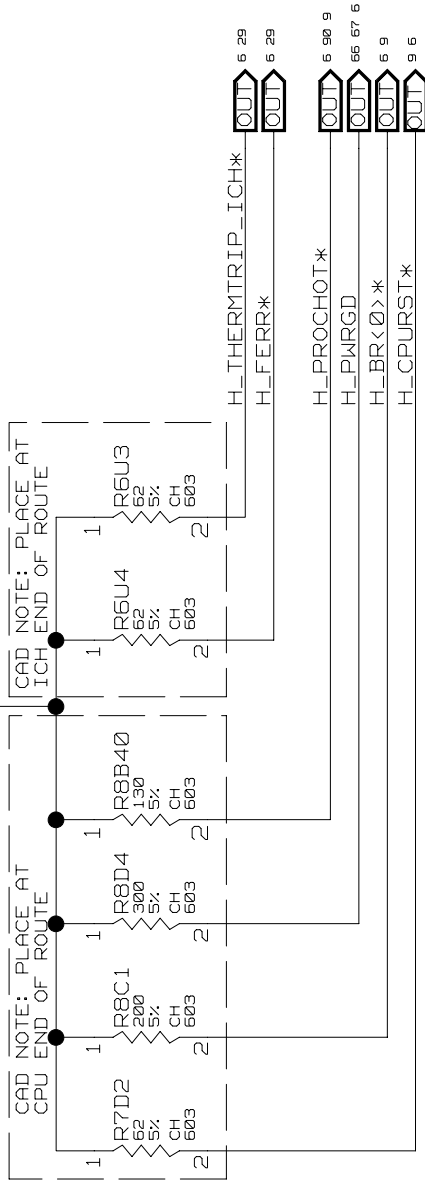
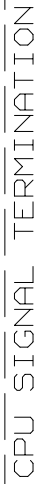




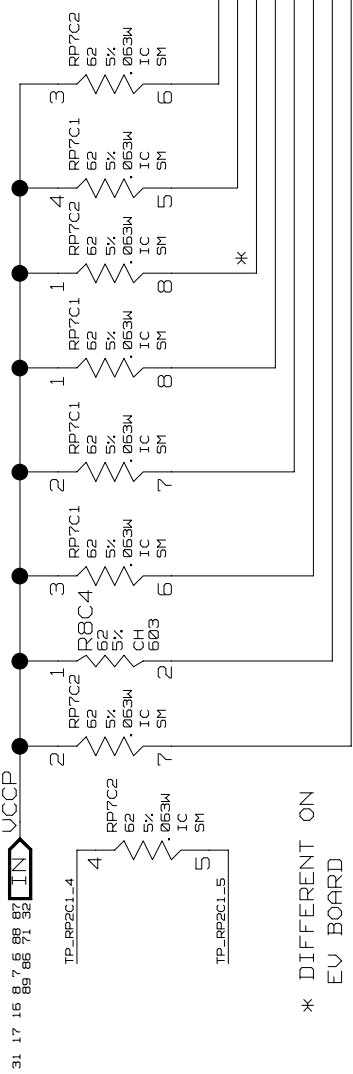






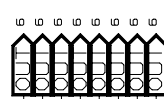


CAD NOTE: PLACE THESE RESISTORS CLOSE TO THE CPU SOCKET



\* DIFFERENT ON  
EV BOARD

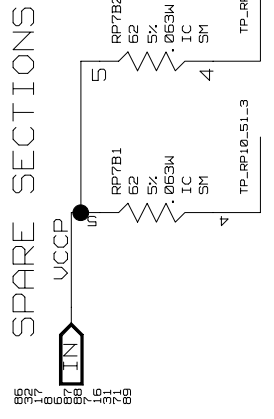
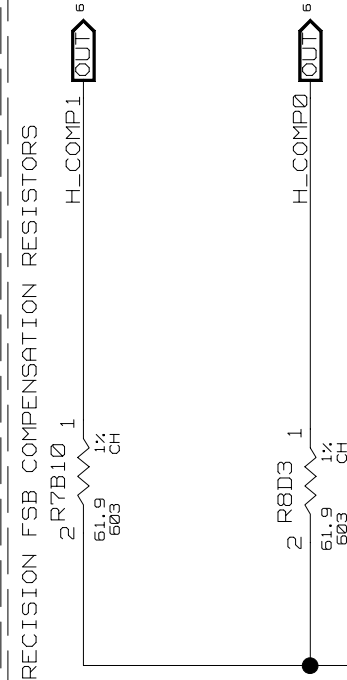
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TESTHI[1]		ODT
TESTHI[5:2]		MCLKC3:
TESTHI[7:6]		MCLKIO[
TESTHI[10:8]		BR#[3:1
TESTHI[11]		GHI#
TESTHI[12]		DPSLP#



\* DIFFERENT ON  
EV BOARD - STUFFED

NEVER JUMPER  
THIS HEADER!!!

CAD NOTE:  
PLACE HEADER AS CLO



PLACE RESISTORS OUTSIDE SOCKET CAVITY  
IF NO ROOM FOR VARIABLE RESISTOR DO NOT PLACE.

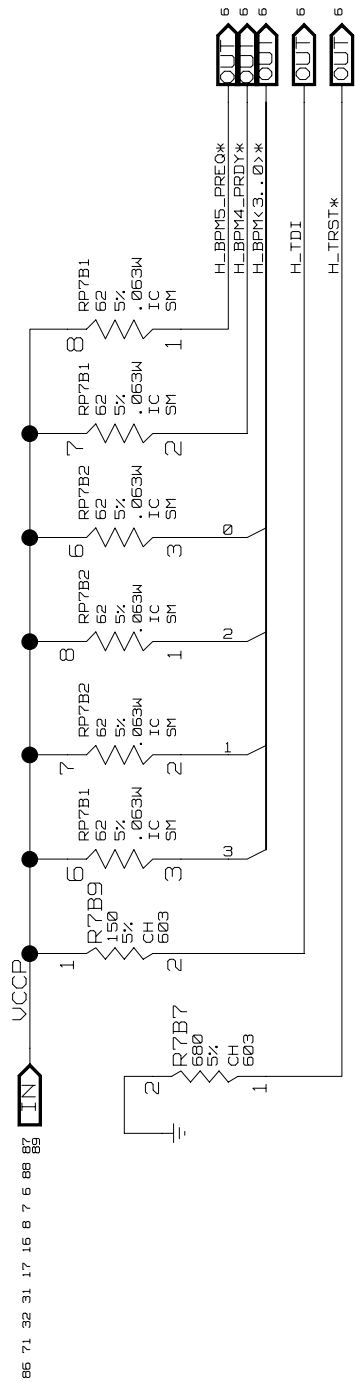
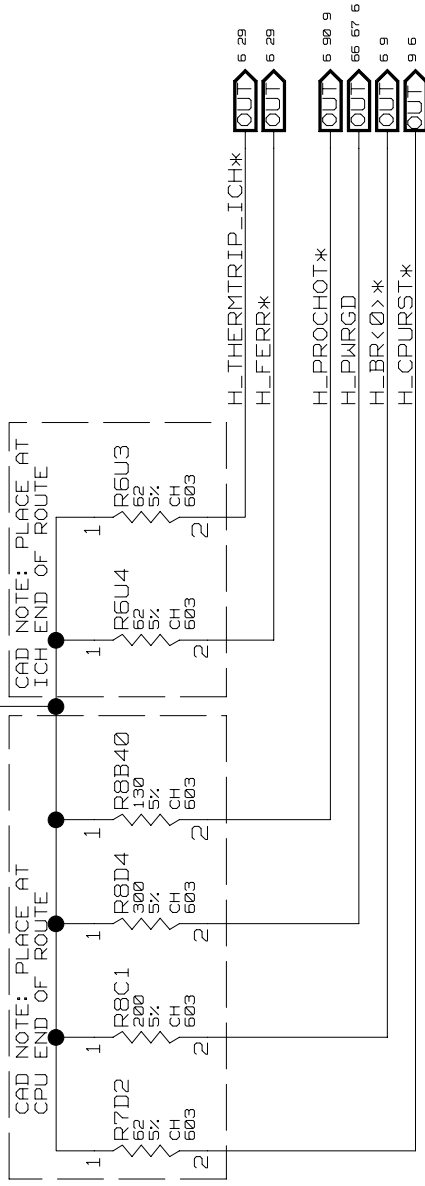
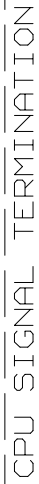
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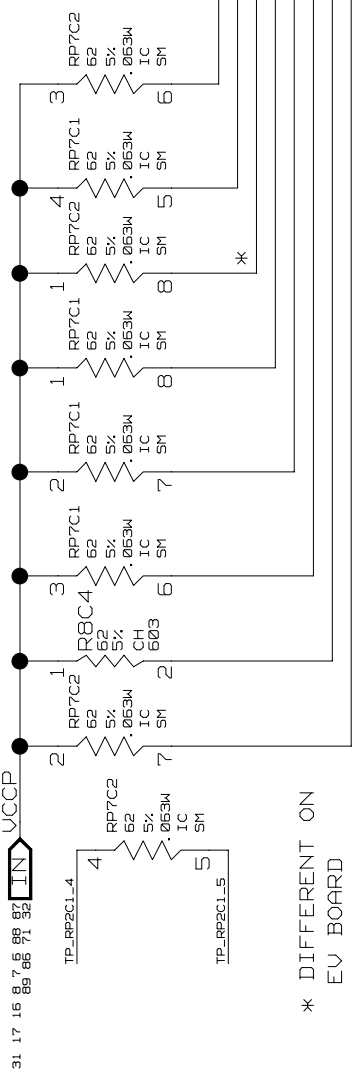
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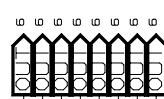


CAD NOTE: PLACE THESE RESISTORS CLOSE TO THE CPU SOCKET



\* DIFFERENT ON  
EV BOARD

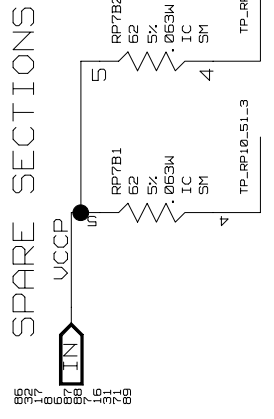
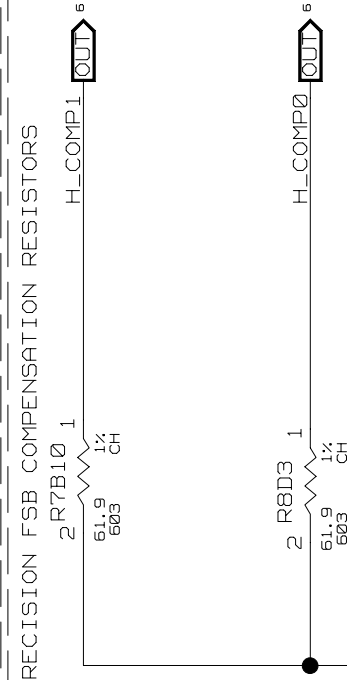
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TESTHI[0]		BPYPASSE
TESTHI[1]		ODT
TESTHI[5:2]		MCLKC3:
TESTHI[7:6]		MCLKIO[
TESTHI[10:8]		BR#[3:1
TESTHI[11]		GHI#
TESTHI[12]		DPSP#



\* DIFFERENT ON  
EV BOARD - STUFFED

NEVER JUMPER  
THIS HEADER!!!

CAD NOTE:  
PLACE HEADER AS CLO



PLACE RESISTORS OUTSIDE SOCKET CAVITY  
IF NO ROOM FOR VARIABLE RESISTOR DO NOT PLACE.

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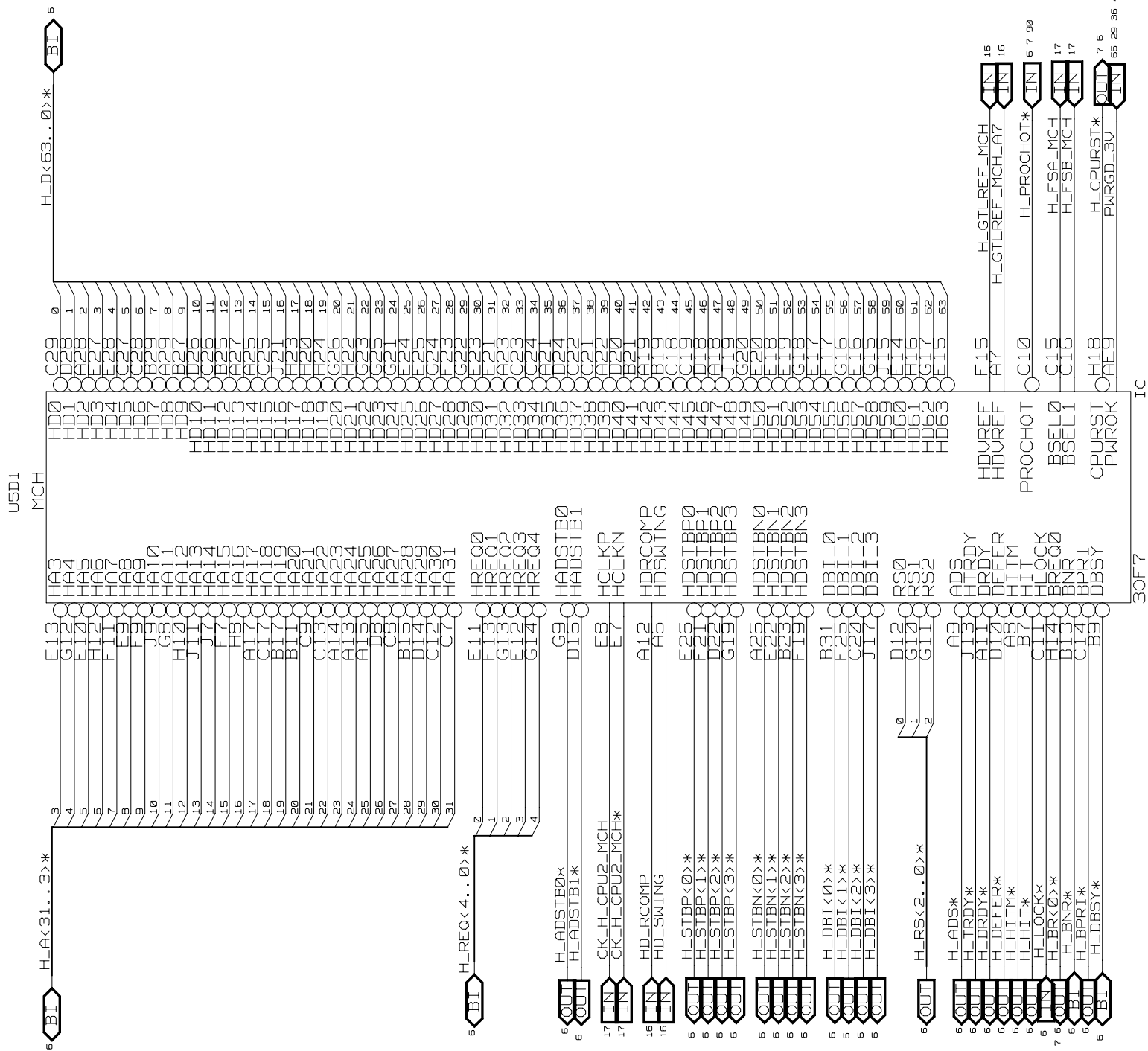
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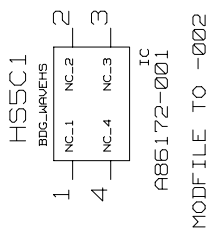
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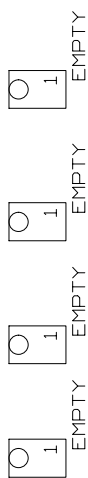


DESIGN NOTE: BOTH WSHS AND ANCHORS DUE TO  
EARLY REQUIREMENTS OF BOTH  
MCH WAVE SOLDER HEATSINK:



MCH RETENTION ANCHOR CLIPS:

ITEM	DESCRIPTION	UNIT	QTY	PRICE	TOTAL
1	ITEM 1	UNIT 1	1	100	100
2	ITEM 2	UNIT 2	2	200	400
3	ITEM 3	UNIT 3	3	300	900
4	ITEM 4	UNIT 4	4	400	1600
5	ITEM 5	UNIT 5	5	500	2500
6	ITEM 6	UNIT 6	6	600	3600
7	ITEM 7	UNIT 7	7	700	4900
8	ITEM 8	UNIT 8	8	800	6400
9	ITEM 9	UNIT 9	9	900	8100
10	ITEM 10	UNIT 10	10	1000	10000
11	ITEM 11	UNIT 11	11	1100	12100
12	ITEM 12	UNIT 12	12	1200	14400
13	ITEM 13	UNIT 13	13	1300	16900
14	ITEM 14	UNIT 14	14	1400	19600
15	ITEM 15	UNIT 15	15	1500	22500
16	ITEM 16	UNIT 16	16	1600	25600
17	ITEM 17	UNIT 17	17	1700	28900
18	ITEM 18	UNIT 18	18	1800	32400
19	ITEM 19	UNIT 19	19	1900	36100
20	ITEM 20	UNIT 20	20	2000	40000
21	ITEM 21	UNIT 21	21	2100	44100
22	ITEM 22	UNIT 22	22	2200	48400
23	ITEM 23	UNIT 23	23	2300	52900
24	ITEM 24	UNIT 24	24	2400	57600
25	ITEM 25	UNIT 25	25	2500	62500
26	ITEM 26	UNIT 26	26	2600	67600
27	ITEM 27	UNIT 27	27	2700	72900
28	ITEM 28	UNIT 28	28	2800	78400
29	ITEM 29	UNIT 29	29	2900	84100
30	ITEM 30	UNIT 30	30	3000	90000
31	ITEM 31	UNIT 31	31	3100	96100
32	ITEM 32	UNIT 32	32	3200	102400
33	ITEM 33	UNIT 33	33	3300	108900
34	ITEM 34	UNIT 34	34	3400	115600
35	ITEM 35	UNIT 35	35	3500	122500
36	ITEM 36	UNIT 36	36	3600	129600
37	ITEM 37	UNIT 37	37	3700	136900
38	ITEM 38	UNIT 38	38	3800	144400
39	ITEM 39	UNIT 39	39	3900	152100
40	ITEM 40	UNIT 40	40	4000	160000
41	ITEM 41	UNIT 41	41	4100	168100
42	ITEM 42	UNIT 42	42	4200	176400
43	ITEM 43	UNIT 43	43	4300	184900
44	ITEM 44	UNIT 44	44	4400	193600
45	ITEM 45	UNIT 45	45	4500	202500
46	ITEM 46	UNIT 46	46	4600	211600
47	ITEM 47	UNIT 47	47	4700	220900
48	ITEM 48	UNIT 48	48	4800	230400
49	ITEM 49	UNIT 49	49	4900	240100
50	ITEM 50	UNIT 50	50	5000	250000
51	ITEM 51	UNIT 51	51	5100	260100
52	ITEM 52	UNIT 52	52	5200	270400
53	ITEM 53	UNIT 53	53	5300	280900
54	ITEM 54	UNIT 54	54	5400	291600
55	ITEM 55	UNIT 55	55	5500	302500
56	ITEM 56	UNIT 56	56	5600	313600
57	ITEM 57	UNIT 57	57	5700	324900
58	ITEM 58	UNIT 58	58	5800	336400
59	ITEM 59	UNIT 59	59	5900	348100
60	ITEM 60	UNIT 60	60	6000	360000
61	ITEM 61	UNIT 61	61	6100	372100
62	ITEM 62	UNIT 62	62	6200	384400
63	ITEM 63	UNIT 63	63	6300	396900
64	ITEM 64				

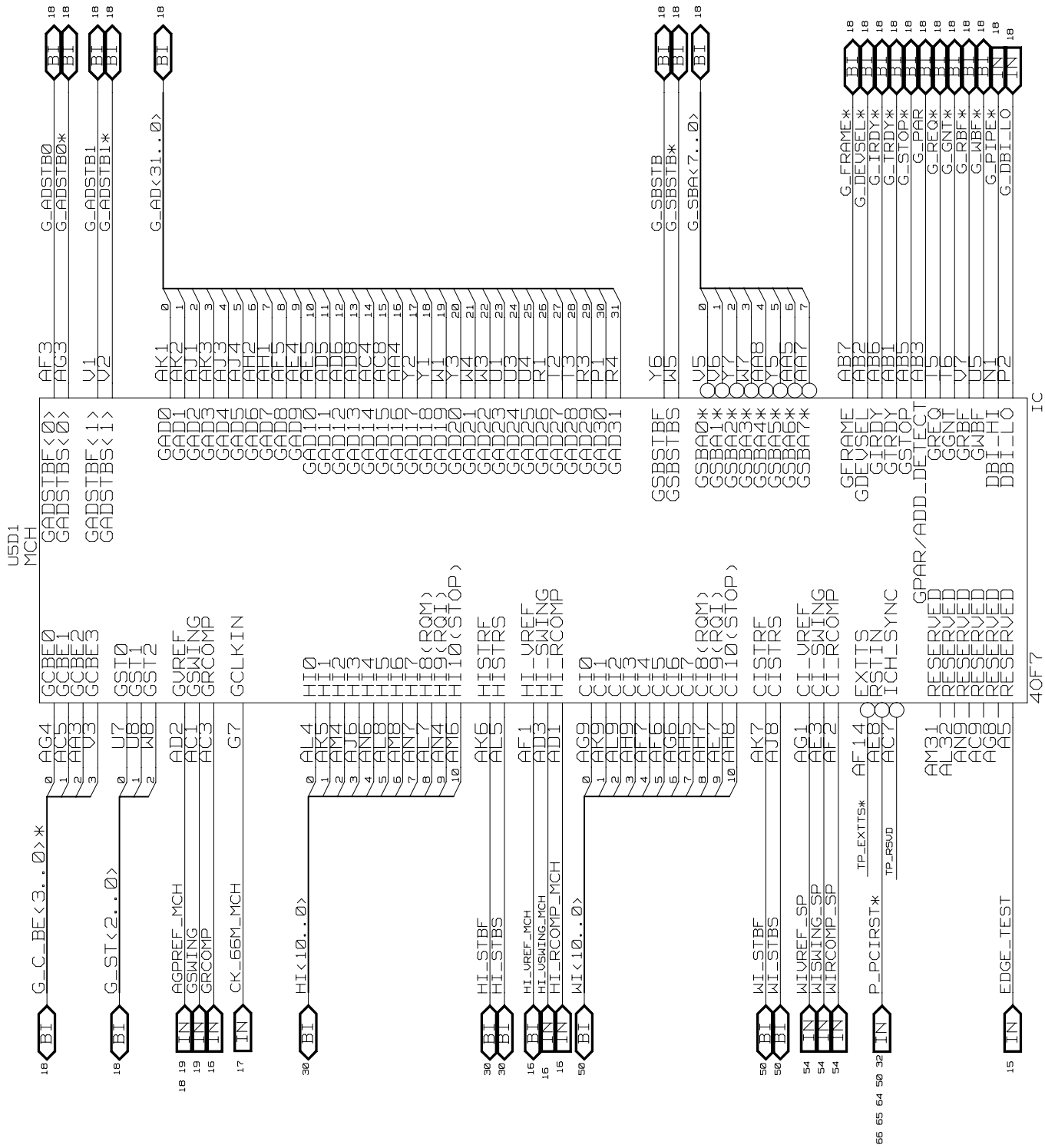


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MCH:CHIPSET 4 OF 6

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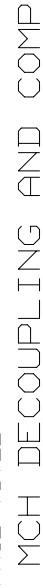
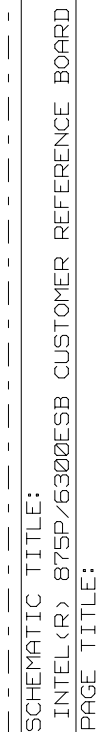
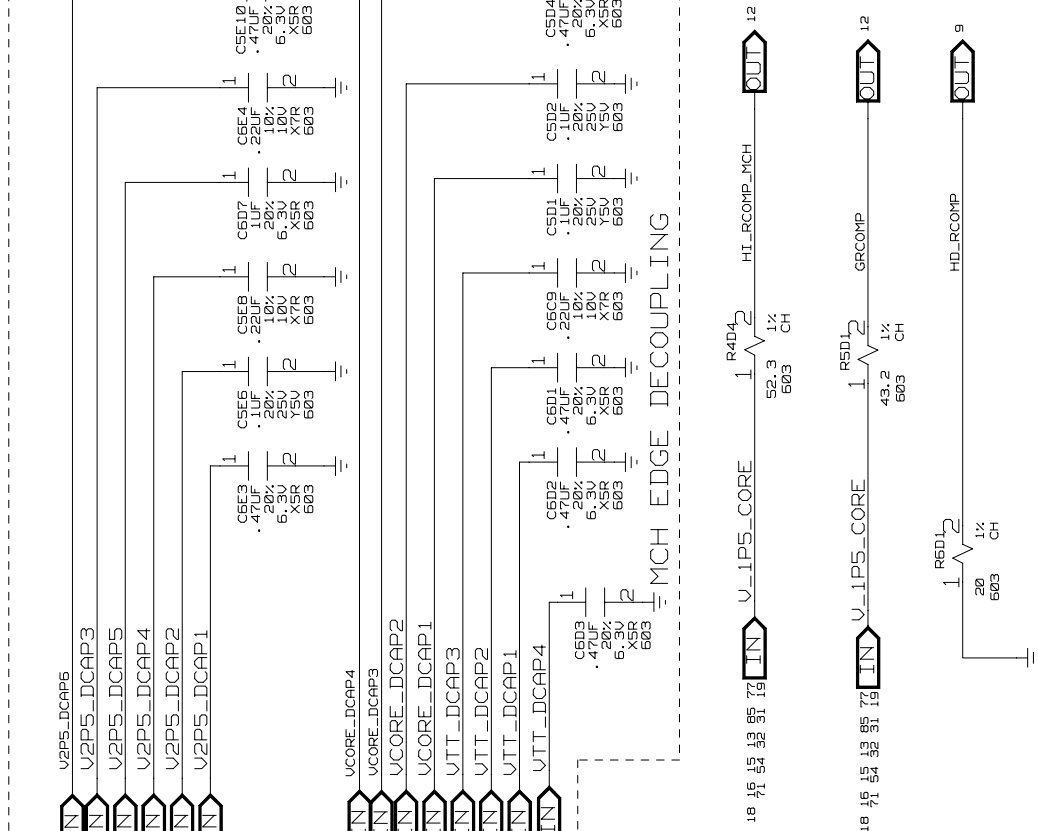
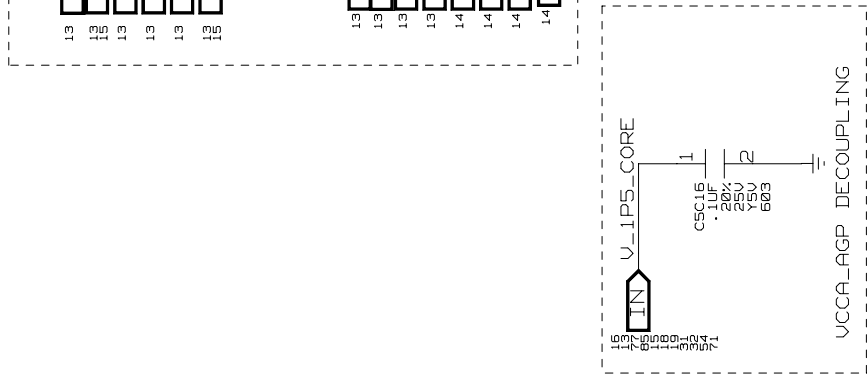
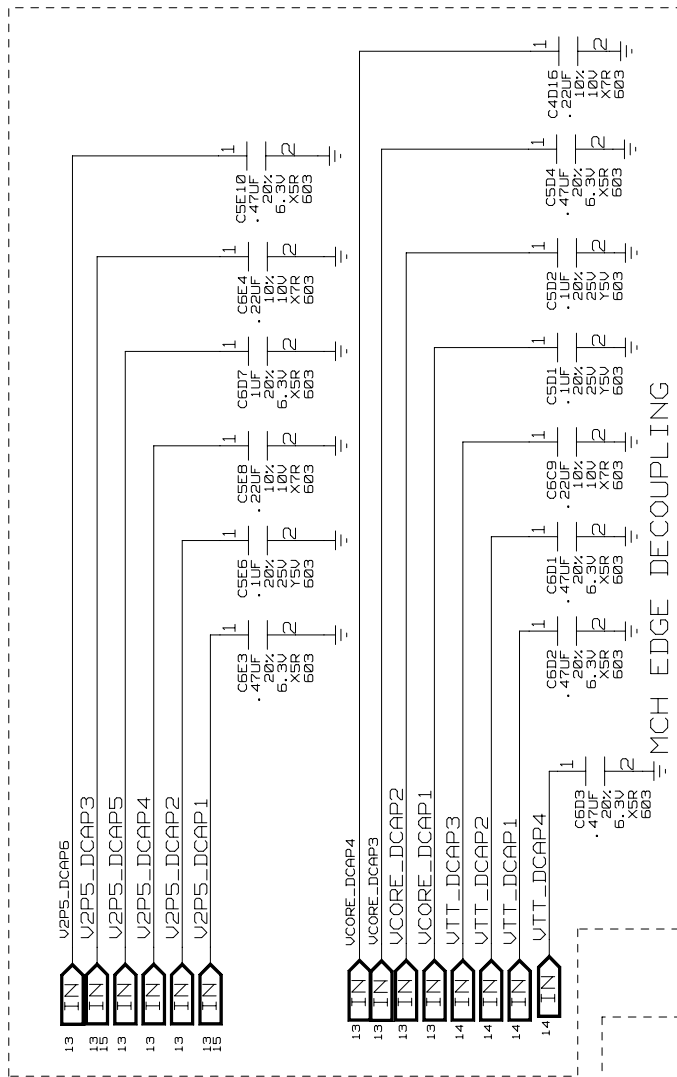
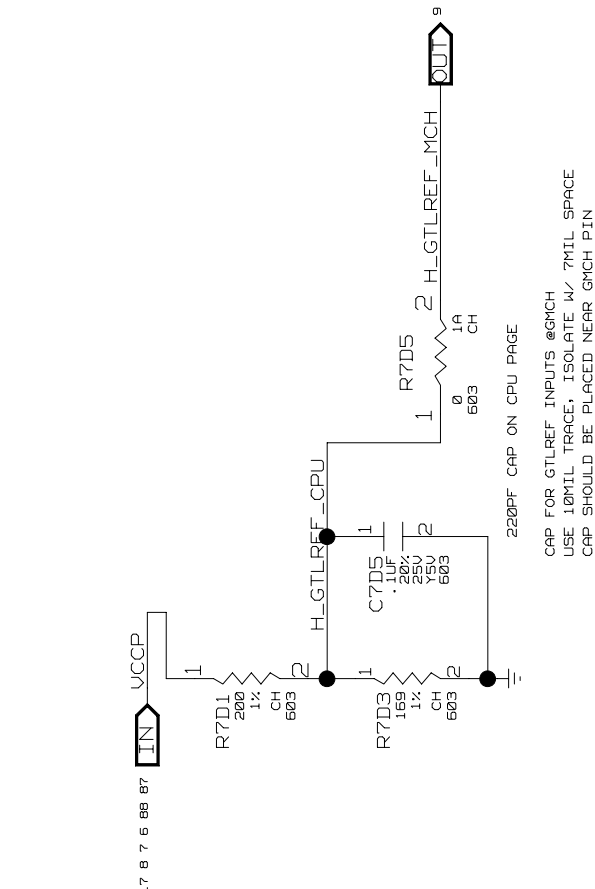
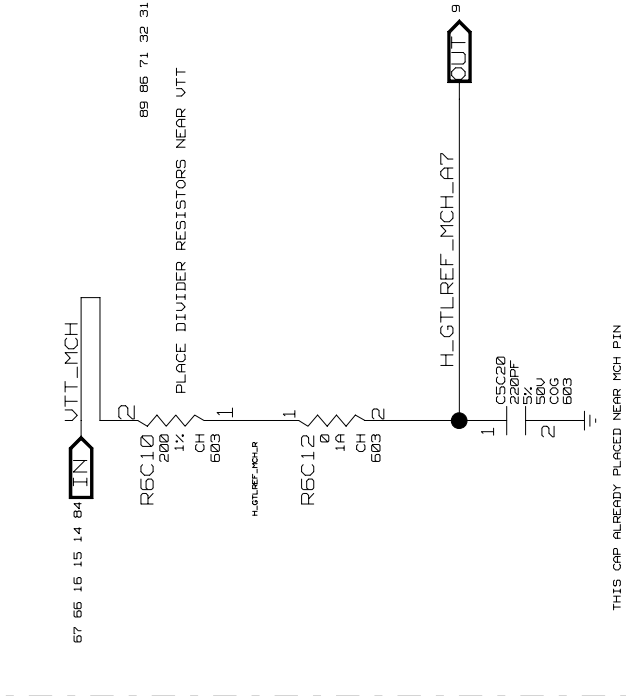
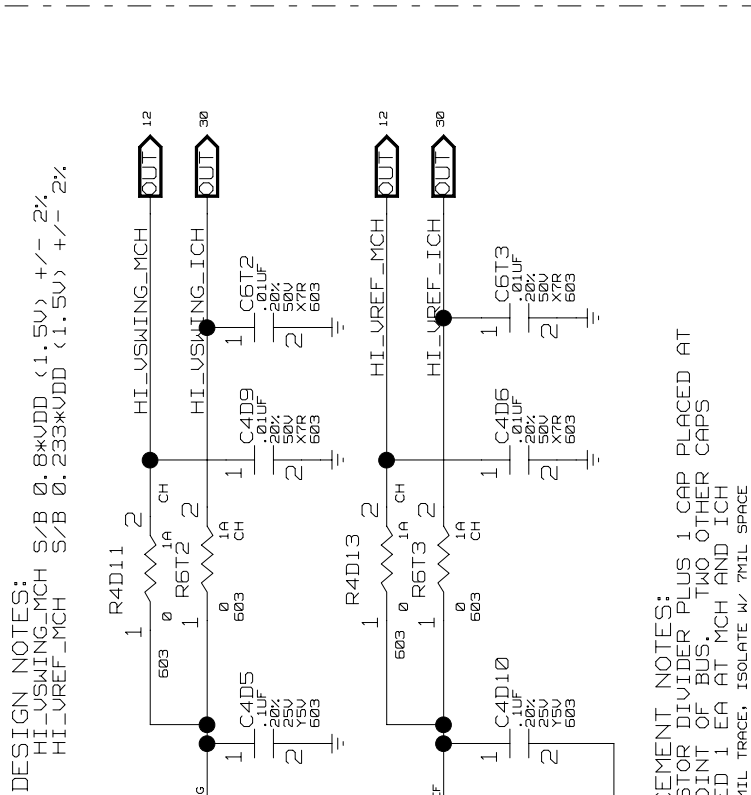
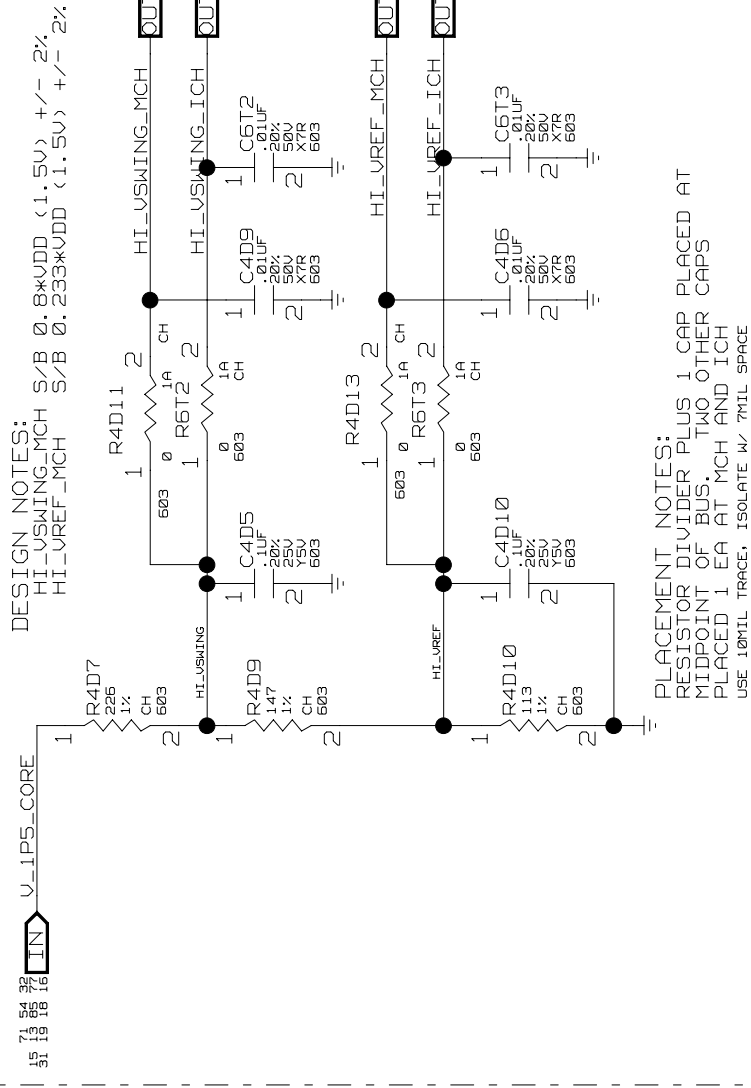
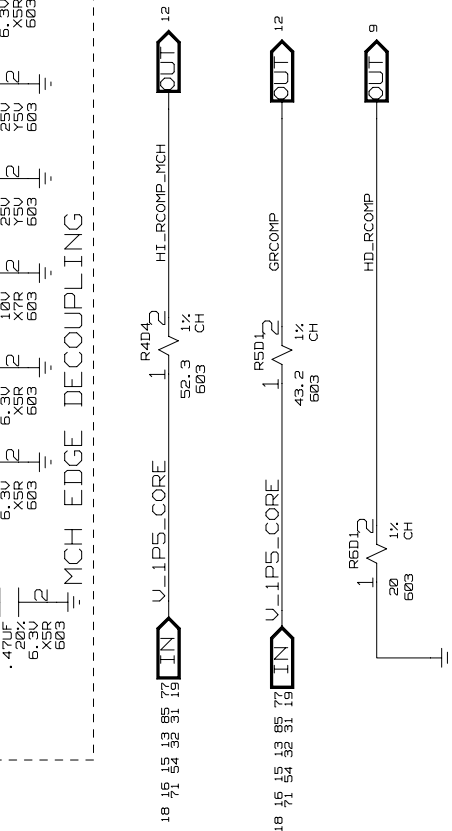
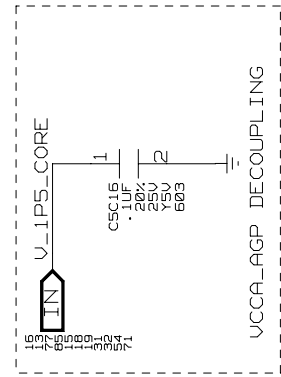
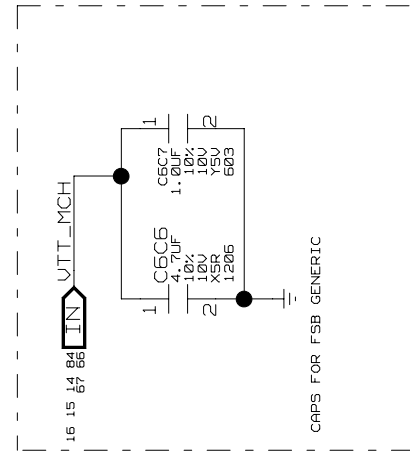
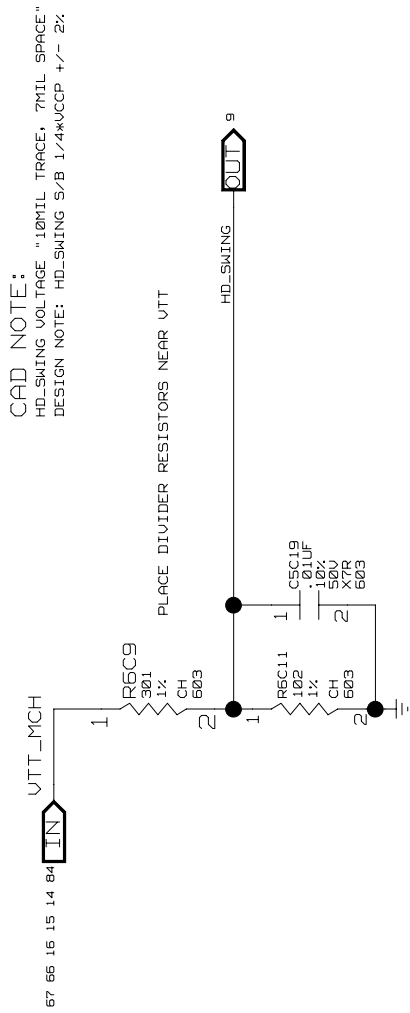
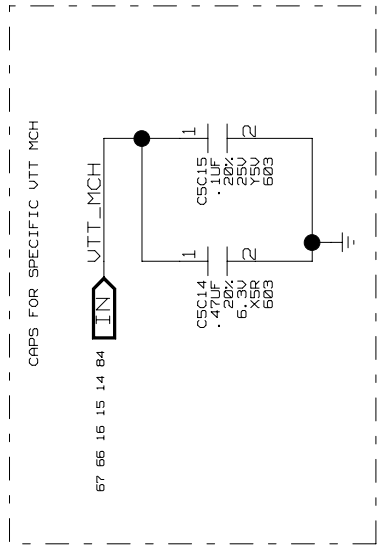
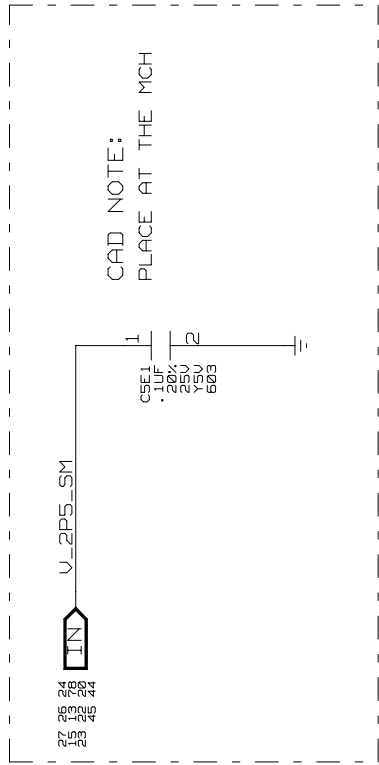
DRAWING

DRAWING



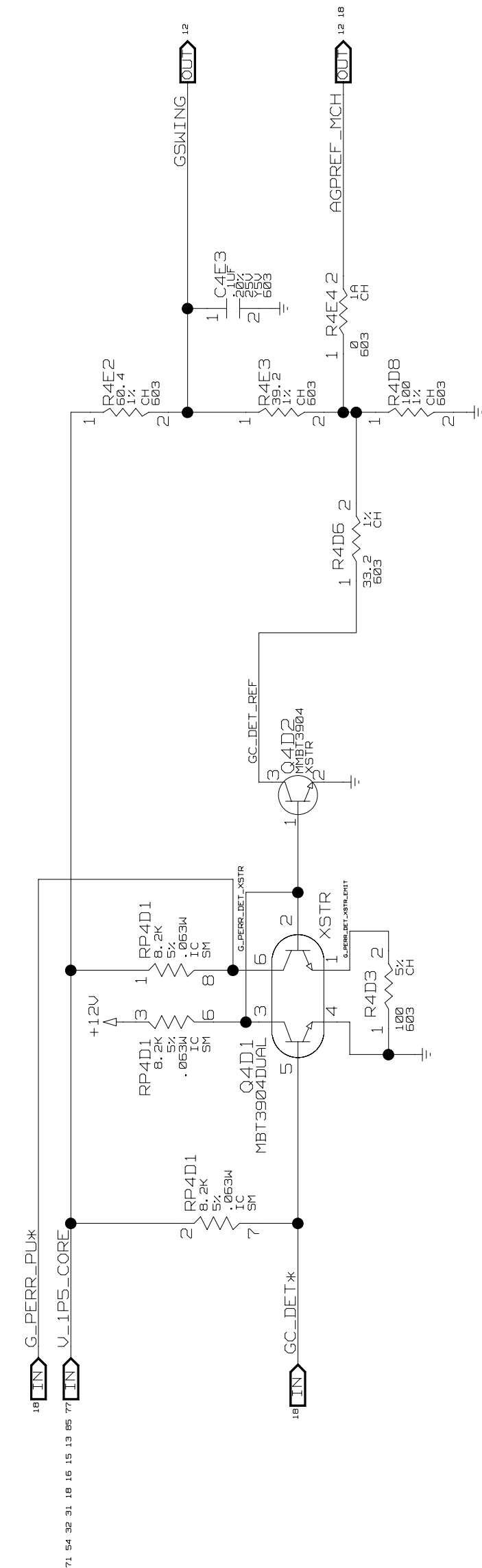
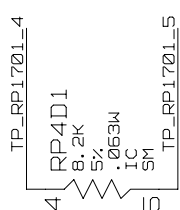
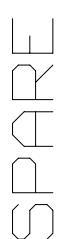












SCHEMATIC TITLE:

INTEL(R) 875P/5300ESB CUSTOMER REFERENCE BOARD

PAGE TITLE:

# ACP SWING AND VREF

REV:  
1.3

INTEL	LAST REVISED:	SHEET:
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1900 PRAIRIE CITY ROAD  
FOLSOM, CALIFORNIA 95630

FOLSOM, CALIFORNIA 95630

LAST REVISED:

2024 2024

SHEET:

19/90

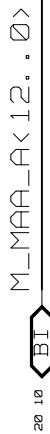
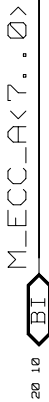
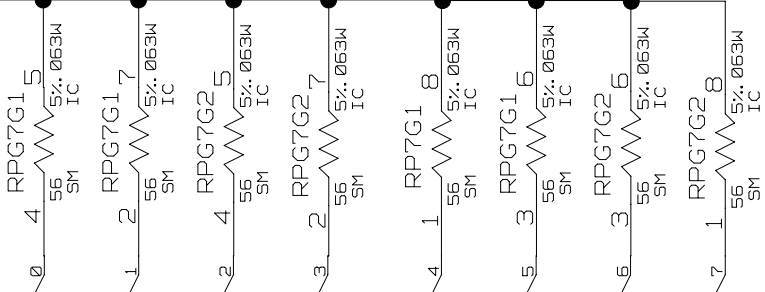
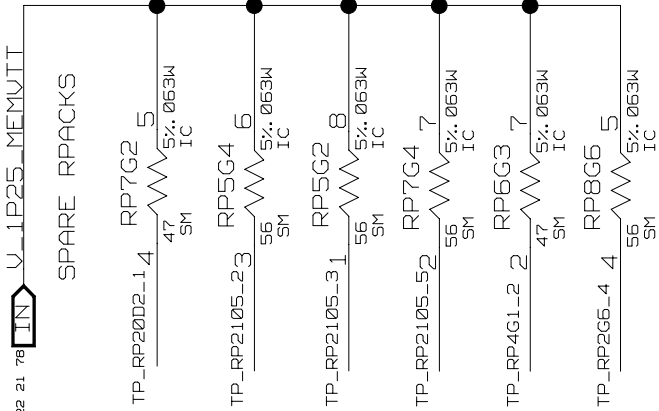
## DRAWING

Wed Feb 11 18:12:16 2004

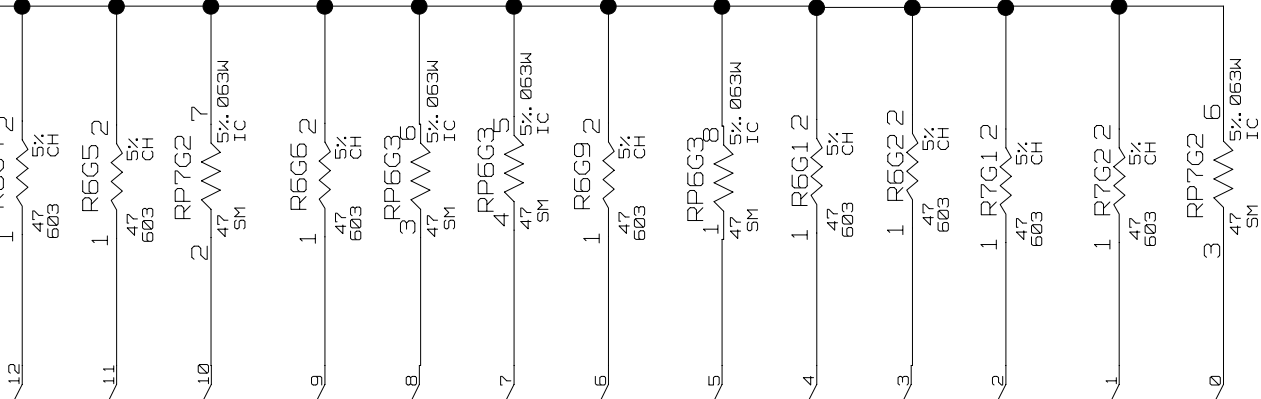
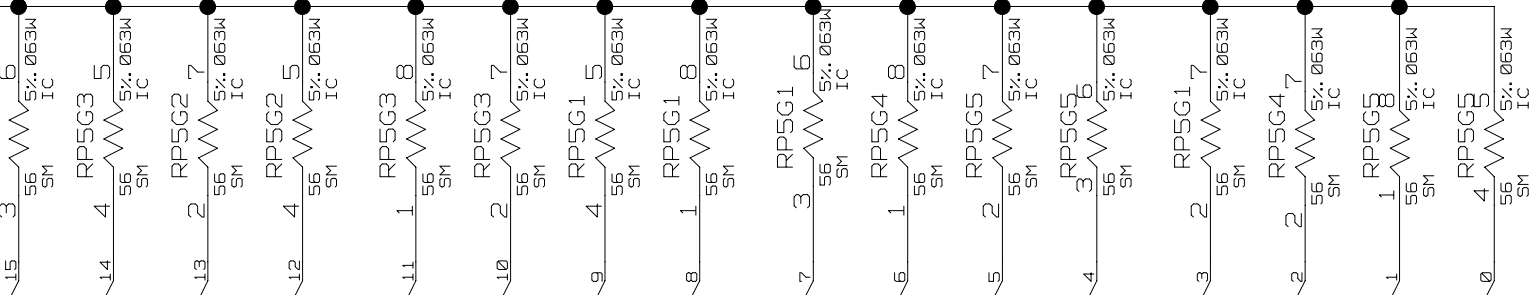
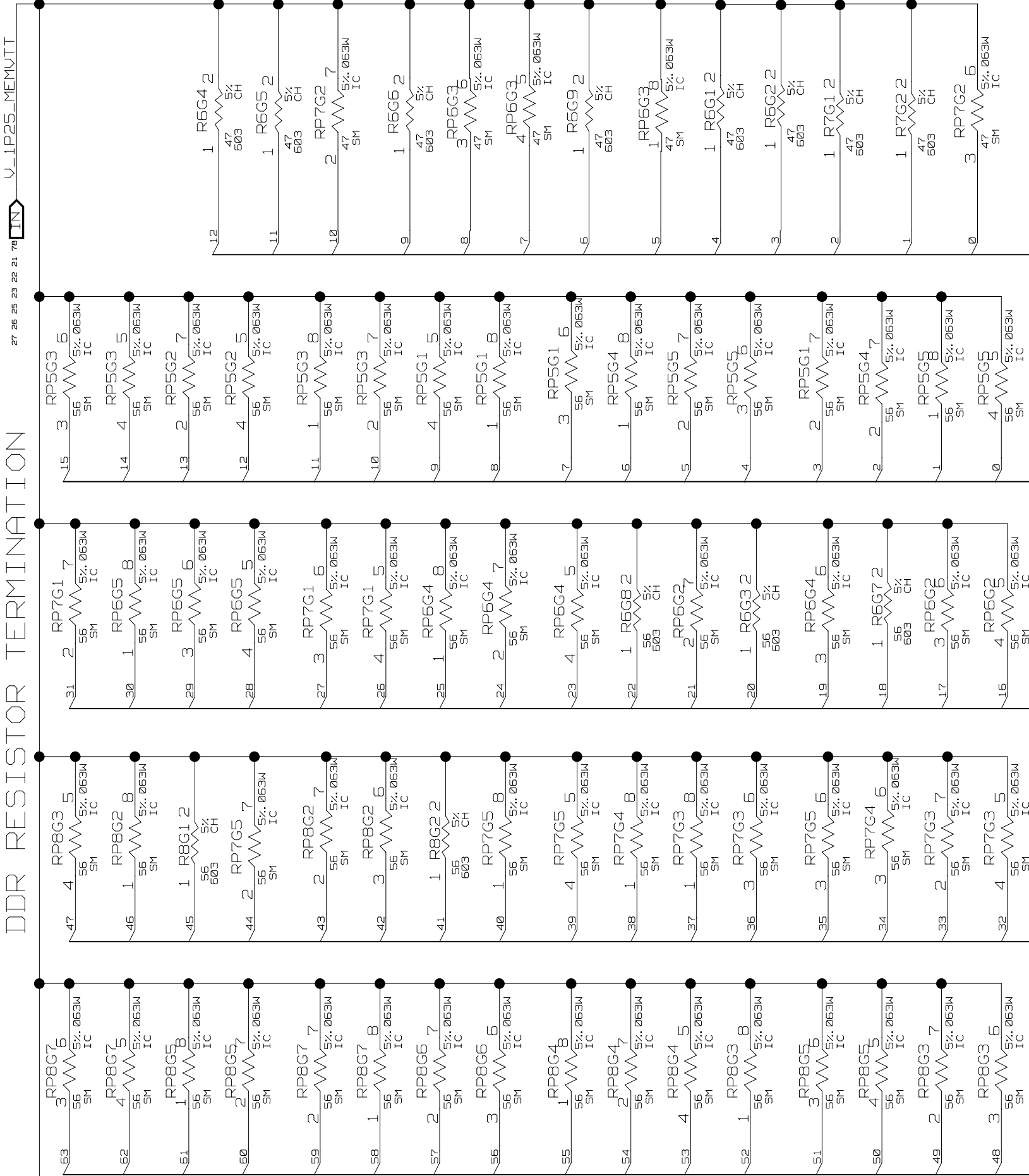




## SPARE SECTIONS

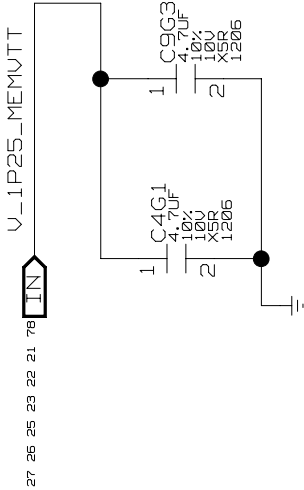


# DDR RESISTOR TERMINATION



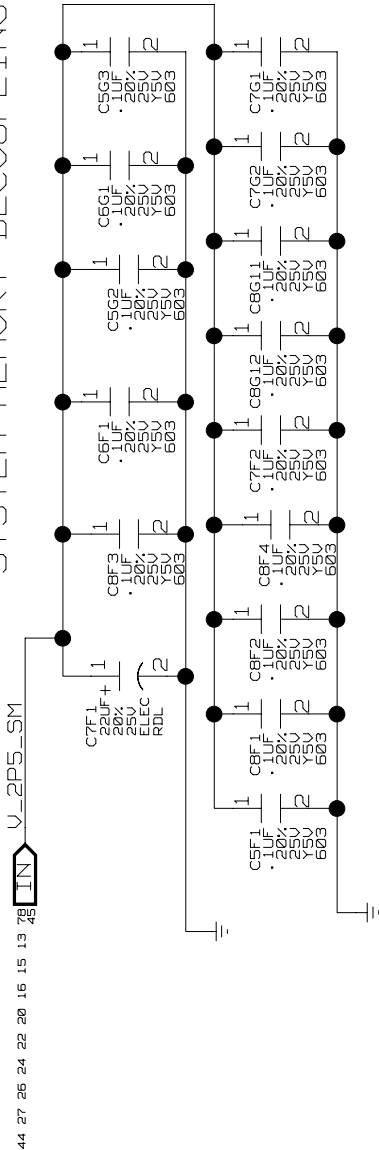


DDR CHANNEL A

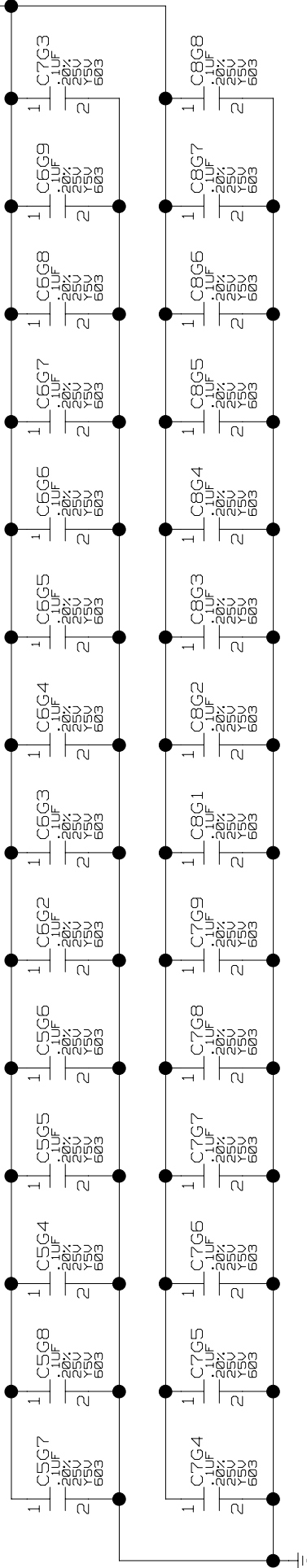


PLACED AT LEFT AND RIGHT ENDS  
OF VTT ISLAND

SYSTEM MEMORY DECOUPLING



V\_1P25\_MEMUTT

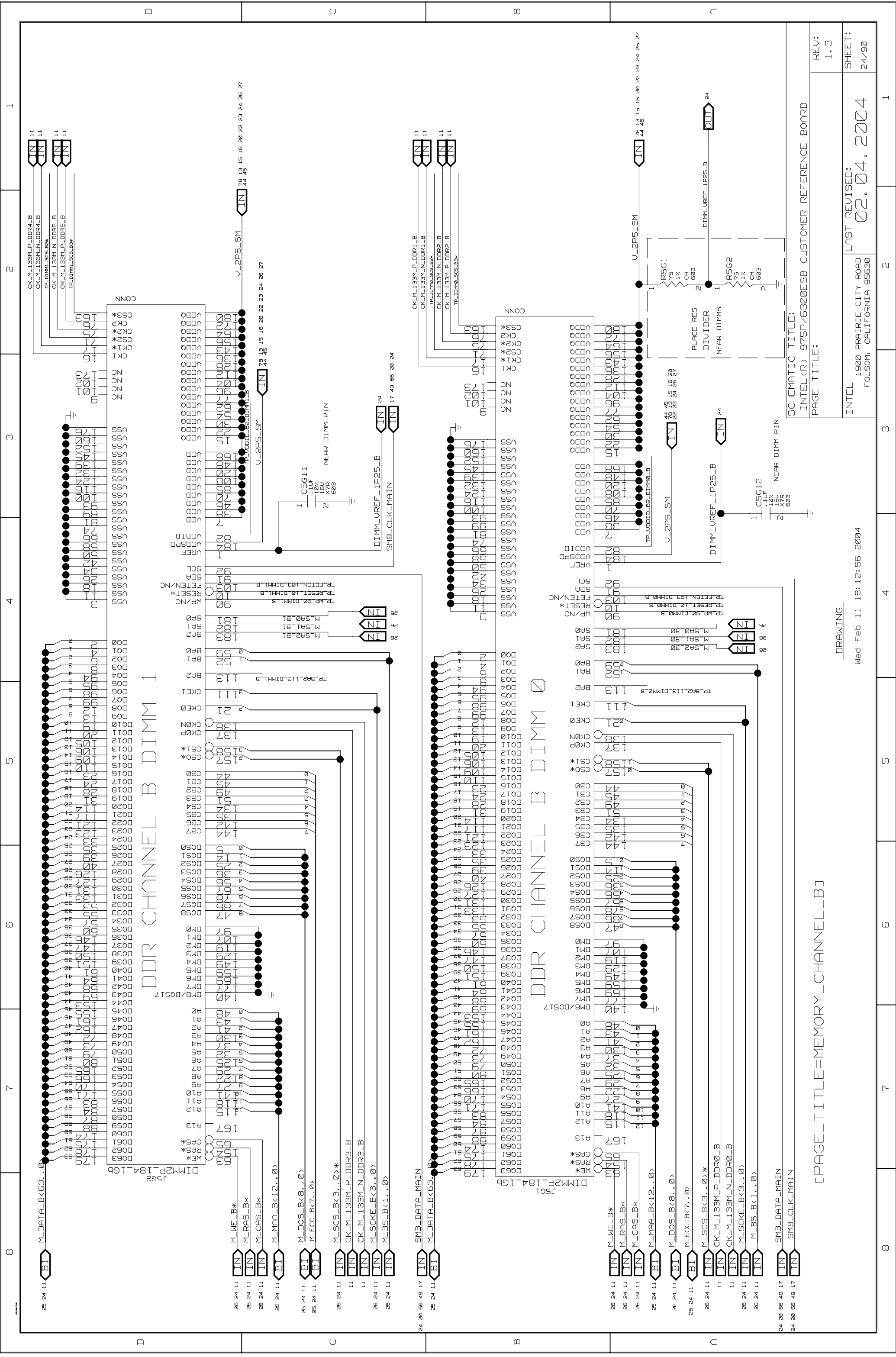


DECOUPLING CAPACITORS FOR DDR TERMINATION RESISTORS

SCHEMATIC TITLE:		INTEL(R) 875P/5300ESB CUSTOMER REFERENCE BOARD		REV:	
PAGE TITLE:		DDR CHAN A VTERM DECOUPLING		1.3	
INTEL		LAST REVISED:		SHEET:	
1900 PRAIRIE CITY ROAD		02.04.2004		23/90	
FOLSOM, CALIFORNIA 95630					

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Wed Feb 11 18:12:48 2004



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Wed Feb 11 18:12:56 2004

[PAGE\_TITLE=MEMORY\_CHANNEL\_B]

SCHEMATIC TITLE:  
INTEL(R) 875P/6300ESB CUSTOMER REFERENCE BOARD  
PAGE TITLE:

REV:  
1.3

LAST REVISED:  
02.04.2004

INTEL  
1900 PRAIRIE CITY ROAD  
FOLSOM, CALIFORNIA 95630

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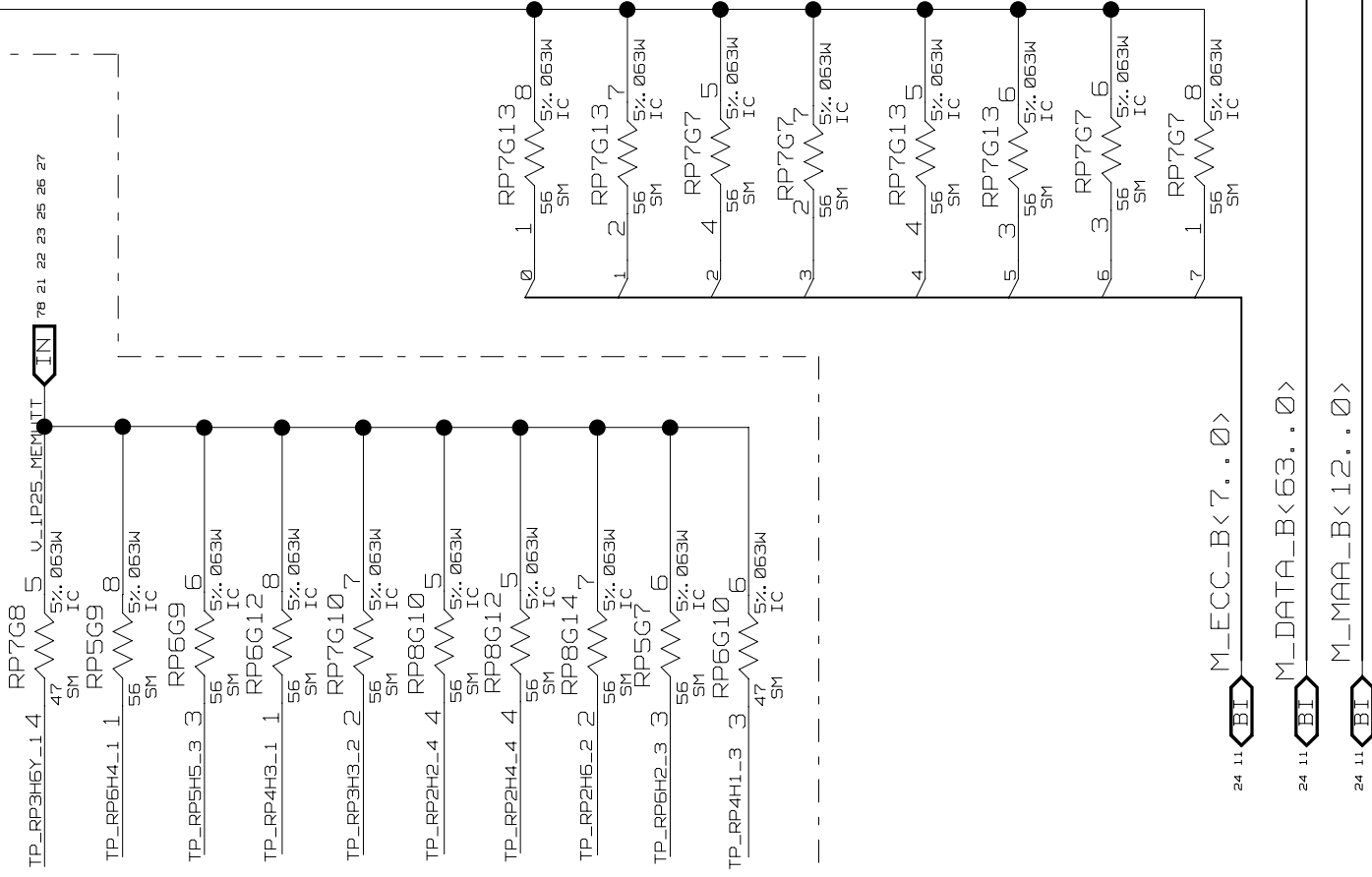
4

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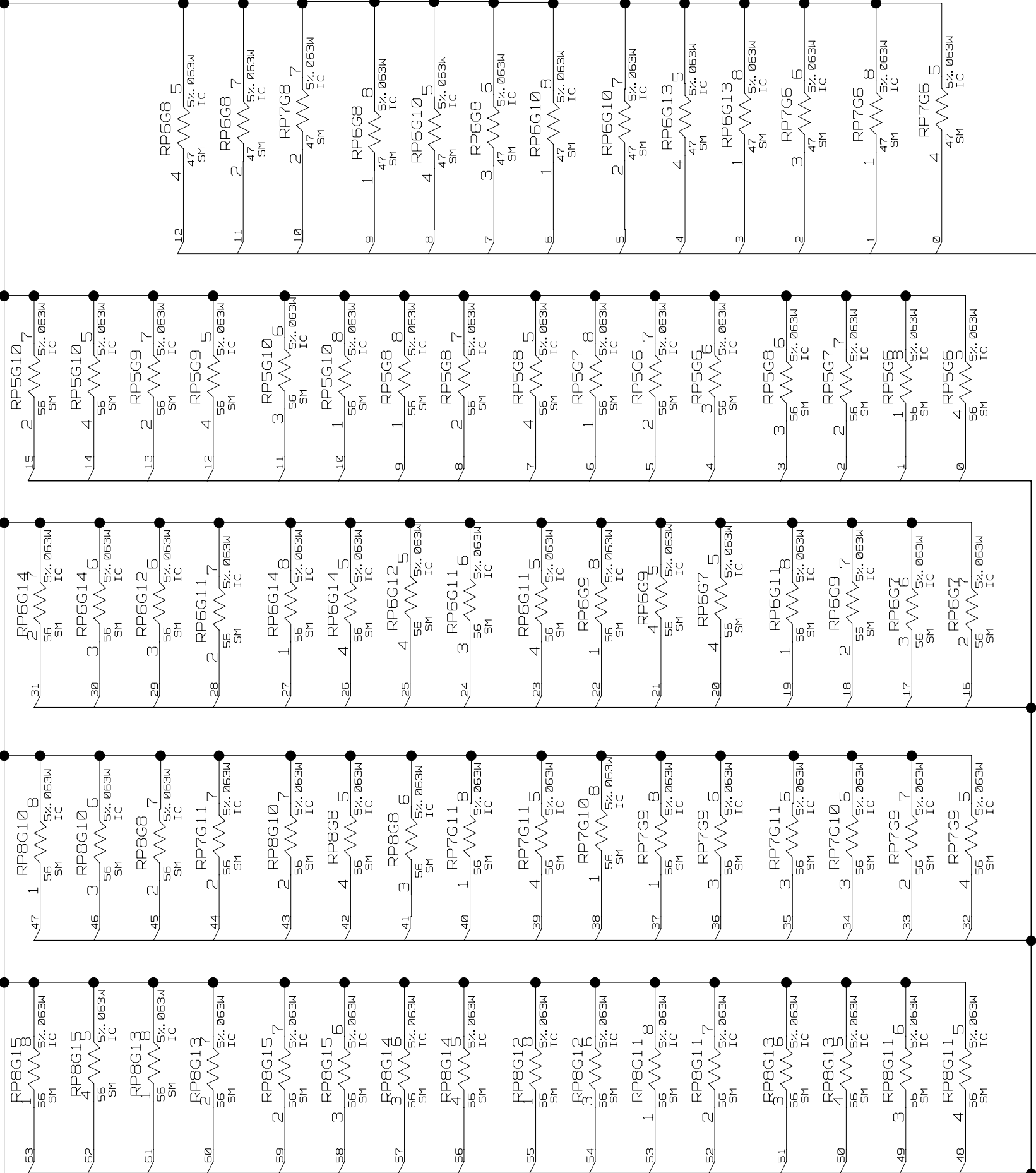
2

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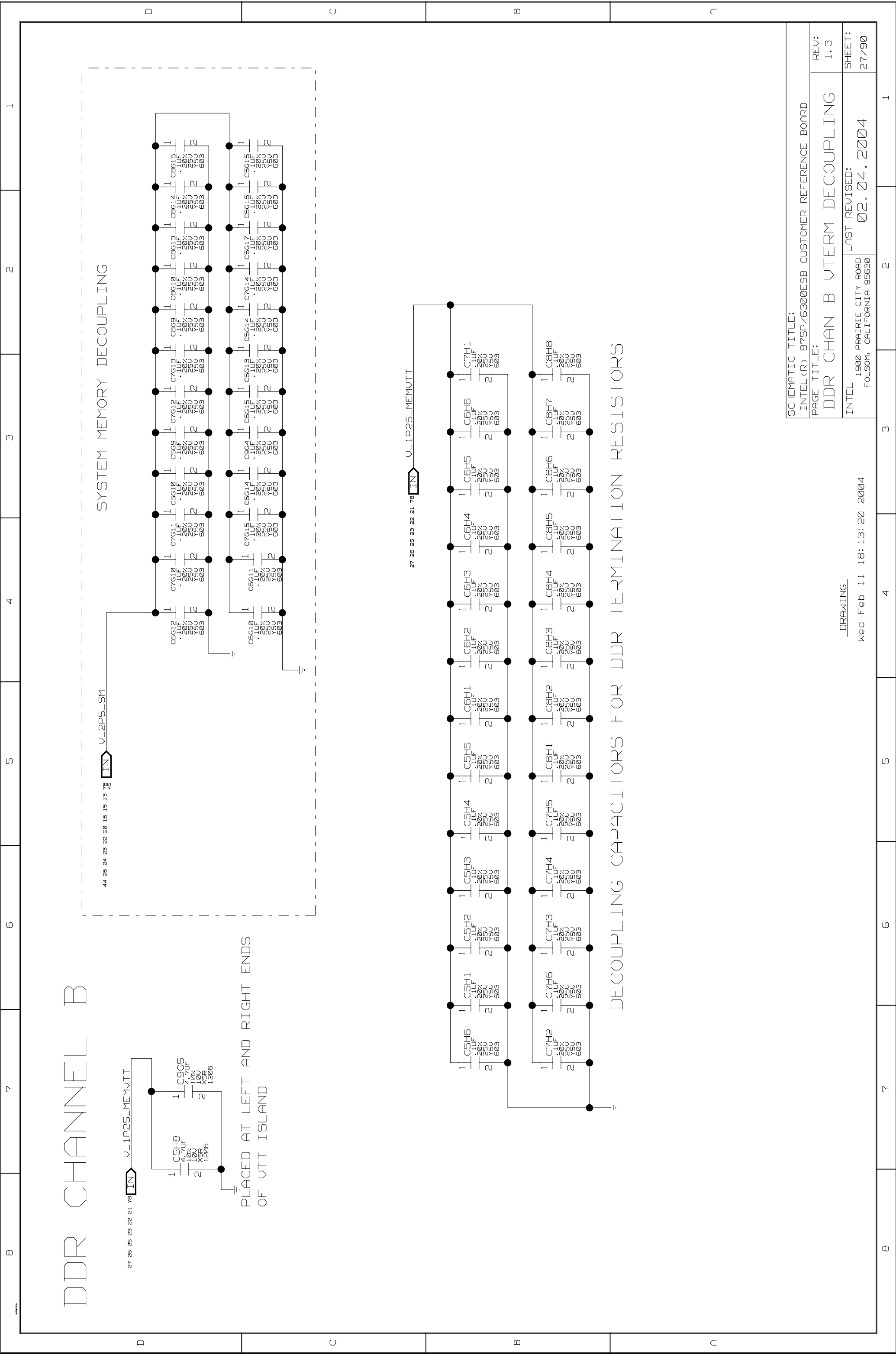
## SPARE SECTIONS



# DDR RESISTOR TERMINATION







DECOUPLING CAPACITORS FOR DDR TERMINATION RESISTORS

8

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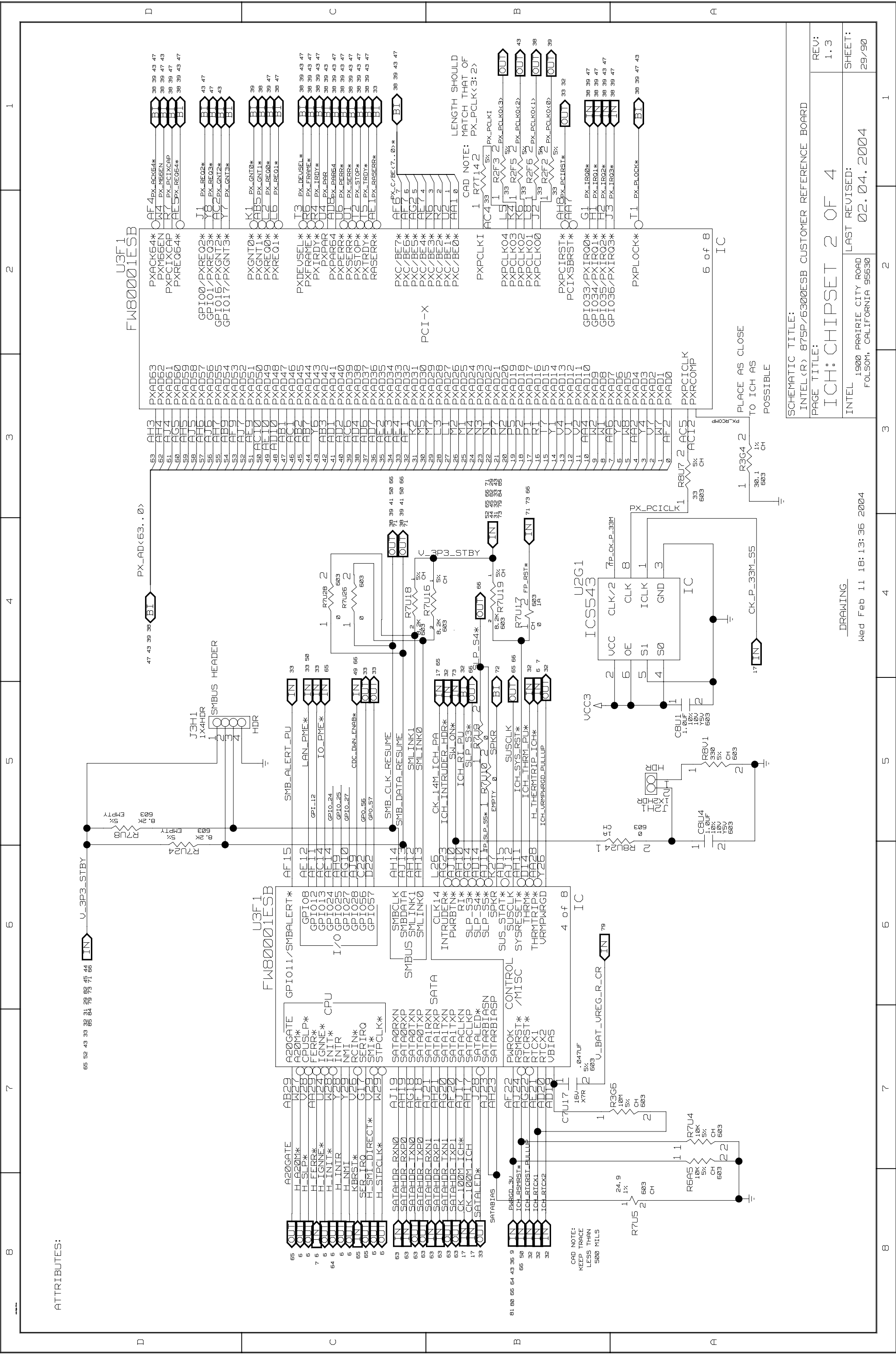
2

1

SCHEMATIC TITLE:  
INTEL(R) 875P/6300ESB CUSTOMER REFERENCE BOARD  
PAGE TITLE:  
DDR CHAN B VTERM DECOUPLING  
REV:  
1.3  
LAST REVISED:  
02.04.2004  
SHEET:  
27/90







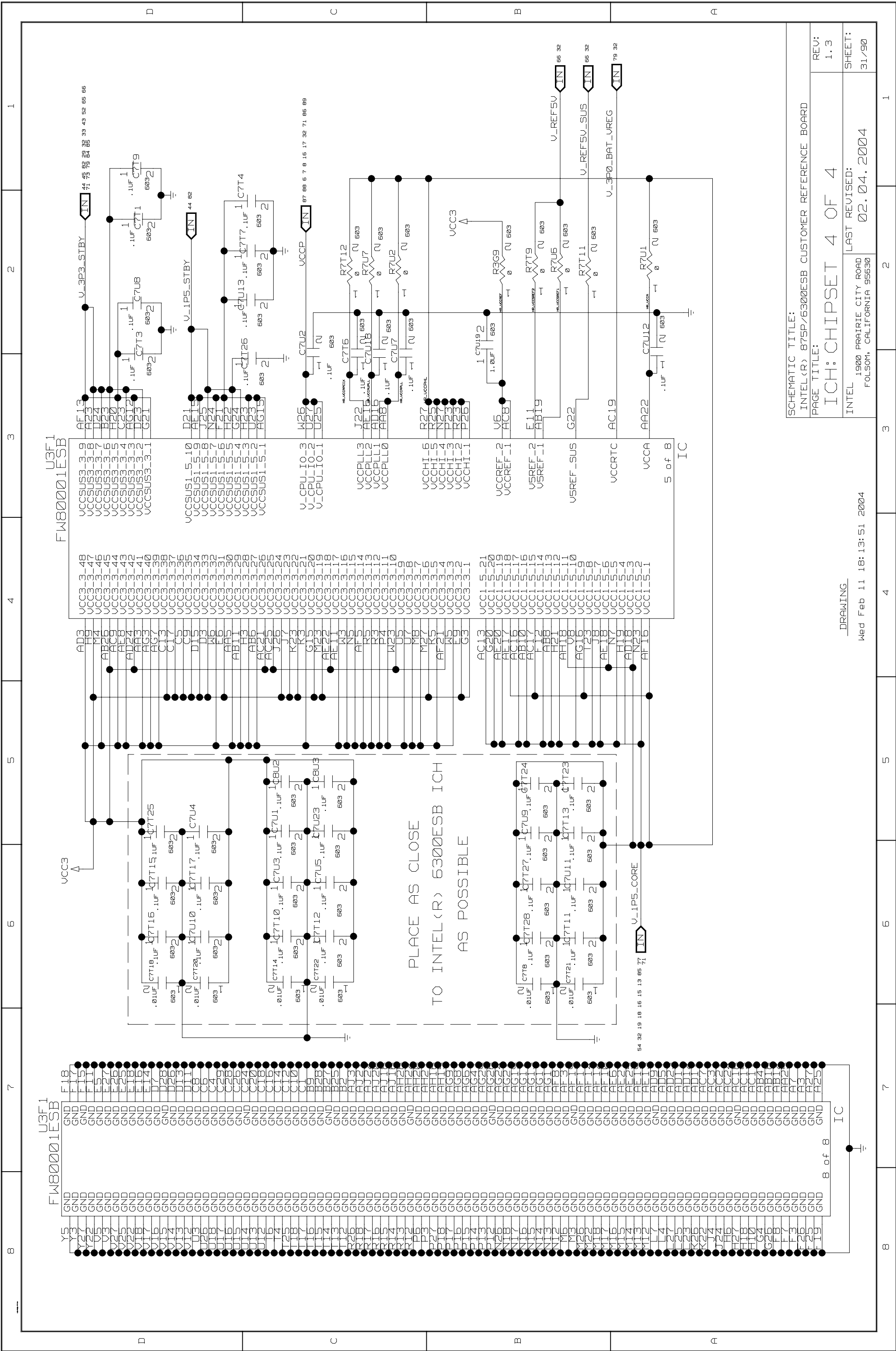
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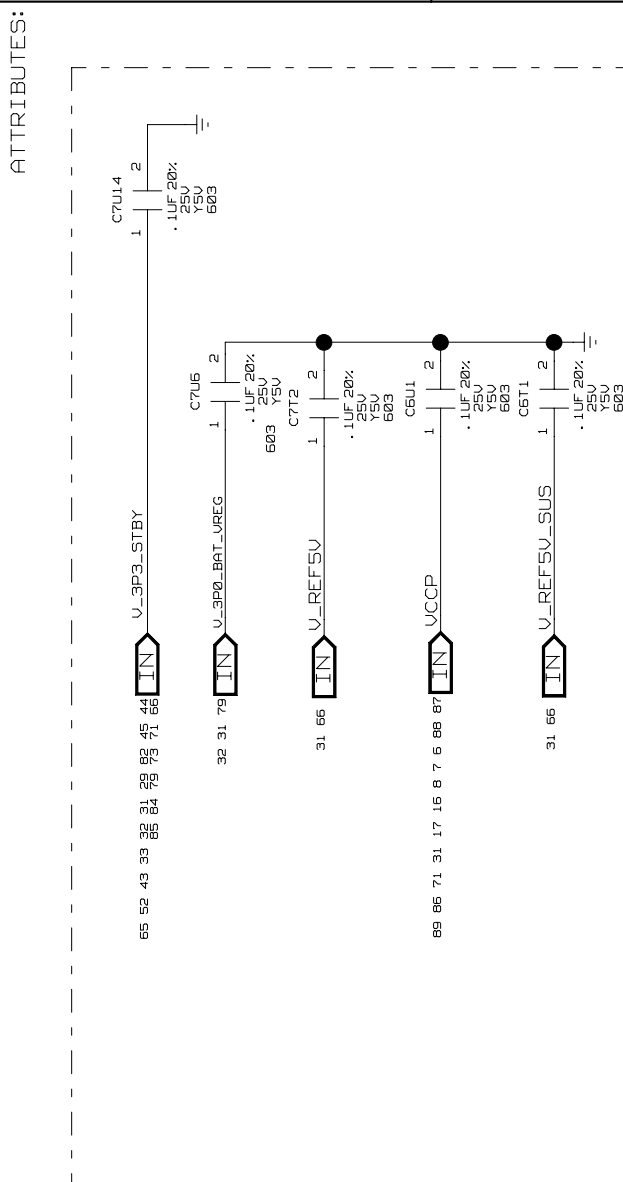
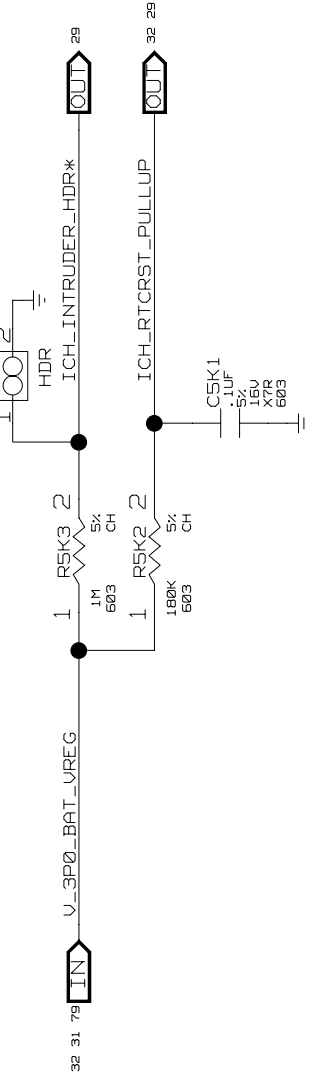
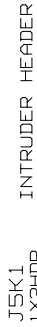
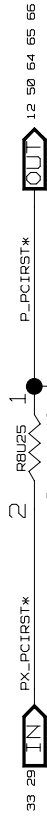
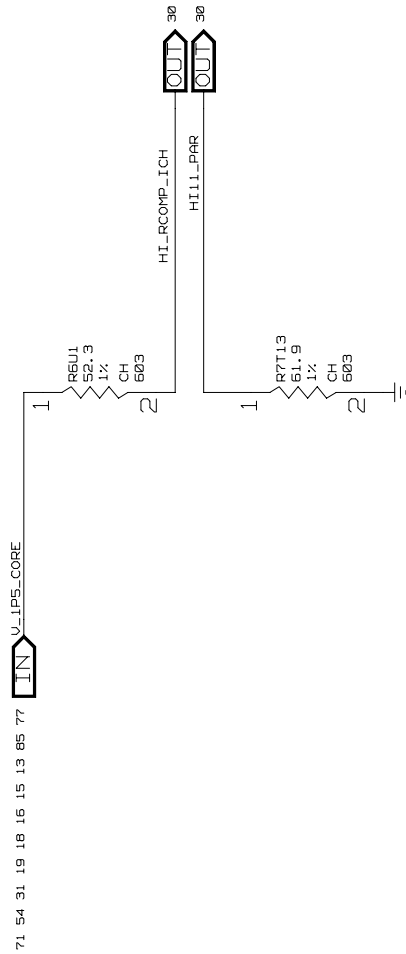
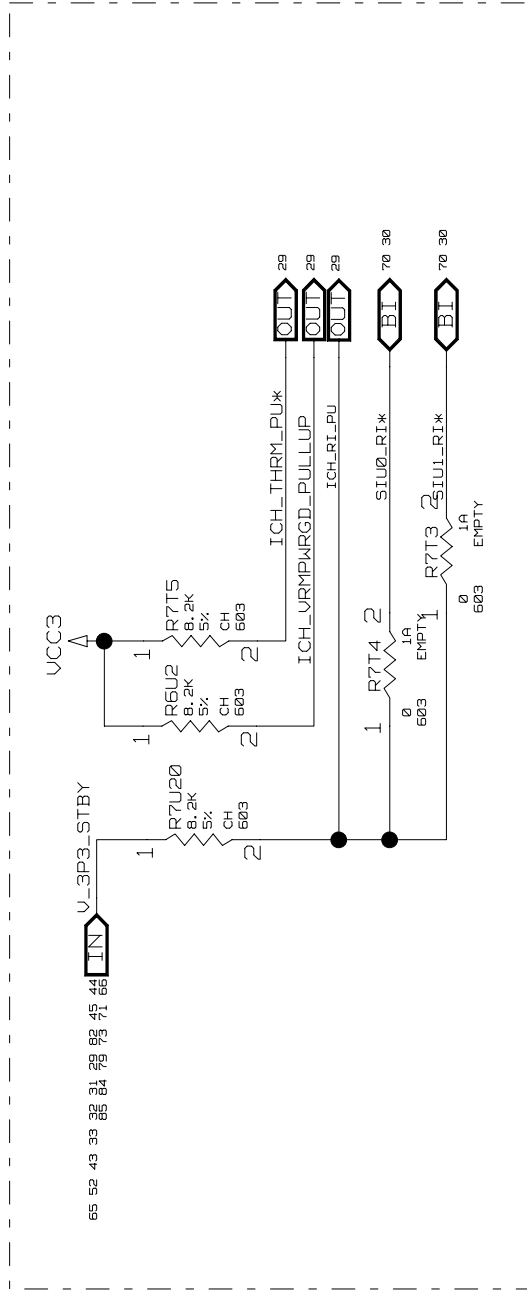
SCHEMATIC TITLE:		INTEL (R) 875P/5300ESB CUSTOMER REFERENCE BOARD		REV:	1.3
PAGE TITLE:		ICH: CHIPSET 2 OF 4			
INTEL		LAST REVISED:		SHEET:	
1900 PRAIRIE CITY ROAD		02.04.2004		29/90	
FOLSOM, CALIFORNIA 95630					

DRAWING

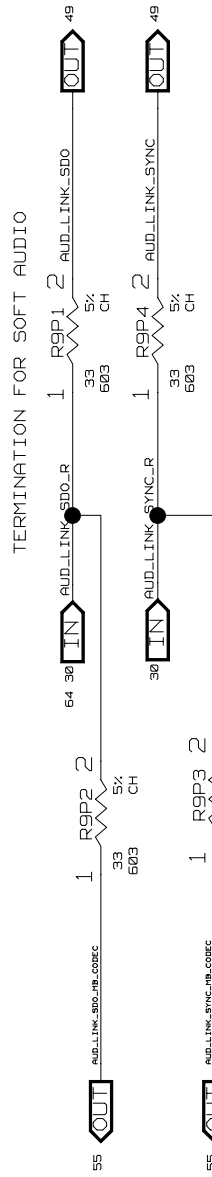
Wed Feb 11 18:13:36 2004



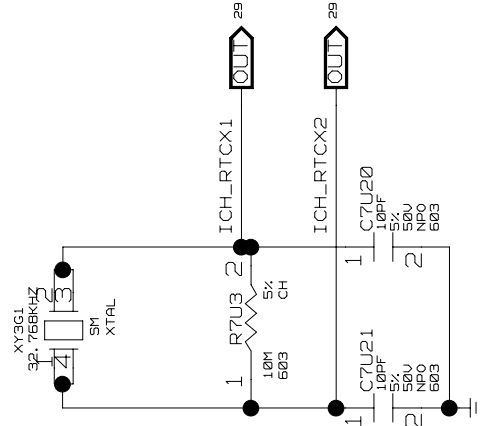
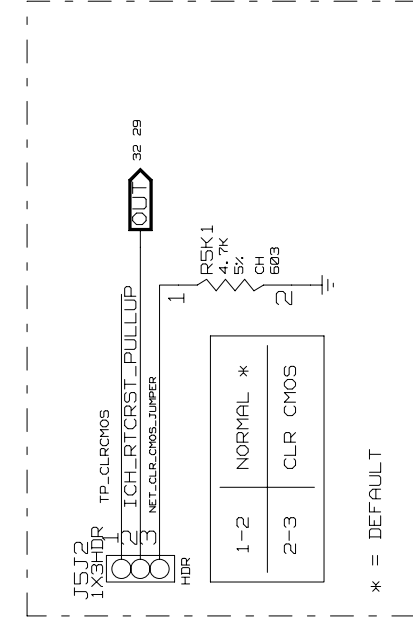




\*NOTE: PLACE ALL WITHIN 40 MILS OF ICH.



CAD NOTE: PLACE CLOSE TO ICH



ATTRIBUTES:

SCHEMATIC TITLE:

INTEL(R) 875P/6300ESB CUSTOMER REFERENCE BOARD

PAGE TITLE:

# ITCH PULLUPS & DECOUPLING

INTEL

1000

LAST REVISED:

32/90

32/90

DRAWING

Wed Feb 11 18:13:59 2004

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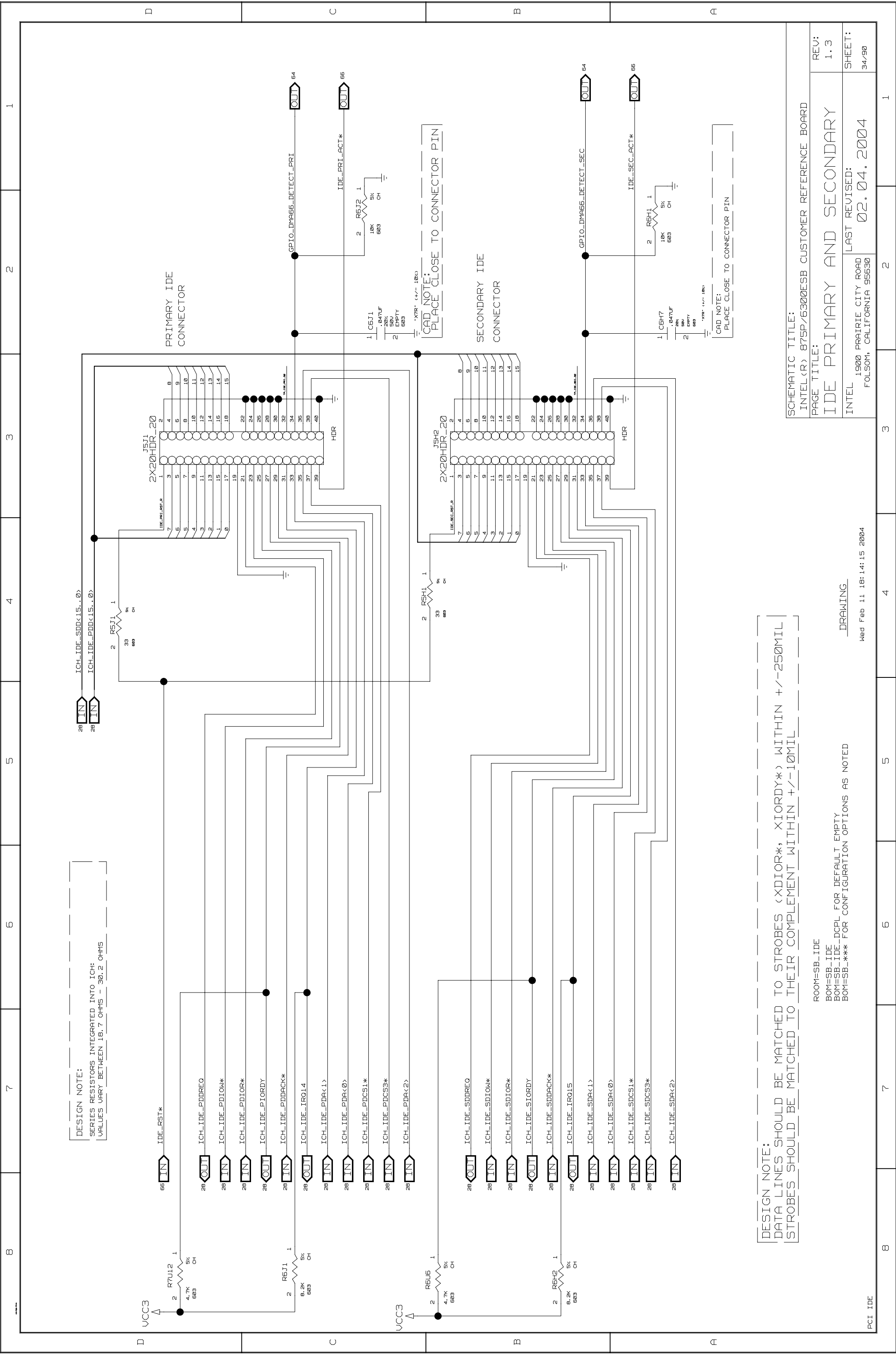
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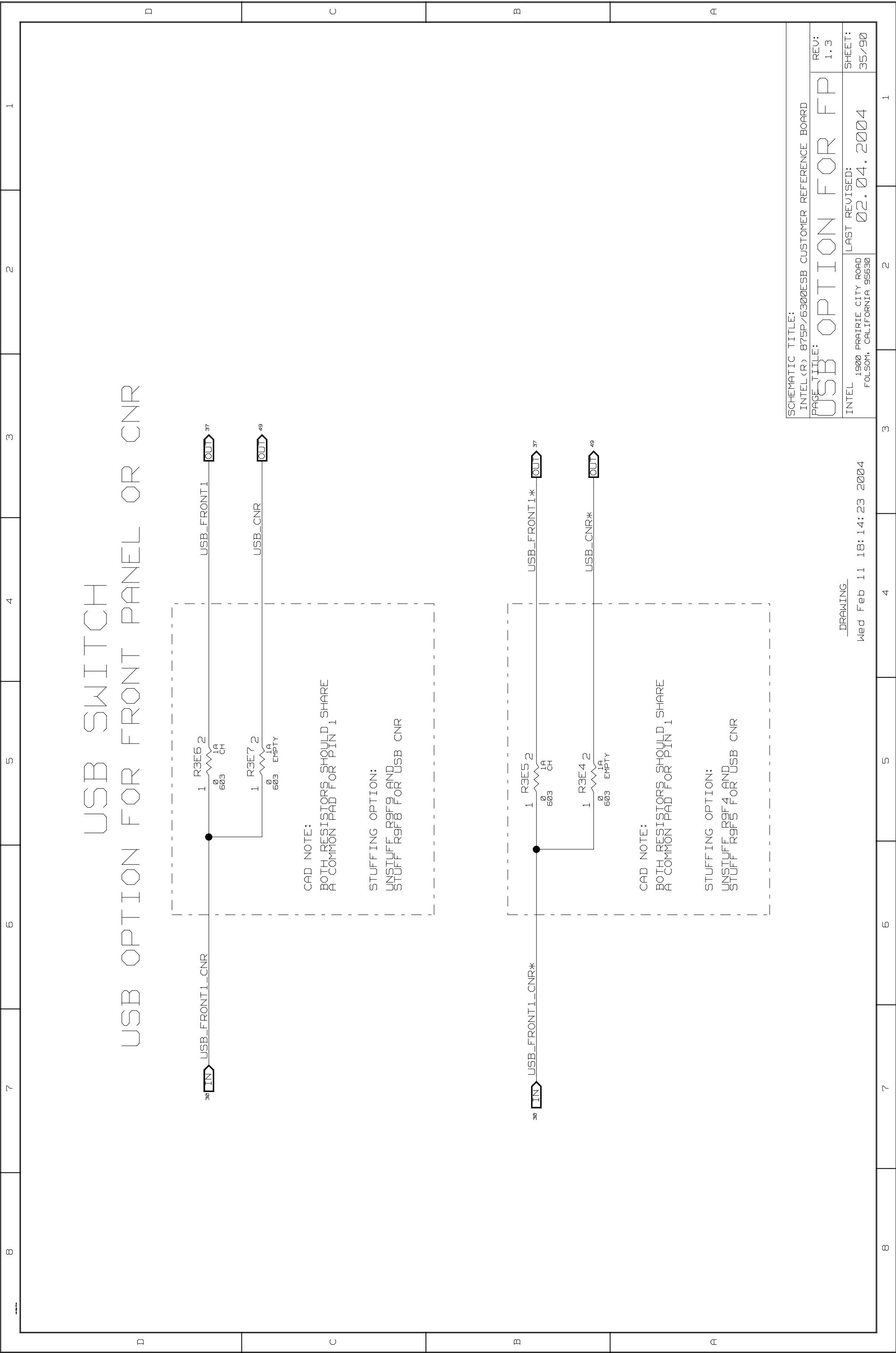
3

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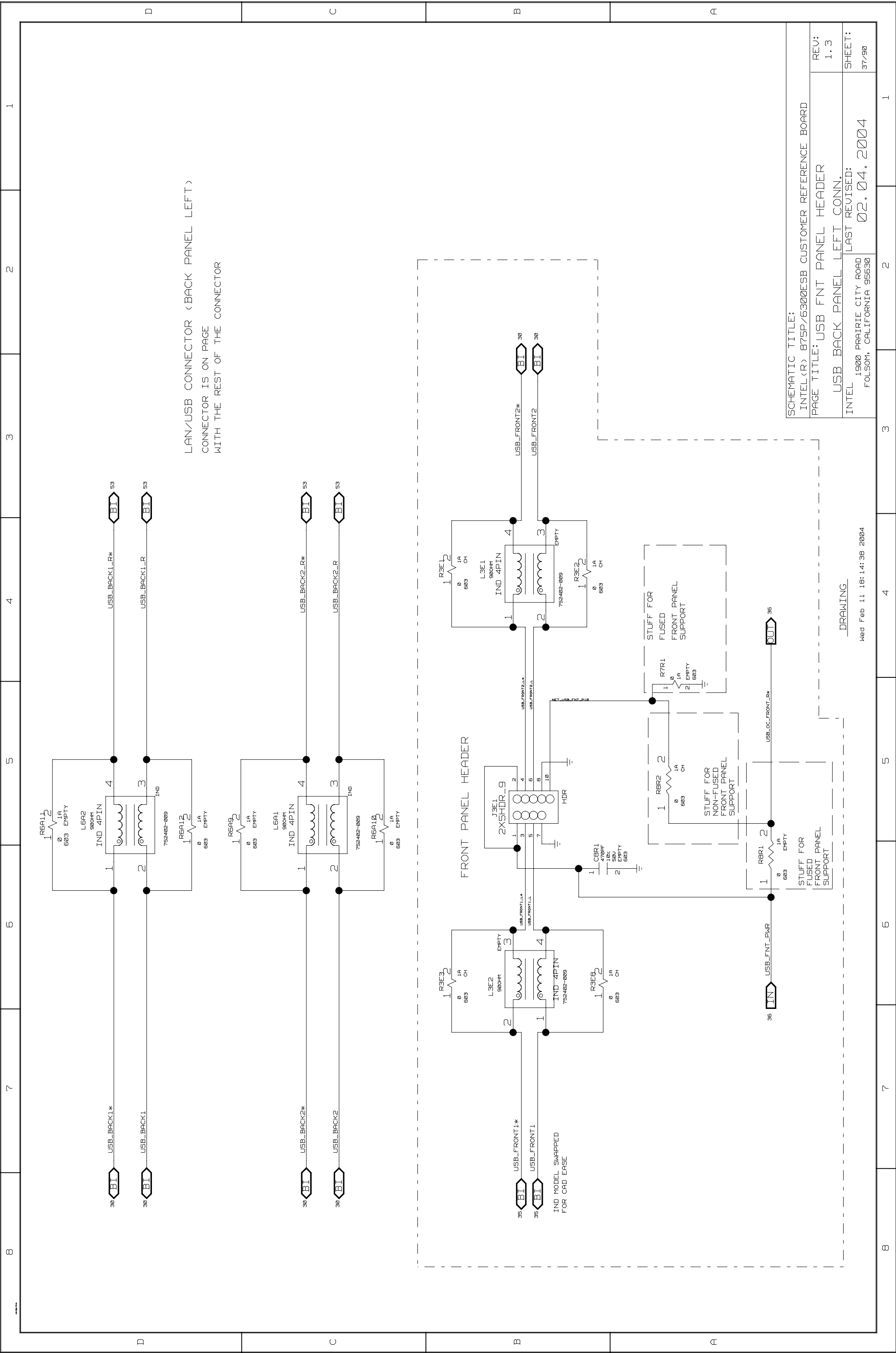


DRAWING

Wed Feb 11 18:14:23 2004

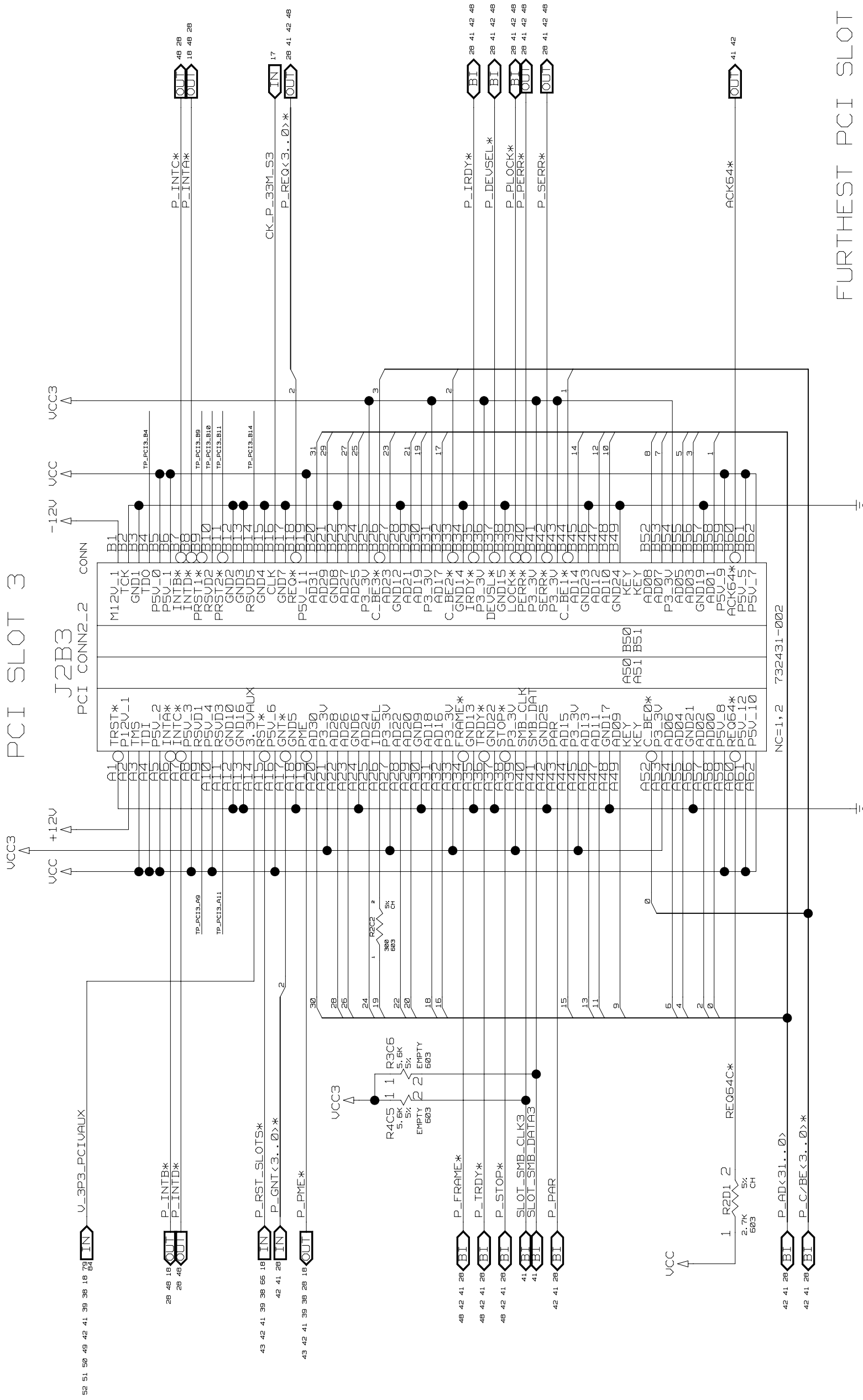












FURTHEST PCI SLOT FROM CPU

SCHEMATIC TITLE: INTEL(R) 875P/6300ESB CUSTOMER REFERENCE BOARD	
PAGE TITLE: PCI SLOT 3	REV: 1.3
INTEL 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: 02.04.2004
SHEET: 40/90	

## DRAWING

Wed Feb 11 18:15:01 2004

DESIGN NOTE:

PCI SLOT3 = PCI DEVICE FUNCTION 10H

= PCI DEVICE NUMBER 2H

= IDSEL VALUE AD18



1

LC

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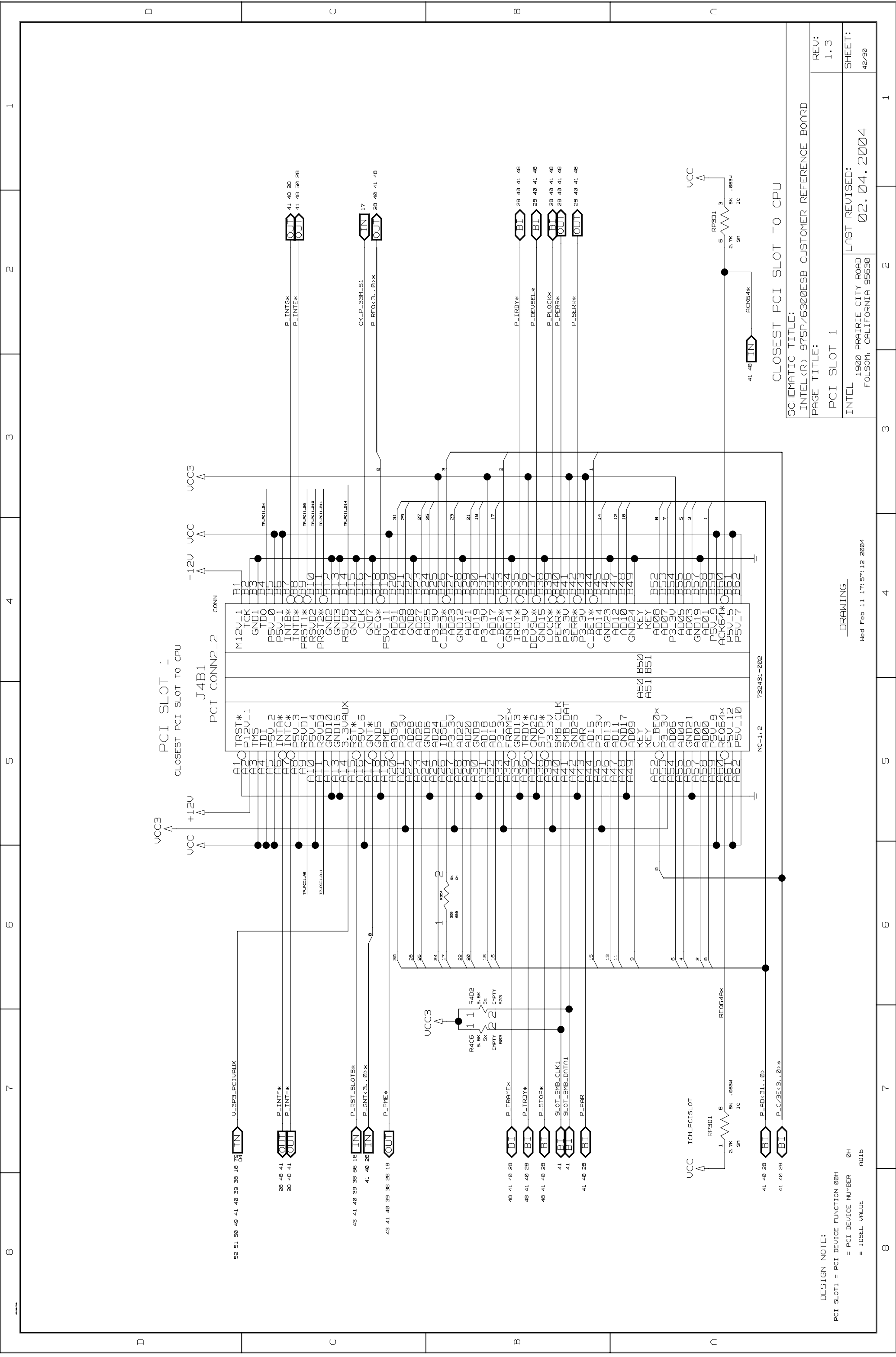
Q

LAST REVISED:

02.04.2004

1

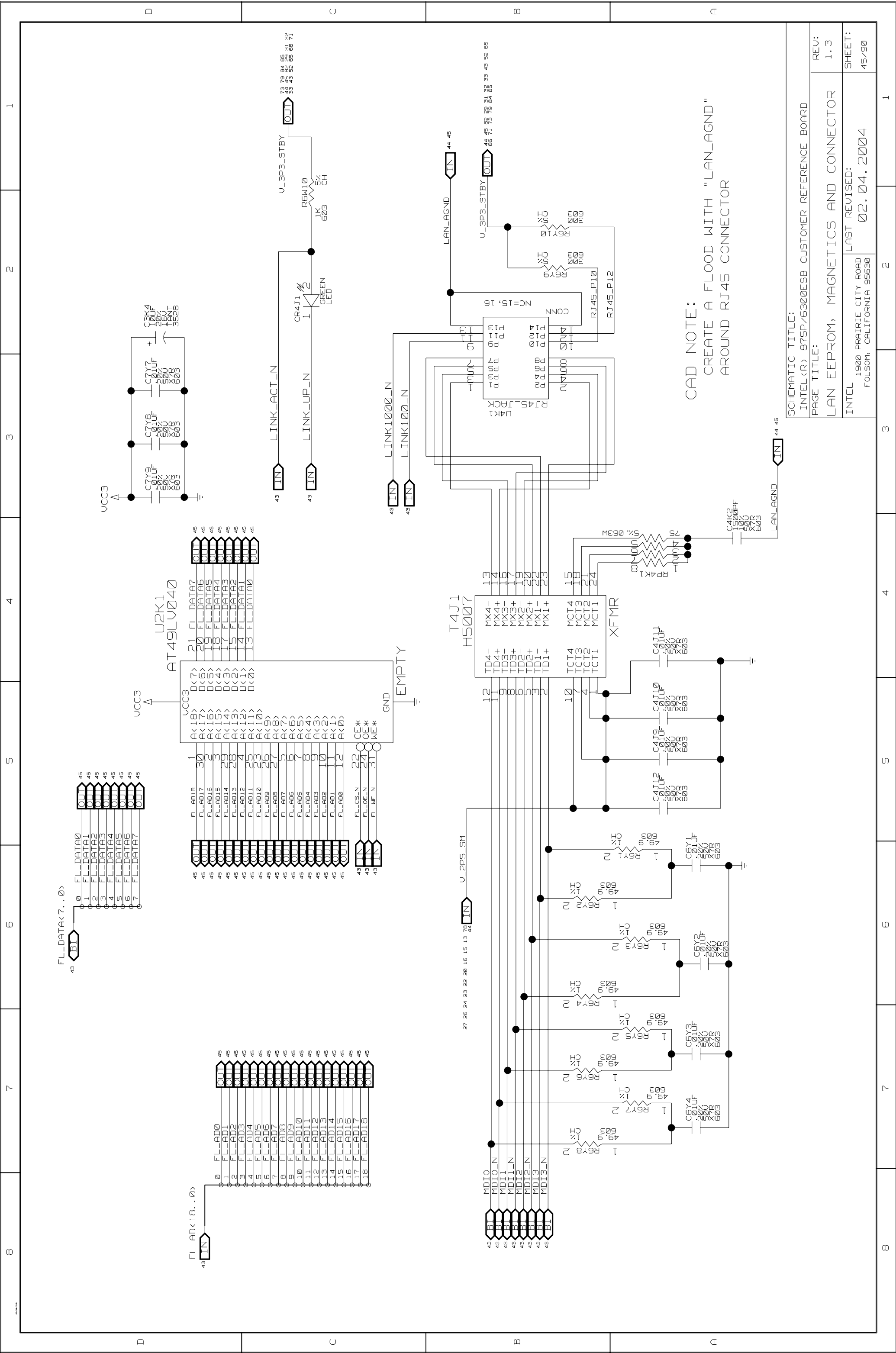




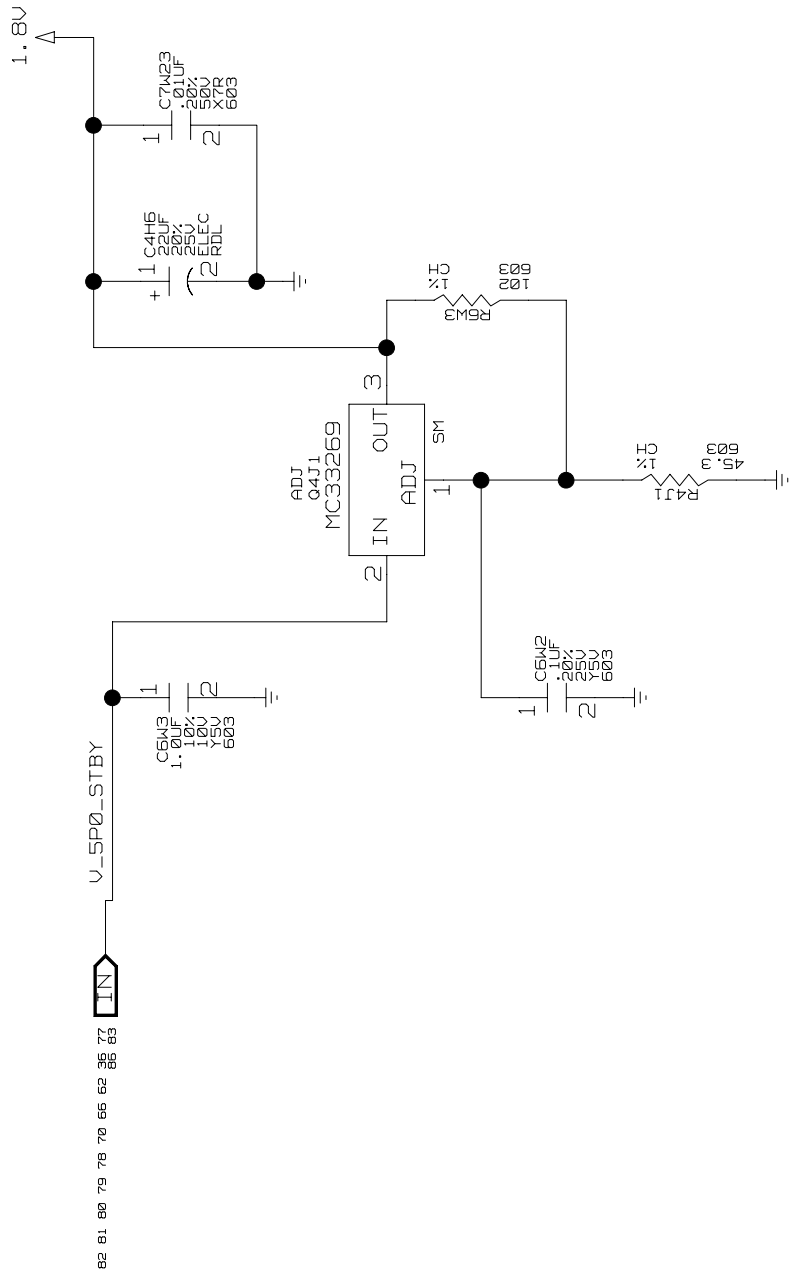








SCHEMATIC TITLE:		INTEL(R) 875P/5300ESB CUSTOMER REFERENCE BOARD	
PAGE TITLE:		REV: 1.3	
LAN EEPROM, MAGNETICS AND CONNECTOR		LAST REVISED:	
INTEL 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630		Ø2.04.2004	
SHEET: 45/90		1	



SCHEMATIC TITLE:

INTEL(R) 875P/6300ESB CUSTOMER REFERENCE BOARD

PAGE TITLE:

1.87 REF (GBE LAN)

INTEL

1900 PRAIRIE CITY ROAD

DRAWING

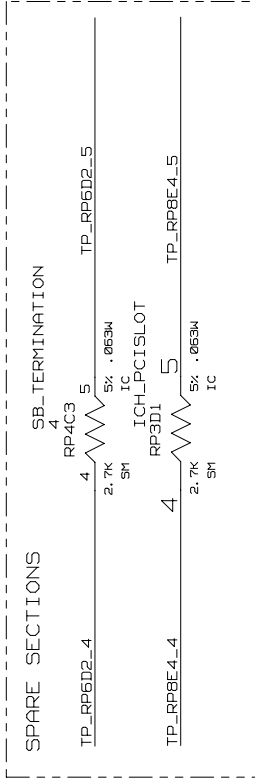
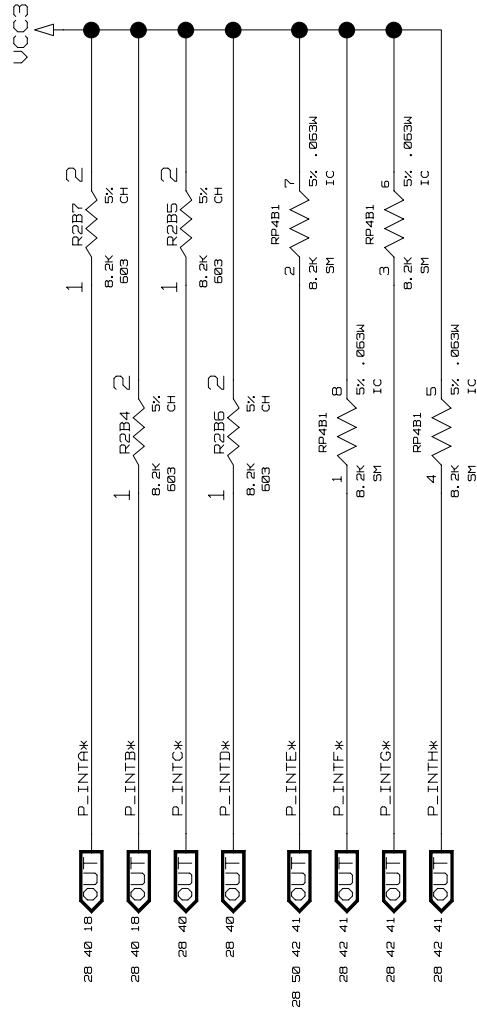
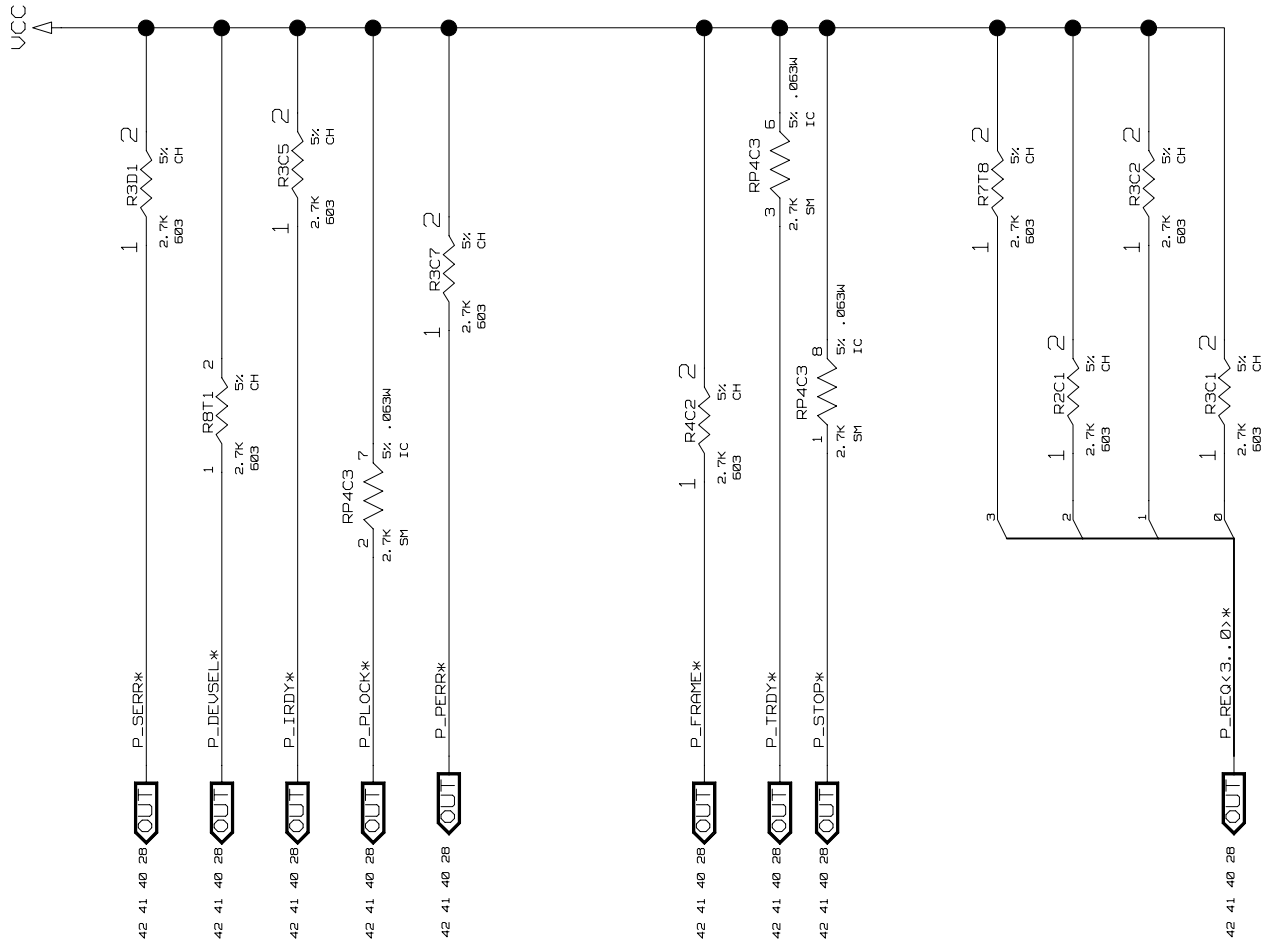
Wed Feb 11 17:56:35 2004

02.04.2004

46/90



# SECRET



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Wed Feb 11 17:56:19 2004

SCHEMATIC TITLE:

INTEL(R) 875P/6300ESB CUSTOMER REFERENCE BOARD

PAGE TITLE:

PCI TERMINATION

HEET:

LAST REVISED:

02.04.2004

48/90



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DRAWING

Wed Feb 11 17:56:19 2004

SCHEMATIC TITLE:

INTEL(R) 875P/6300ESB CUSTOMER REFERENCE BOARD

PAGE TITLE:

PCI TERMINATION

HEET:

LAST REVISED:

02.04.2004

48/90



1

U

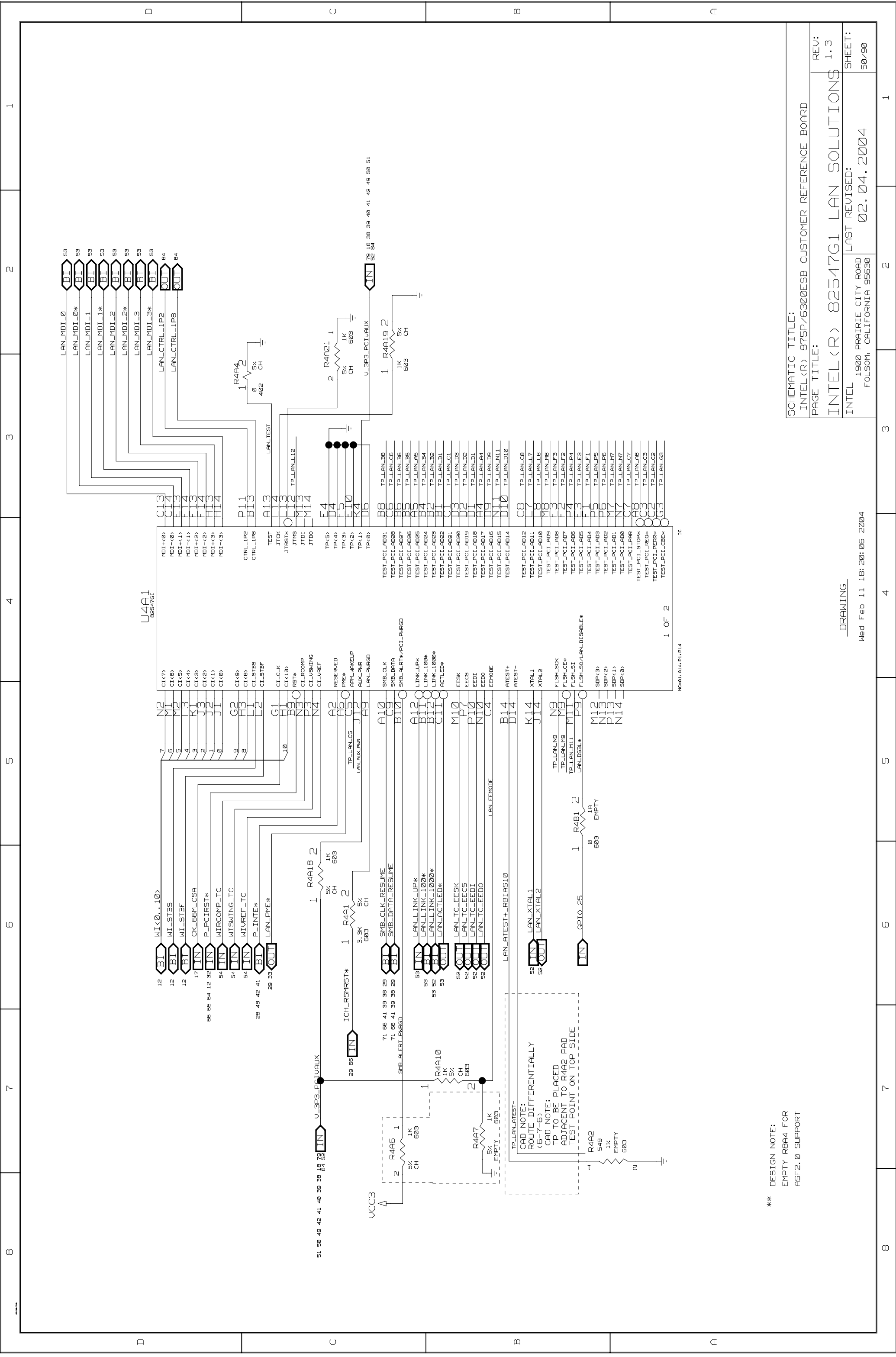
5

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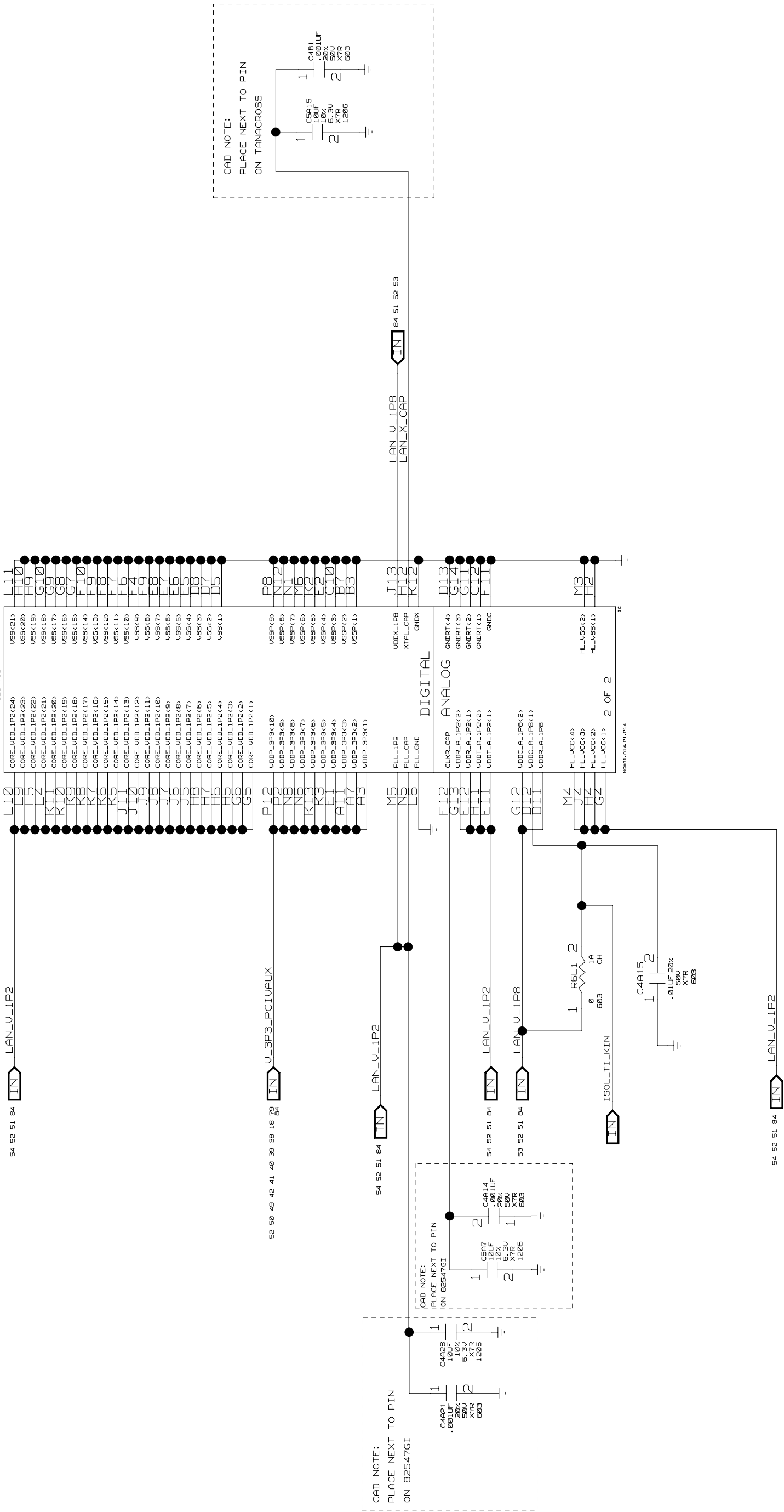


DESIGN NOTE:  
EMPTY RBA4 FOR  
ASF2.0 SUPPORT

DRAWING

Wed Feb 11 18:20:05 2004

SCHEMATIC TITLE:		INTEL(R) 875P/5300ESB CUSTOMER REFERENCE BOARD		REV:	1.3
PAGE TITLE:		INTEL(R) 82547G1 LAN SOLUTIONS		SHEET:	
INTEL		1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630		LAST REVISED:	
		Ø2.04.2004		50/90	



SCHEMATIC TITLE:

INTEL(R) 875P/6300ESB CUSTOMER REFERENCE BOARD

PAGE TITLE: \_\_\_\_\_ REV: \_\_\_\_\_

DRAWING

Wed Feb 11 18:20:14 2004

INTEL	LAST REVISED:	SHEET:
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1900 PRAIRIE CITY ROAD  
02-04-2004  
51/90

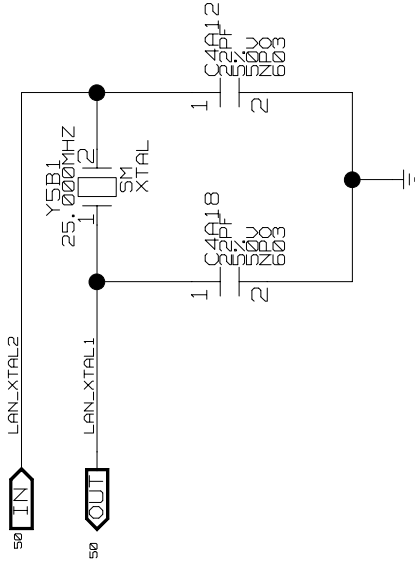
U





# EXTENSION

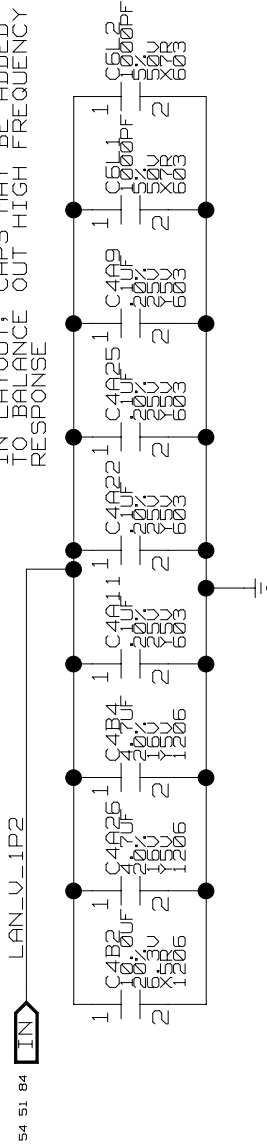
MINIMIZE XTAL TRACES  
DO NOT PLACE OR ROUTE NEAR PLANE SPLIT



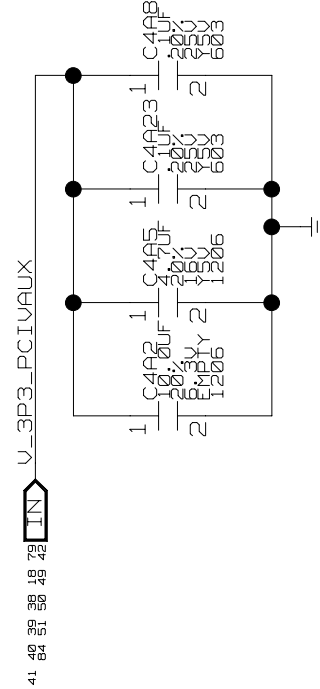
## LAN DECOUPLING

DESIGN NOTE:

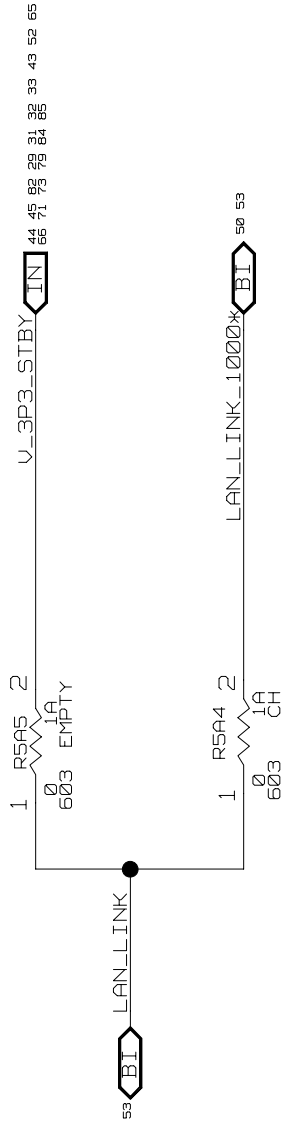
DEPENDENT ON POWER DELIVERY  
IN LAYOUT, CAPS MAY BE ADDED  
TO BALANCE OUT HIGH FREQUENCY  
RESPONSE



-----DESIGN NOTE:-----

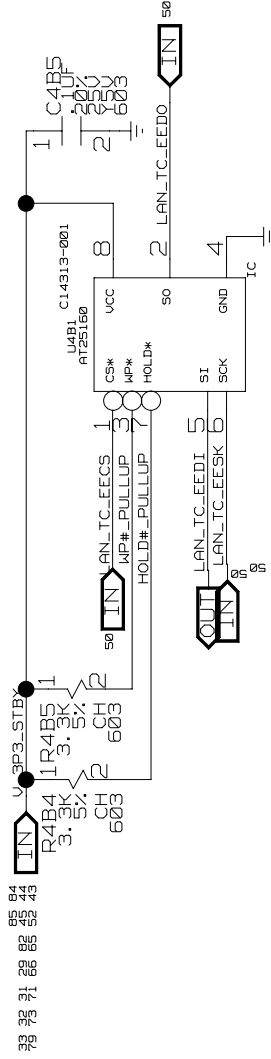
DECOUPLING CAPS SHARE BETWEEN  
82547GI VOLTAGE NETS

# STUFFING OPTIONS FOR LED ENABLING



## 82547GI EEPROM

CAD NOTE:  
PLACE EEPROM NEAR LAN CONTROLLER.



SCHEMATIC TITLE:

INTEL(R) 875P/6300ESB CUSTOMER REFERENCE BOARD

PAGE TITLE:

PAGE TITLE:	REV
INTEL 'D\ 82E172I MISS CIRCUITS	1.3

## DRAWING

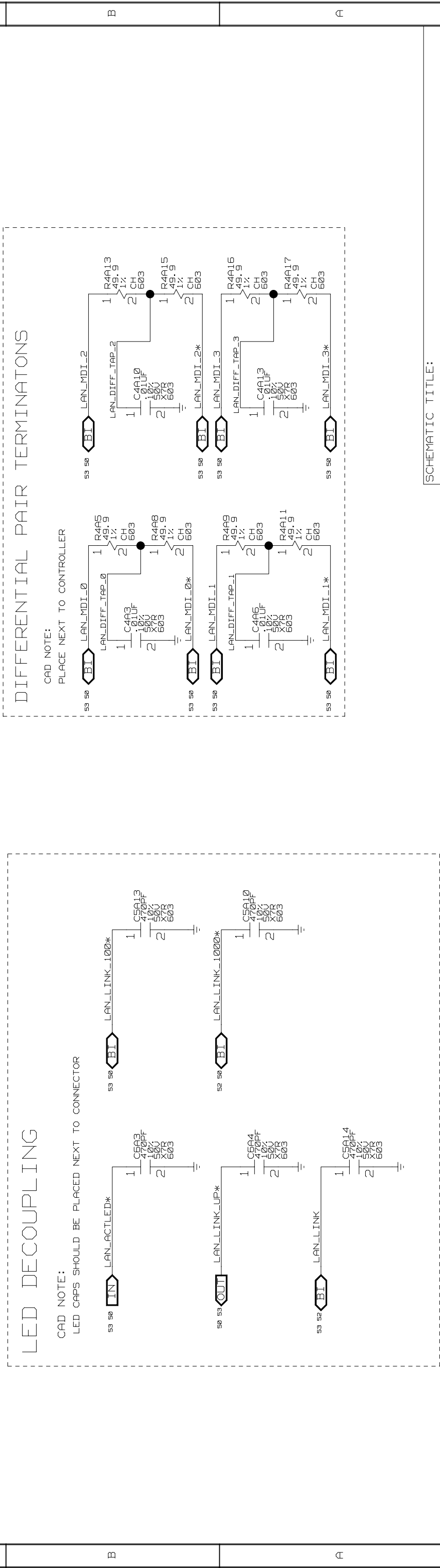
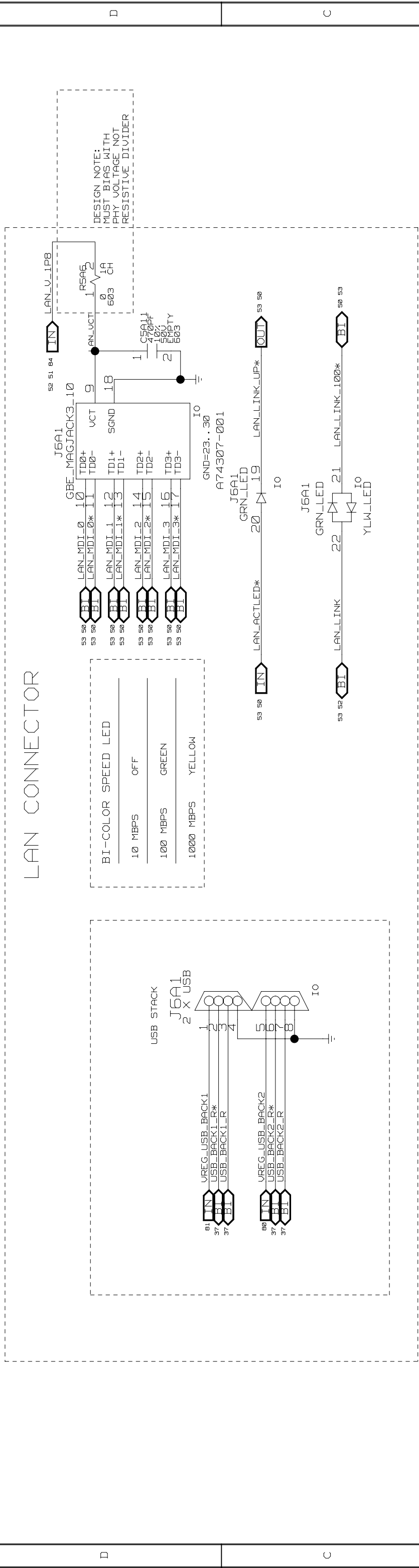
Wed Feb 11 18:20:23 2004

LAST REVISED:

2024.04.20

SHEET:

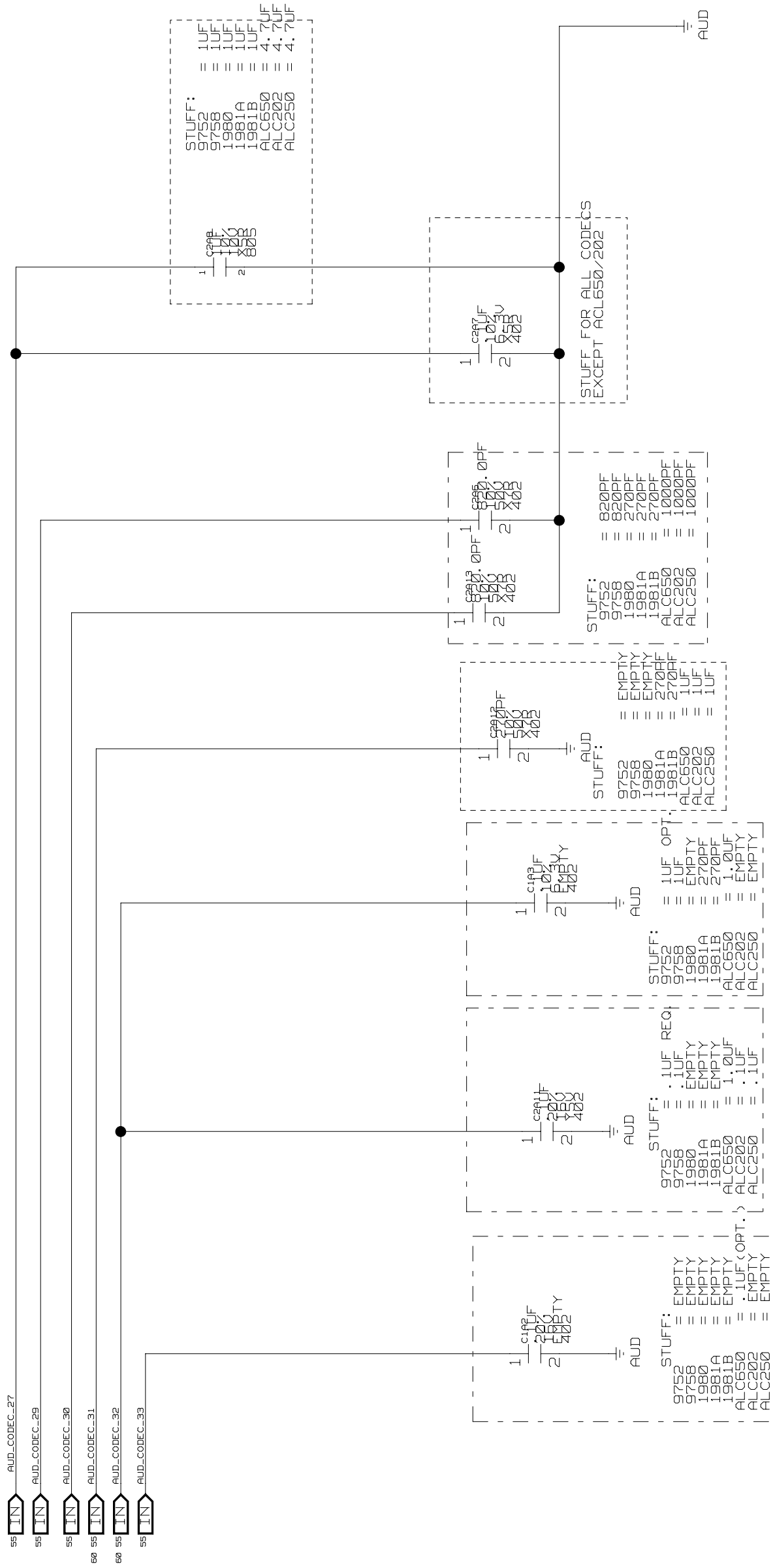
52/99



SCHEMATIC TITLE: INTEL(R) 875P/6300ESB CUSTOMER REFERENCE BOARD		REV: 1.3
PAGE TITLE: LAN MAGJACK & DIFF PAIR TERM		SHEET: 53/90
INTEL 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: 02.04.2004	



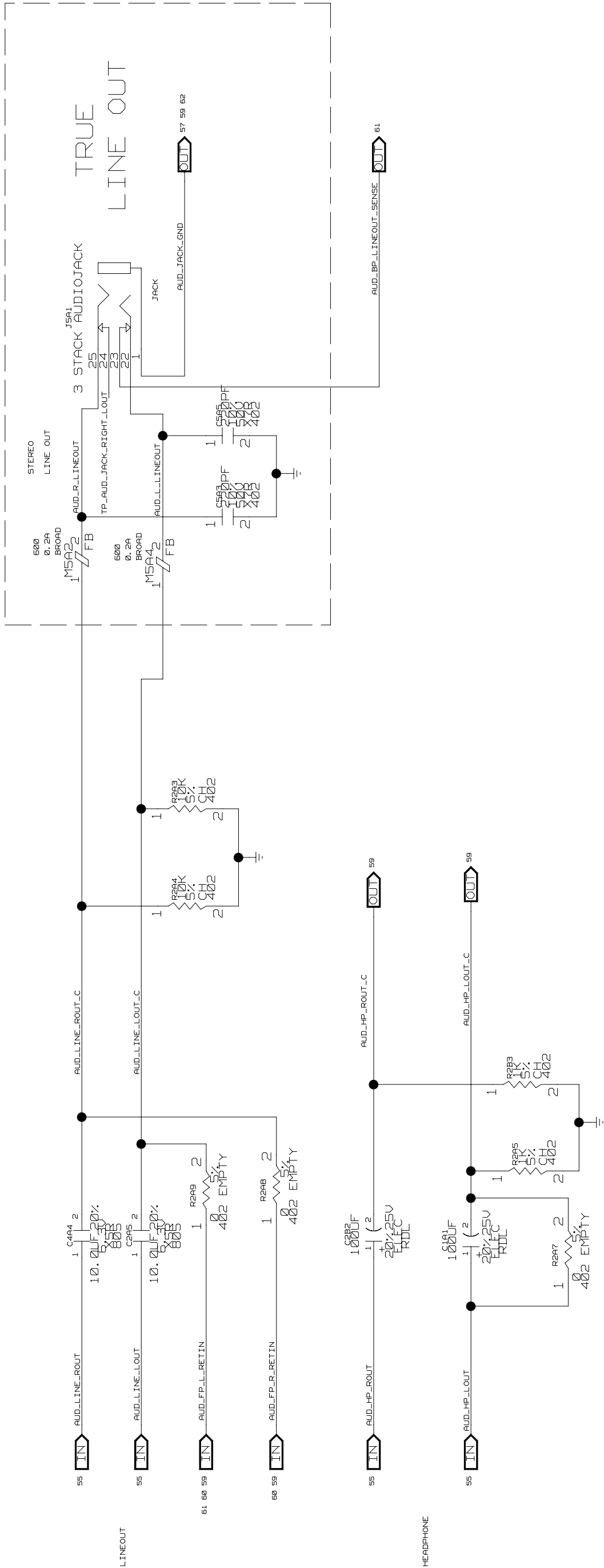




CODEC FILTER CAPS:

9752, 9758, 1980, 1981A, 1981B, ALC650, ALC202, ALC250





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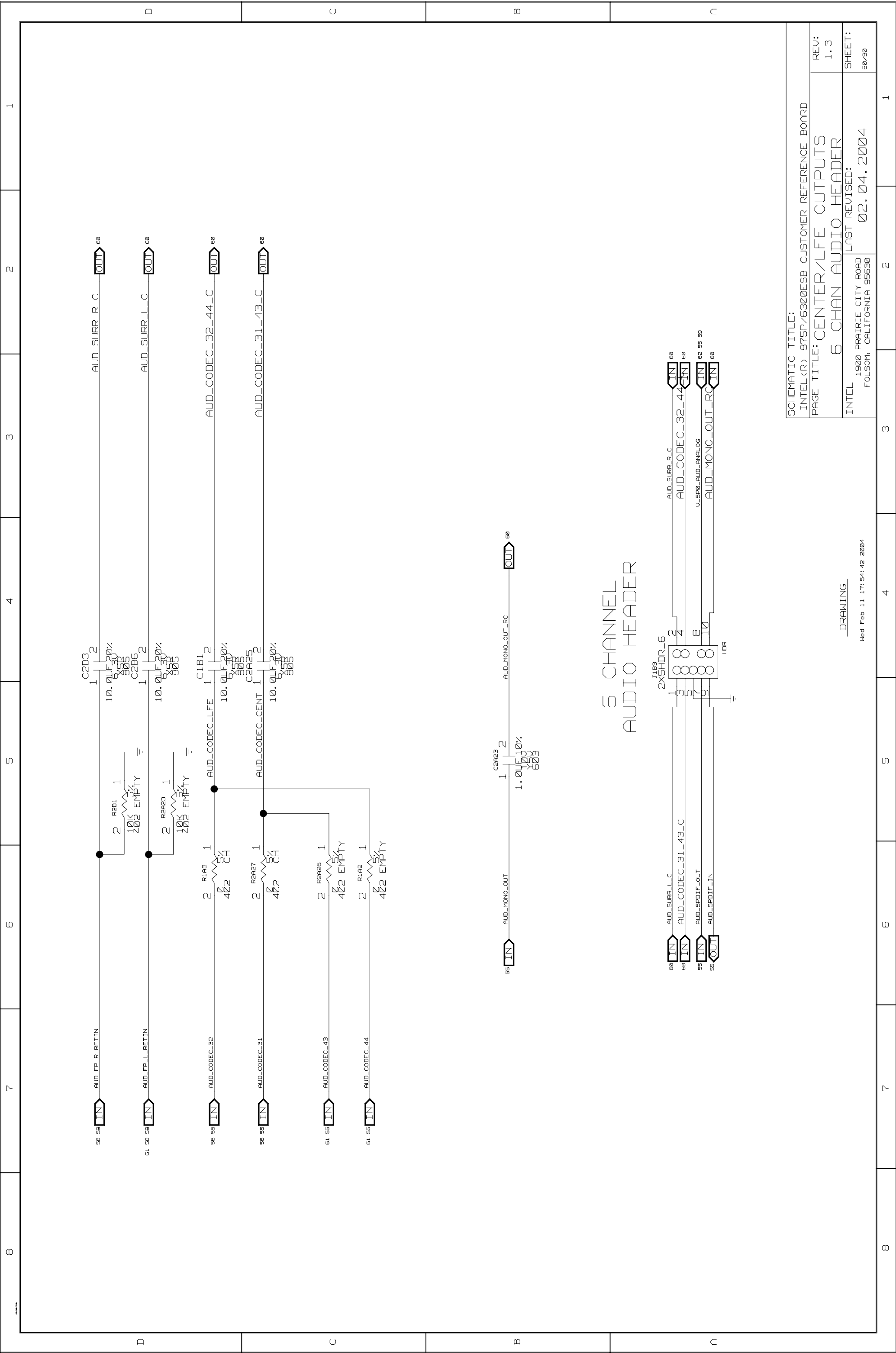
Wed Feb 11 17:54:58 2004

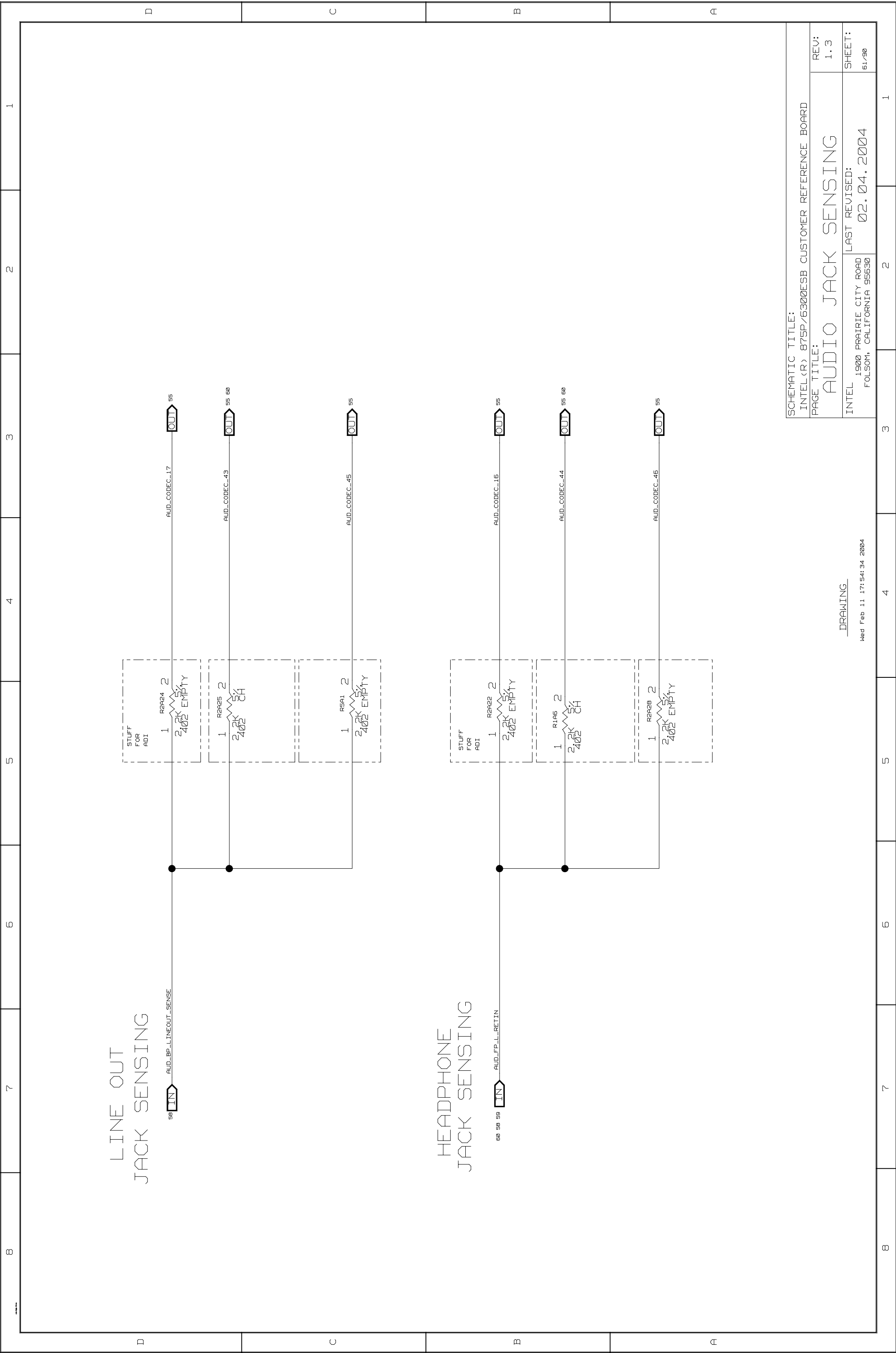
SCHEMATIC TITLE: INTEL(R) 875P/6300ESB CUSTOMER REFERENCE BOARD	
PAGE TITLE: LINE OUT CONN. (2 OF 3)	REV: 1.3
INTEL 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: 02.04.2004
SHEET: 58/90	

INTEL 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: 02.04.2004	SHEET: 58/90
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SCHMATIC TITLE:

INTEL(R) 875P/5300ESB CUSTOMER REFERENCE BOARD

PAGE TITLE:

AUDIO JACK SENSING

REV:

1.3

INTEL

1900 PRAIRIE CITY ROAD  
FOLSOM, CALIFORNIA 95630

LAST REVISED:

02.04.2004

SHEET:

61/90

DRAWING

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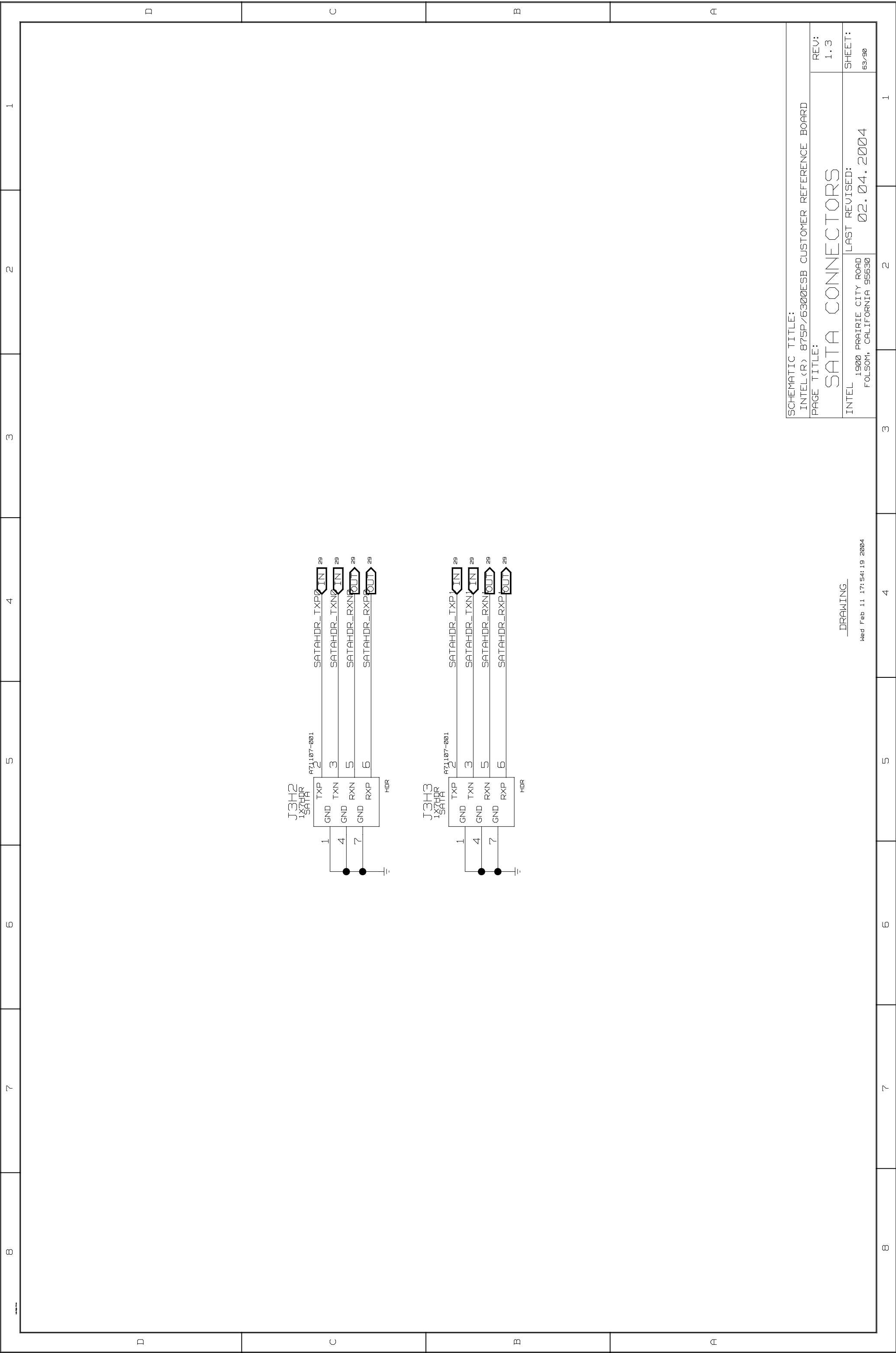
D

C

B

A





1

GND

4

GND

7

GND

2

TXP

3

TXN

5

RXN

6

RXP

SATAHDR

TXP1

TXN1

RXN1

RXP1

IN

IN

OUT

OUT

A71107-001

J3H3

1X HDR

SATA

8 7 | 6 | 5 | 4 | 3 | 2 | 1 || D | C | B | A |  | | | |

1

GND

4

GND

7

GND

2

TXP

3

TXN

5

RXN

6

RXP

SATAHDR

TXP0

TXN0

RXN0

RXP0

IN

IN

OUT

OUT

A71107-001

J3H2

1X HDR

SATA

1

GND

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GND

7

GND

2

TXP

3

TXN

5

RXN

6

RXP

SATAHDR

TXP1

TXN1

RXN1

RXP1

IN

IN

OUT

OUT

A71107-001

J3H3

1X HDR

SATA

8 7 | 6 | 5 | 4 | 3 | 2 | 1 || D | C | B | A |  | | | |

1

GND

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GND

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GND

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TXP

3

TXN

5

RXN

6

RXP

SATAHDR

TXP0

TXN0

RXN0

RXP0

IN

IN

OUT

OUT

A71107-001

J3H2

1X HDR

SATA

1

GND

4

GND

7

GND

2

TXP

3

TXN

5

RXN

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RXP

SATAHDR

TXP1

TXN1

RXN1

RXP1

IN

IN

OUT

OUT

A71107-001

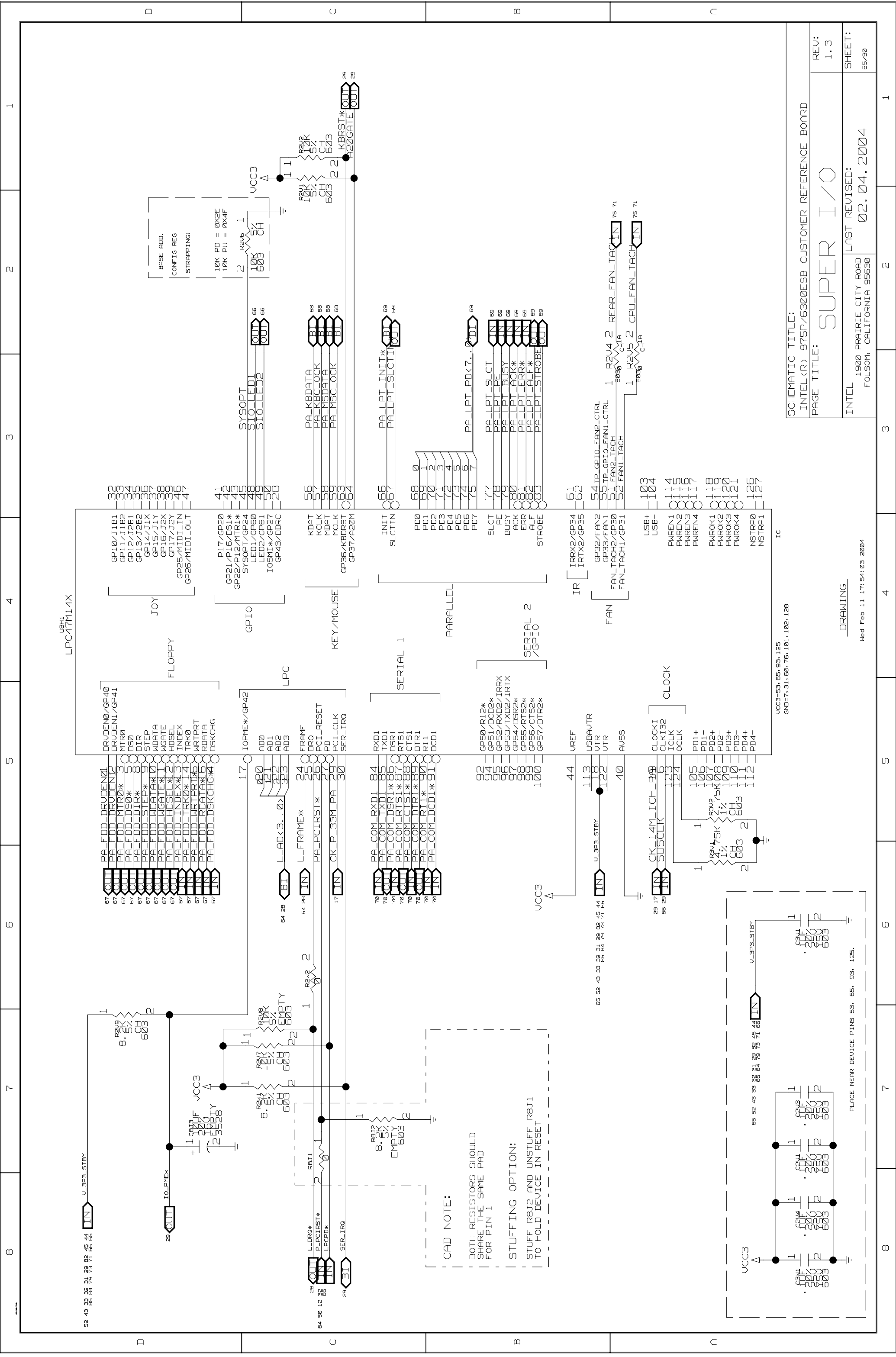
J3H3

1X HDR

SATA

SCHEMATIC TITLE:	
INTEL(R) 875P/5300ESB CUSTOMER REFERENCE BOARD	
PAGE TITLE:	REV:
SATA CONNECTORS	1.3
INTEL	LAST REVISED:
1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	02.04.2004
	SHEET:
	63/90





SCHEMATIC TITLE:			INTEL (R) 875P/5300ESB CUSTOMER REFERENCE BOARD	
PAGE TITLE:			SUPER I/O	
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1900 PRAIRIE CITY ROAD			02.04.2004	
FOLSOM, CALIFORNIA 95630				

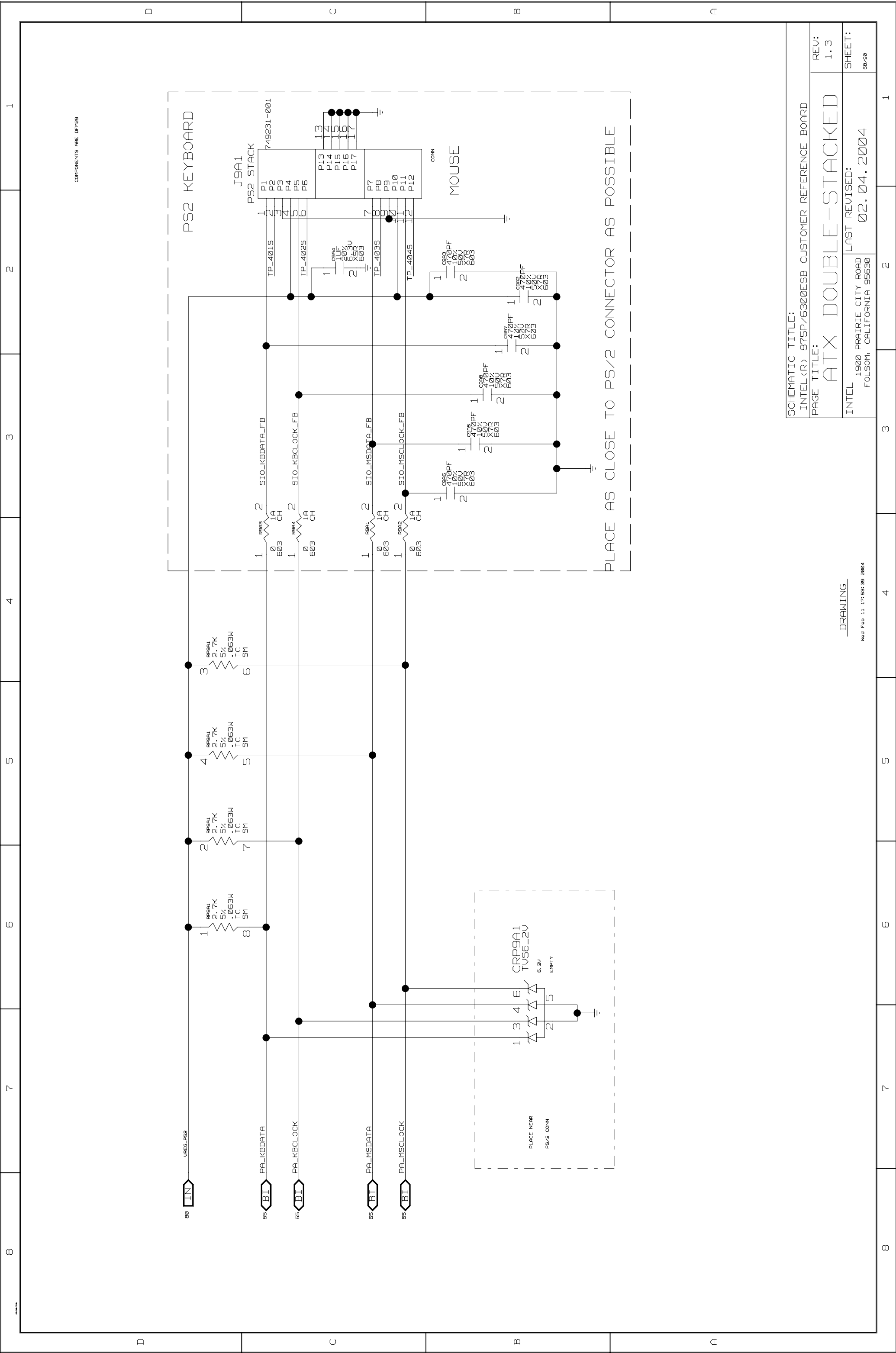
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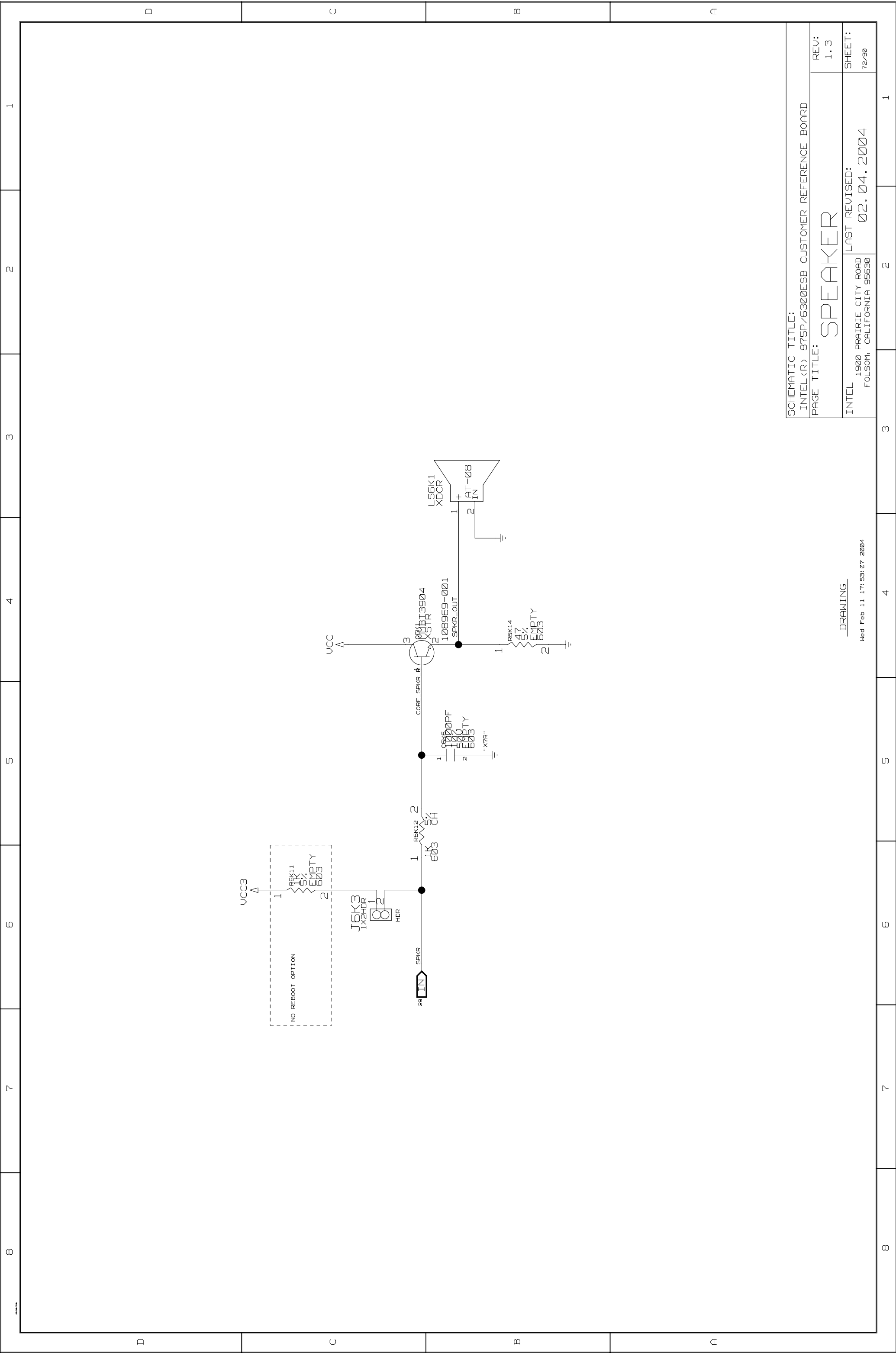






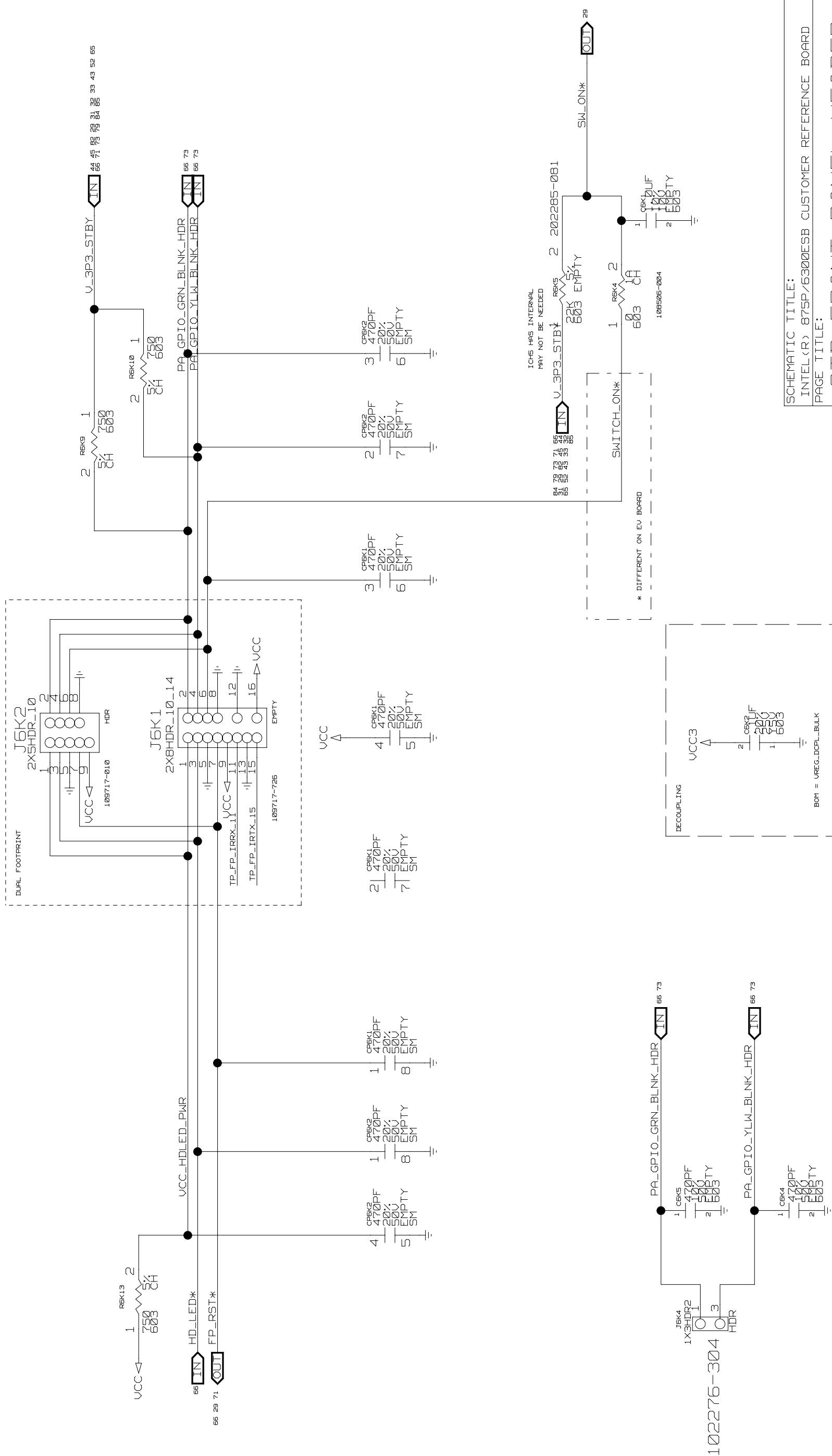
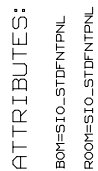






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INTEL 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: 02.04.2004
SHEET: 73/90	

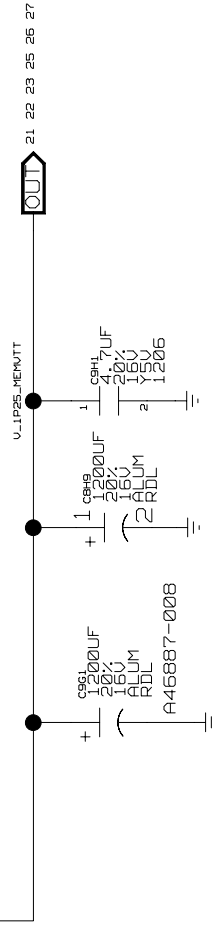
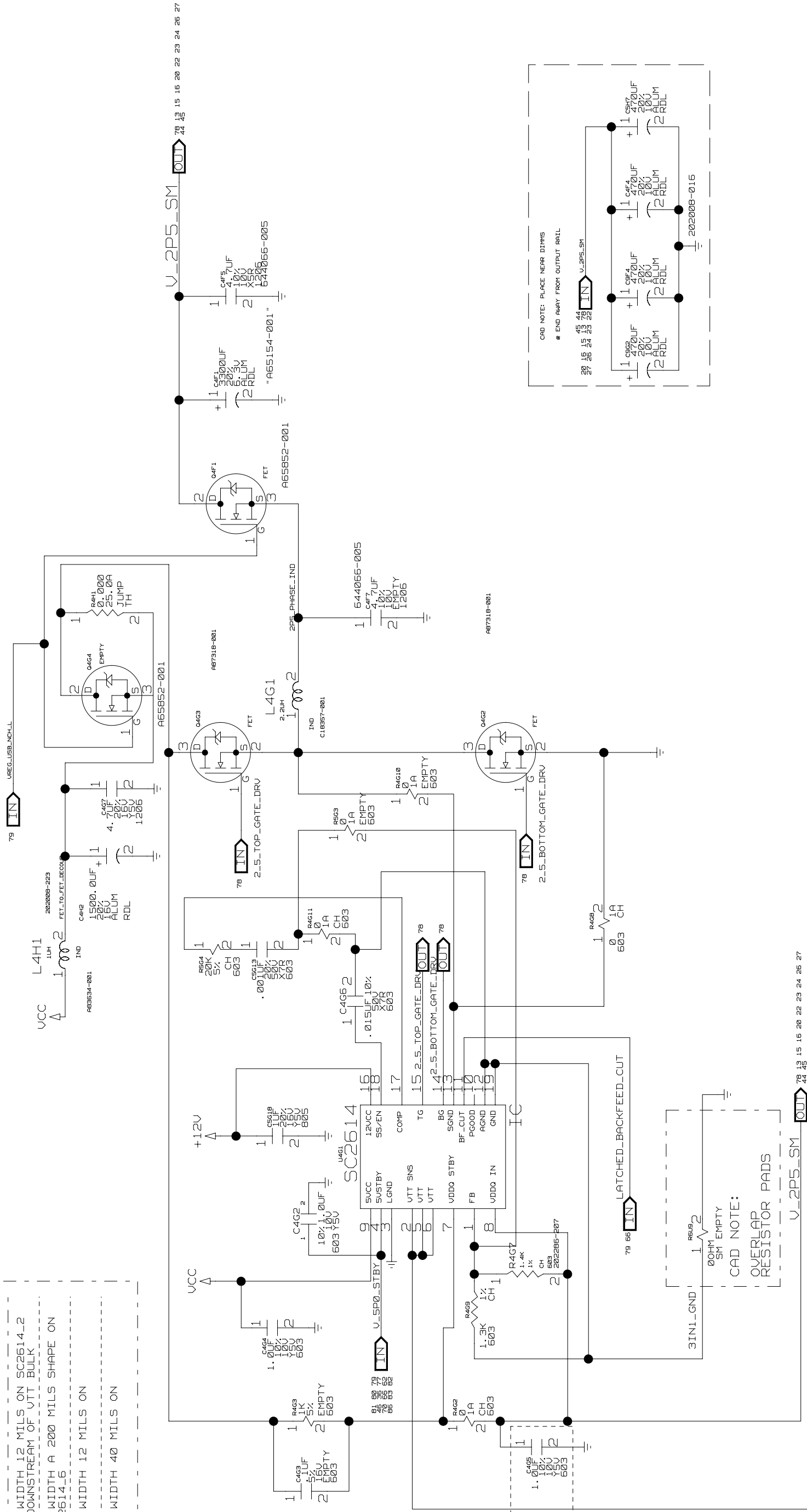
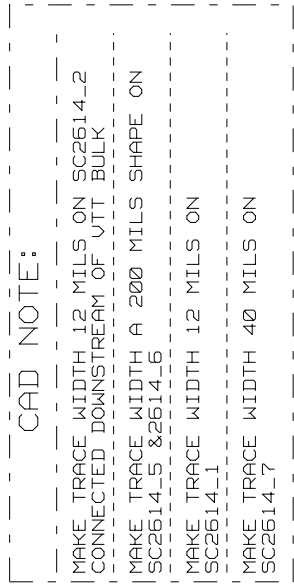






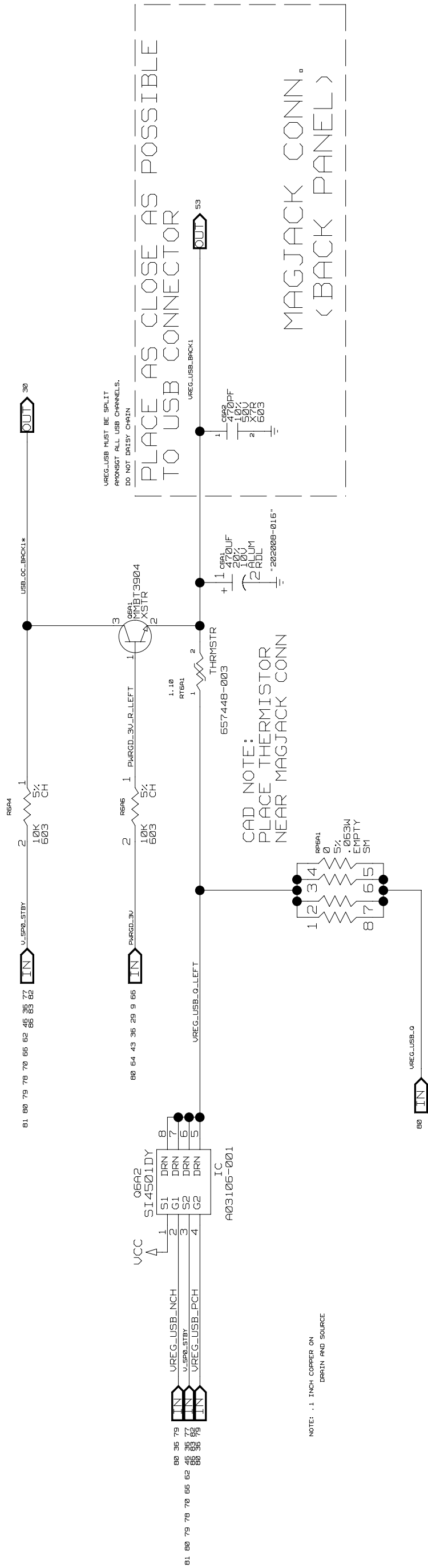












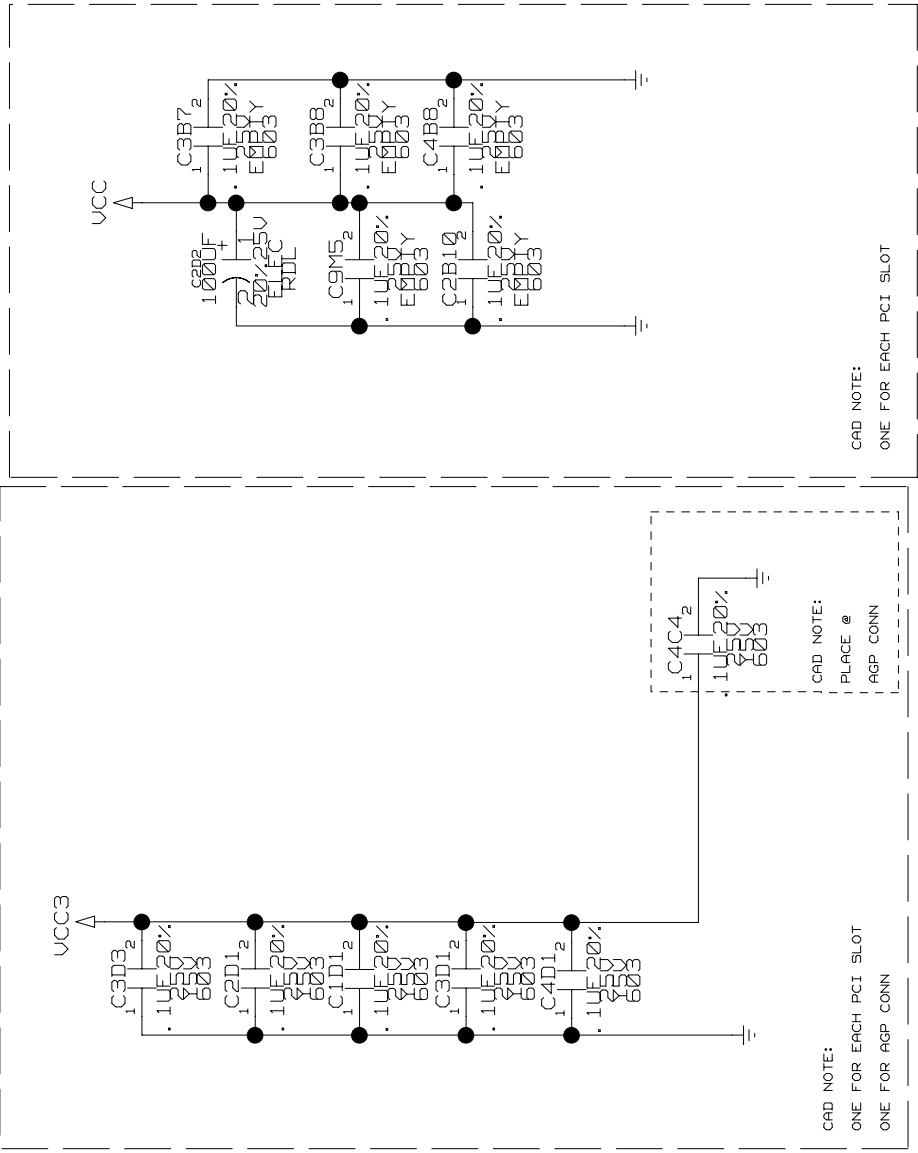
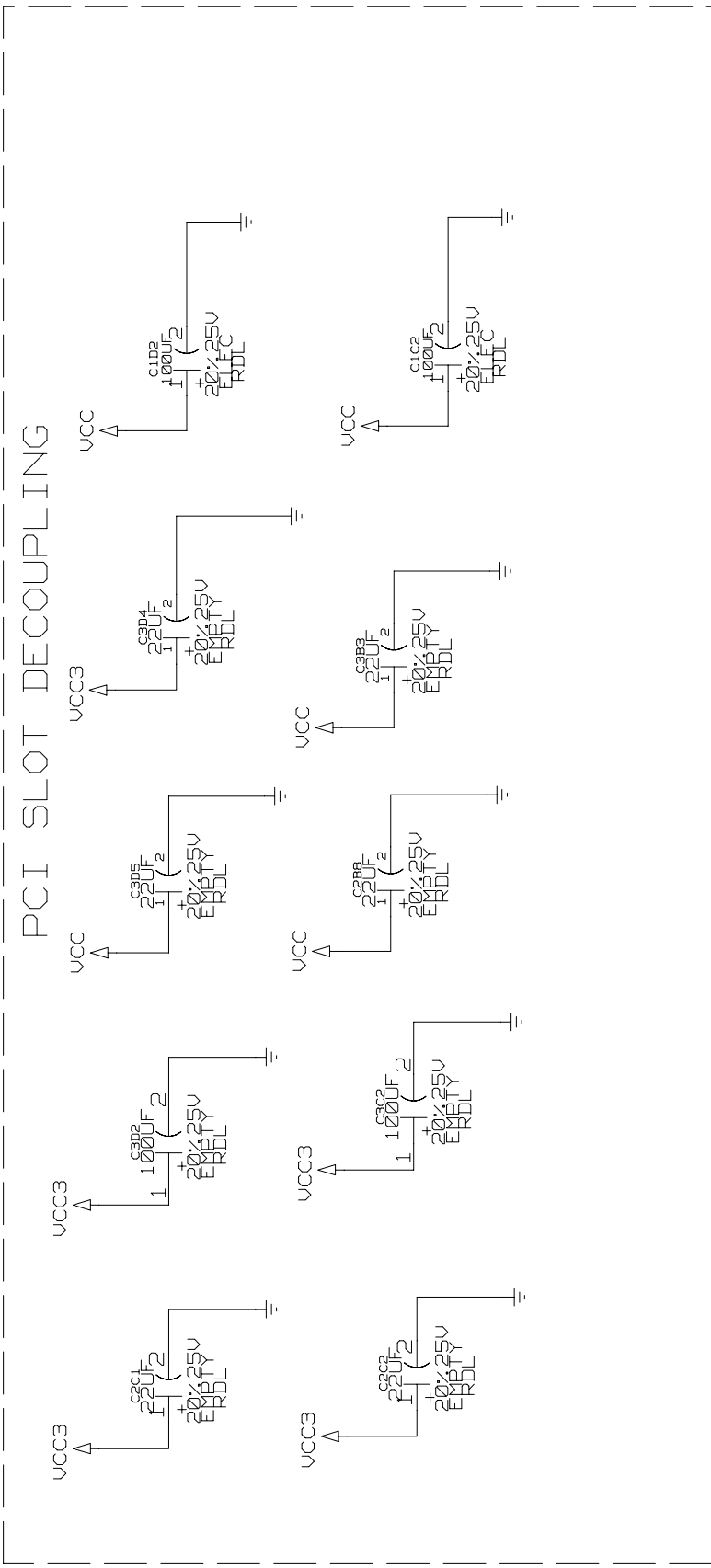
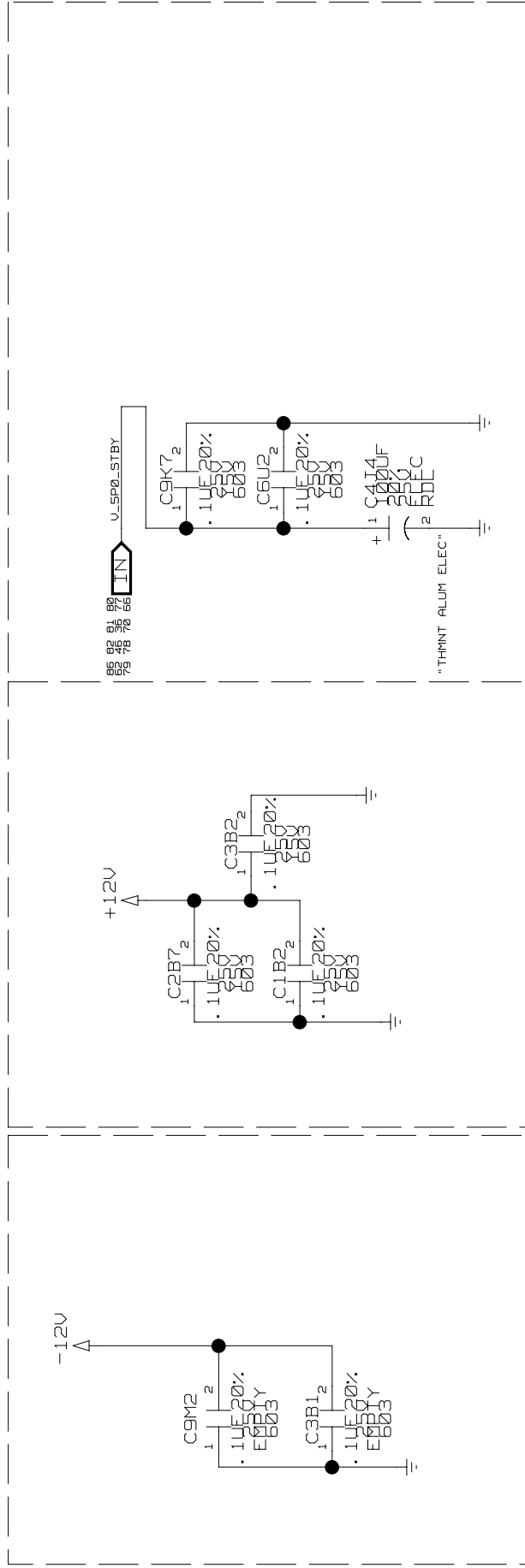
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Wed Feb 11 17:51:56 2004

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INTEL 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: 02.04.2004
SHEET: B1/90	



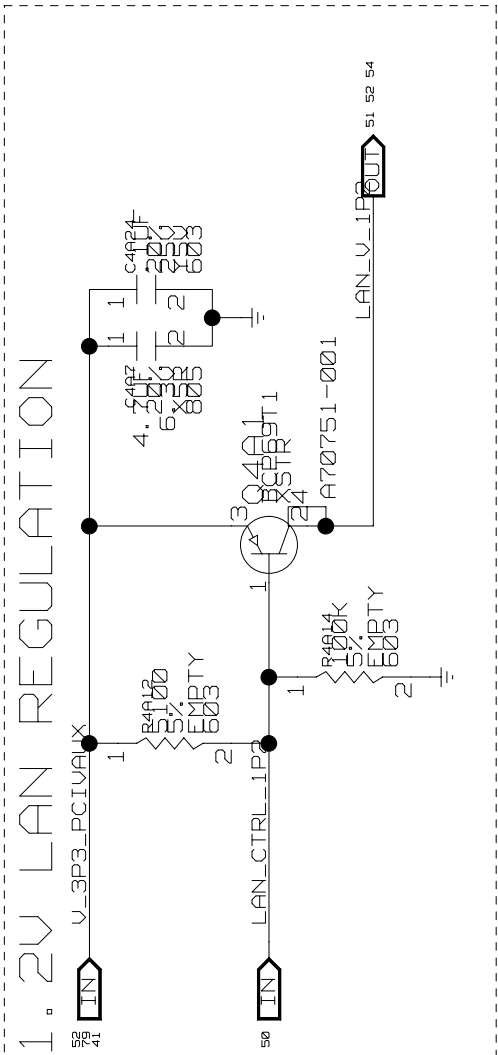


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SHEET: 83/90	

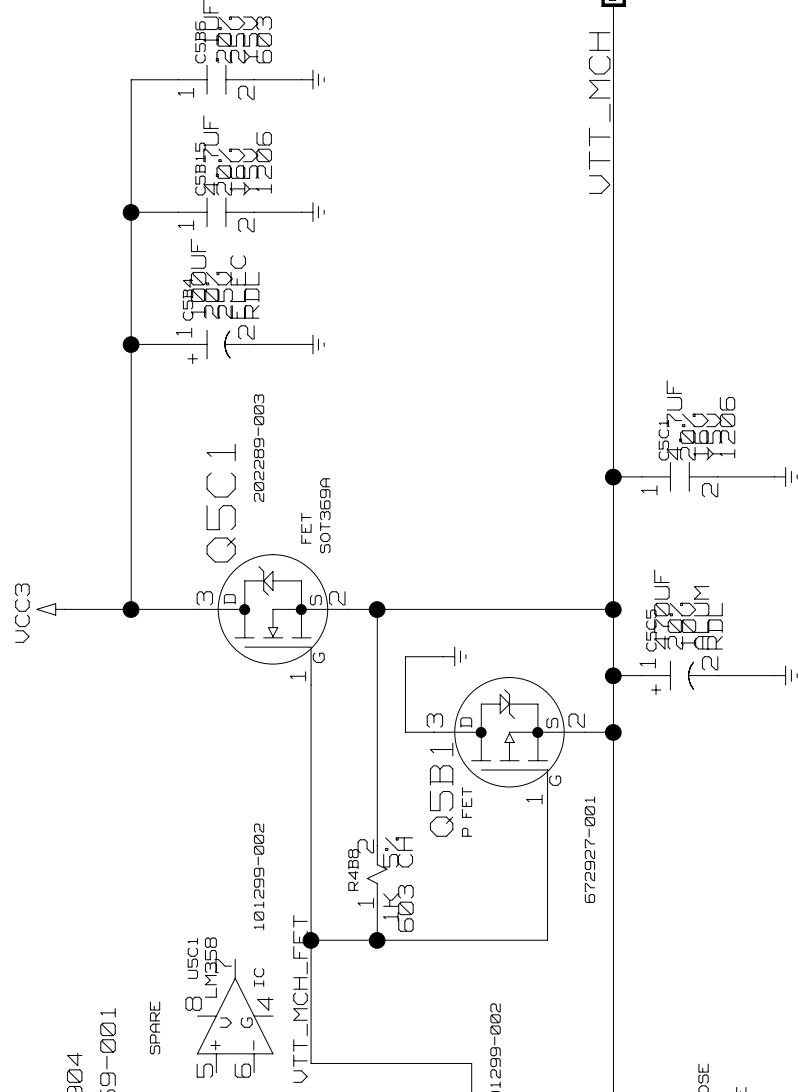
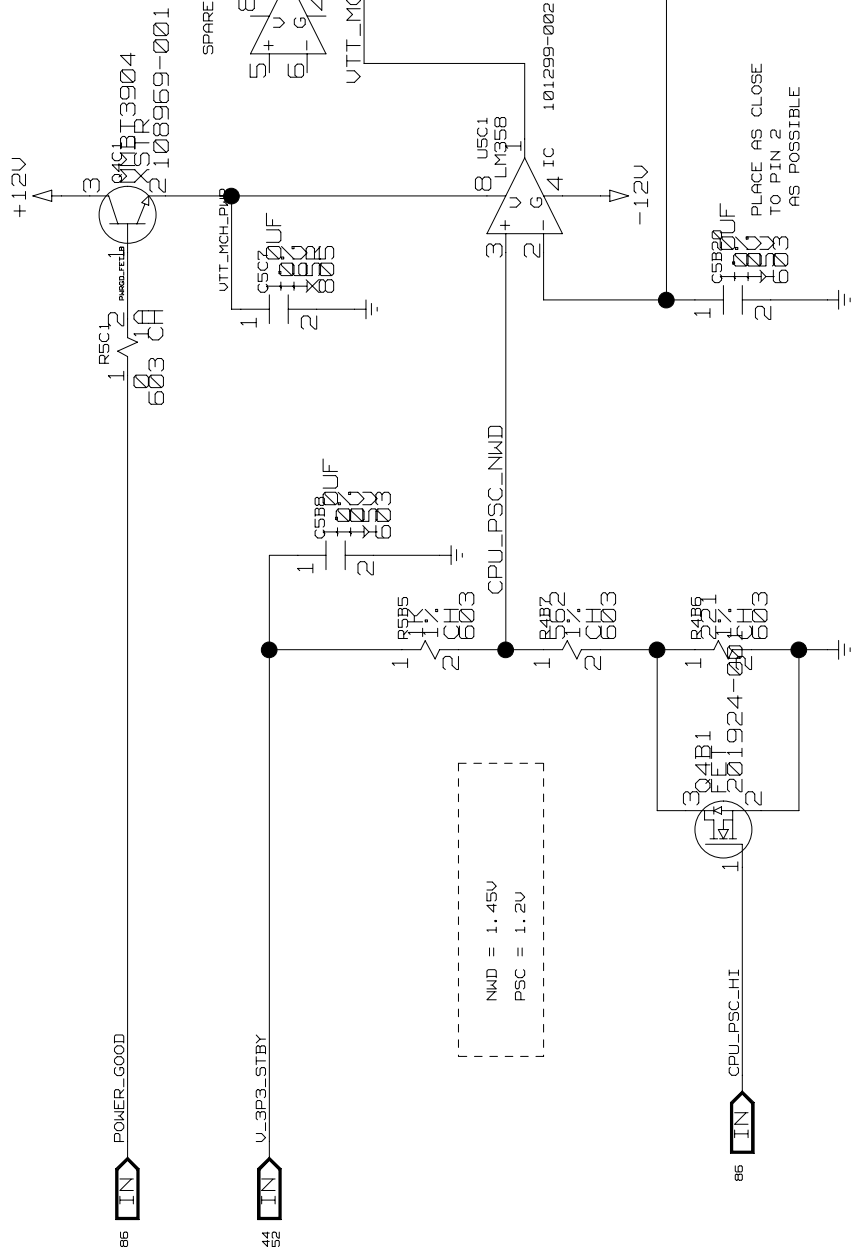
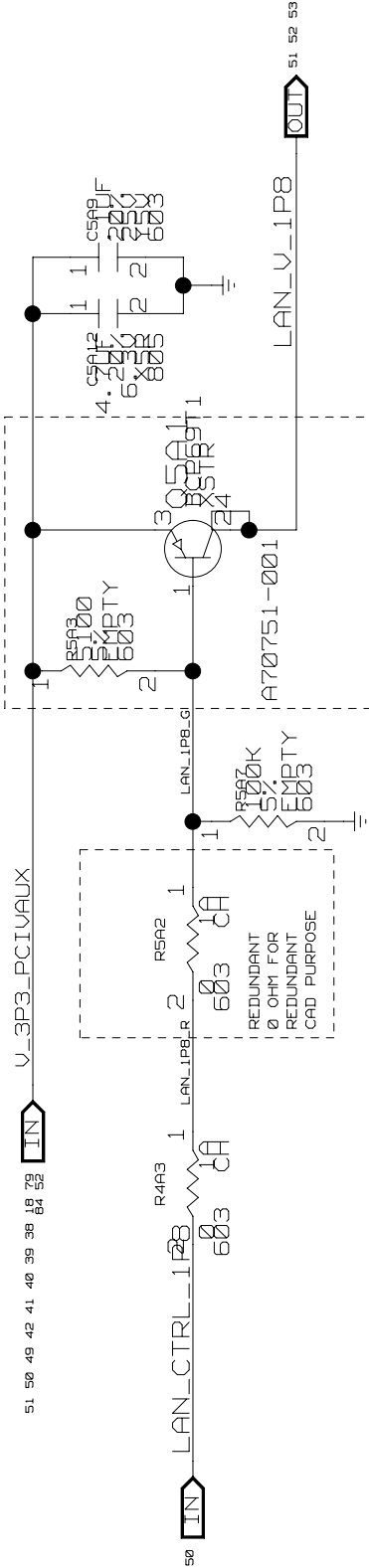
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## 1.8V LAM REGULATION



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INTEL(R) 875P/6300ESB CUSTOMER REFERENCE BOARD

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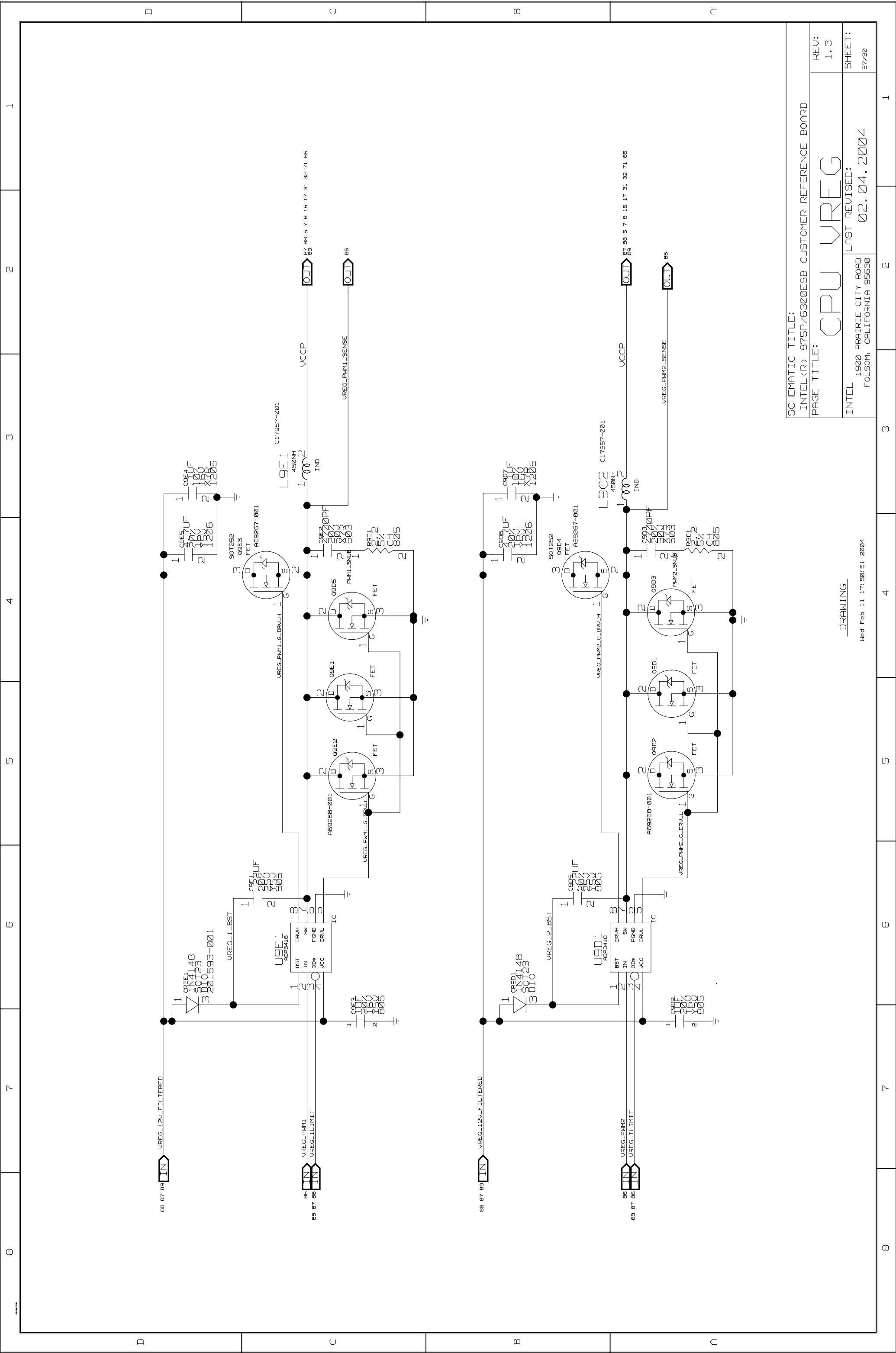
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INTEL	1900 PRAIRIE CITY ROAD 501 SOM COLLENTIA DES20	LAST REVISED: 02.04.2004
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SCHEMATIC TITLE:			INTEL(R) 875P/5300ESB CUSTOMER REFERENCE BOARD			REV:		
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INTEL			LAST REVISED:			SHEET:		
1900 PRAIRIE CITY ROAD			02.04.2004			87/90		
FOLSOM, CALIFORNIA 95630								

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